DATA HANDBOOK

ICs for Telecom
Subscriber Sets
Cordless Telephones
Mobile/cellular
Radio Pagers
CA3089 to PCD4413

BOOK IC03a 1991

Philips Semiconductors

PHILIPS

ICs for Telecom
Subscriber sets
Cordless Telephones
Mobile/Cellular
Radio Pagers

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COMPARISON OF THE TEA1060 FAMILY

	60	61	62	63	64A	66T	67	68
Microphones								
low sensitivity dynamic or magnetic	•					•		•
medium sensitivity: dynamic or magnetic	•		•	•	•	•	•	•
electret with preamplifier		•	•	•	•	•	•	•
piezo-electric		•	•	•	•	•	•	•
very accurate microphone matching			•	•	•		•	•
dynamic limiter				•	•			
Earpiece outputs								
dynamic or magnetic or piezo (17 to 39 dB)	•	•	•			•		•
dynamic or magnetic or piezo (20 to 45 dB)					•		•	
dynamic or magnetic or piezo (23 to 48 dB)				•				
Power-down input	•	•		•	•	•	•	•
DTMF and MUTE input	•	•	•	•	•	•	•	•
Voltage regulator								
adjustable DC voltage/resistance	•	•	•	•	•	•	•	•
parallel operation possible			•	•	•		•	
Peripheral supply								
unregulated - limited power	•	•	•			•	•	•
unregulated - extended power				•	•			
stabilized - extended power				•	•			
Automatic line loss compensation	•	•	•	•(1)	•	•	•	•

(1) 9 dB range instead of 6 dB.

COMPARISON OF MICROCONTROLLERS FOR TELEPHONE SETS

Type	ROM	RAM	I/O	I²C	pins	comments
PCD3315	1.5 K	160	20	Y	28	
PCD3343	3 K	224	20	Y	28	
PCD3344	2 K	224	20	N	28	plus DTMF
PCD3346	4 K	128	20	Y	28	plus 256 x 8 EEPROM
PCD3347	1.5 K	64	12	N	20	plus DTMF
PCD3348	8 K	256	20	Y	28	
PCD3349	4 K	224	20	N	28	plus DTMF
PCF84C00	-	256	20	Y	28	
PCF84C12	1 K	64	13	N	20	
PCF84C21C	2 K	64	20	Y	28	
PCF84C22	2 K	64	13	N	20	
PCF84C41C	4 K	128	20	Y	28	
PCF84C42	4 K	64	13	N	20	
PCF84C81C	8 K	256	20	Y	28	
PCF84C85	8 K	256	32	Y	40	

Product status definitions

for type numbers with prefixes
CA, MC, NE, SA and SE

Ordering information

for type numbers with prefixes
CA, MC, NE, SA and SE

Type designation

for type numbers with prefixes
FCB, FCF, OM, PCA, PCB, PCD,
PCF, TDA, TDD, TEA, UAA and UMA

Rating systems

for type numbers with prefixes
FCB, FCF, OM, PCA, PCB, PCD,
PCF, TDA, TDD, TEA, UAA and UMA

Handling MOS devices

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

ORDERING INFORMATION

Signetics' Linear LSI integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:

$1000 per order

$250 per line item per order

Military Product:

$250 per line item per order

Table 1 provides part number information concerning Signetics originated products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Tables 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted, however, that devices with a SE prefix (– 55°C to + 125°C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any Linear LSI product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

Table 1 PART NUMBER DESCRIPTION

PART NUMBER	CROSS REF PART NO.	PRODUCT FAMILY	PRODUCT DESCRIPTION
NE5537N	LF398	LIN	Sample & Hold Amp

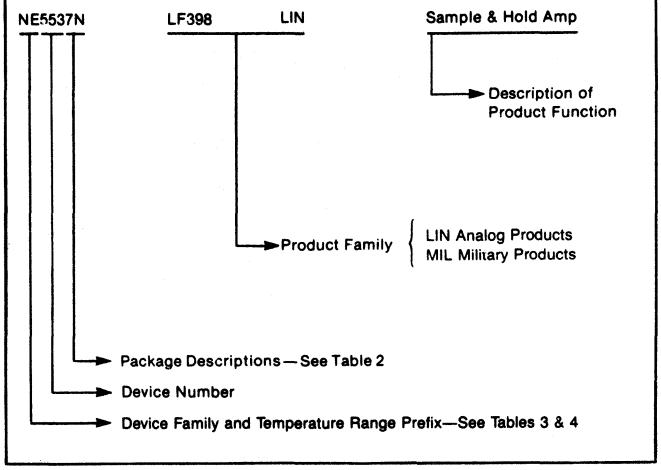


Table 2 PACKAGE DESCRIPTIONS

Old	New	PACKAGE DESCRIPTION
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
-	D	Microminiature package (SO)
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
T,TA	H	8-lead TO-99
U	U	SIL Plastic power
V	N	8-lead plastic DIL
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 3 SIGNETICS PREFIX AND DEVICE TEMPERATURE

PREFIX	DEVICE TEMPERATURE RANGE
N	0° to + 70°C
S	– 55° to + 125°C
NE	0° to + 70°C
SE	– 55° to + 125°C
SA	– 40° to + 85°C

Table 4 INDUSTRY STANDARD PREFIX

PREFIX	DEVICE FAMILY
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
JB	Mil Rel—Jan Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LF	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
NE	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
ULN	Linear Industry Standard

Pro electron type designation code for integrated circuits

TYPE DESIGNATION

Basic type number

This type designation applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick- film and hybrid integrated circuits.

A basic type number consists of three letters followed by a serial number.

FIRST AND SECOND LETTER

Digital family circuits

The first two letters identify the family (see note 1).

Solitary circuits

The first letter divides the solitary circuits into:

S : solitary digital circuits
T : analog circuits
U : mixed analog/digital circuits

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits (see note 2).

Microprocessors

The first two letters identify microprocessors and correlated circuits as follows:

MA: microcomputer central processing unit
MB: slice processor (see note 3)
MD: correlated memories
ME: other correlated circuits (interface, clock, peripheral controller, etc.)

Charge-transfer devices and switched capacitors.

The first two letters identify the following:

NH : hybrid circuits
NL : logic circuits
NM: memories
NS : analog signal processing, using switched capacitors
NT : analog signal processing, using change-transfer device
NX : imaging devices
NY : other correlated circuits

THIRD LETTER

The third letter indicates the operating ambient temperature range. The letters A to G give information about the temperature:

A : temperature range not specified below (see note 4)
B : 0 to + 70 °C
C : −55 to +125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example : the range 0 to +75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

Version letter(s)

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack (2 leads)
G : for flat pack (4 leads)
H : for quadrature flat pack (QFP)
L : for chip on tape (foil)
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Pro electron type designation code for integrated circuits

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : cylindrical
D : dual-in-line (DIL)
E : power DIL (with external heatsink)
F : flat (leads on 2 sides)
G : flat (leads on 4 sides)
H : quadrature flat pack (QFP)
K : diamond (TO-3 family)
M : multiple-in-line (except dual-, triple-, quadruple-in-line)
Q : quadruple-in-line (QIL)
R : power QIL (with external heatsink)
S : single-in-line
T : triple-in-line
W : lead chip-carrier (LCC)
X : leadless chip-carrier (LLCC)
Y : pin grid array (PGA)

SECOND LETTER: Material

C : metal-ceramic
G : glass-ceramic (cerdip)
M : metal
P : plastic

To avoid confusion when the serial number ends with a letter, a hyphen is used preceding the suffix.

Examples (see note 5)

PCF1105WP : Digital IC, PC family, operational temperature range –40 to +85 °C, serial number 1105, plastic leaded chip-carrier.

GMB74LS00A-DC: Digital IC, GM family, operational temperature range 0 to +70 °C, company number 74LSS00A, ceramic DIL package.

TDA1000P : Analog circuit, no standard temperature range, serial number 1000, plastic DIL package.

SAC2000 : Solitary digital circuit, operational temperature range –55 to +125 °C.

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).

2. The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added (e.g. SH for Bubble-memories).

3. By 'slice processor' is meant: a functional slice of microprocessor.

4. In the case of two same types with two different temperature ranges not specified below, one type should use the letter 'A' as the third letter and the other, the letter 'X'.

5. Some companies have been using version letters and/or two letter-suffix, which differ from the Pro Electron definitions. In case of confusion Pro Electron may be contacted.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and D.C. lines.

DEVICE DATA

CA3089
FM IF System

Product Specification

DESCRIPTION

CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM IF system. The block diagram shows the CA3089 features, which include a three-stage FM IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The circuit design of the IF system includes desirable features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8V to +18V.

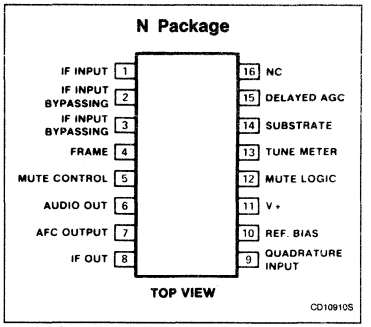
The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089 utilizes a 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40°C to +85°C.

FEATURES

- **Exceptional limiting sensitivity: 10μV typ. at −3dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**
- **Single-coil tuning capability**
- **High recovered audio: 400mV typ.**
- **Provides specific signal for control of interchannel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **Provides delayed AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible AFC**
- **Internal supply/voltage regulators**

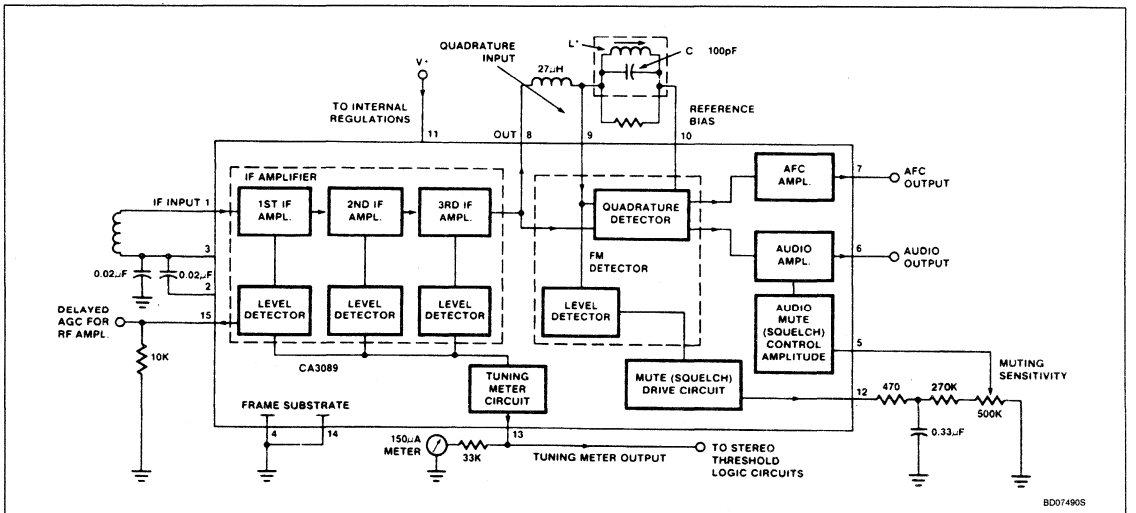
PIN CONFIGURATION



APPLICATIONS

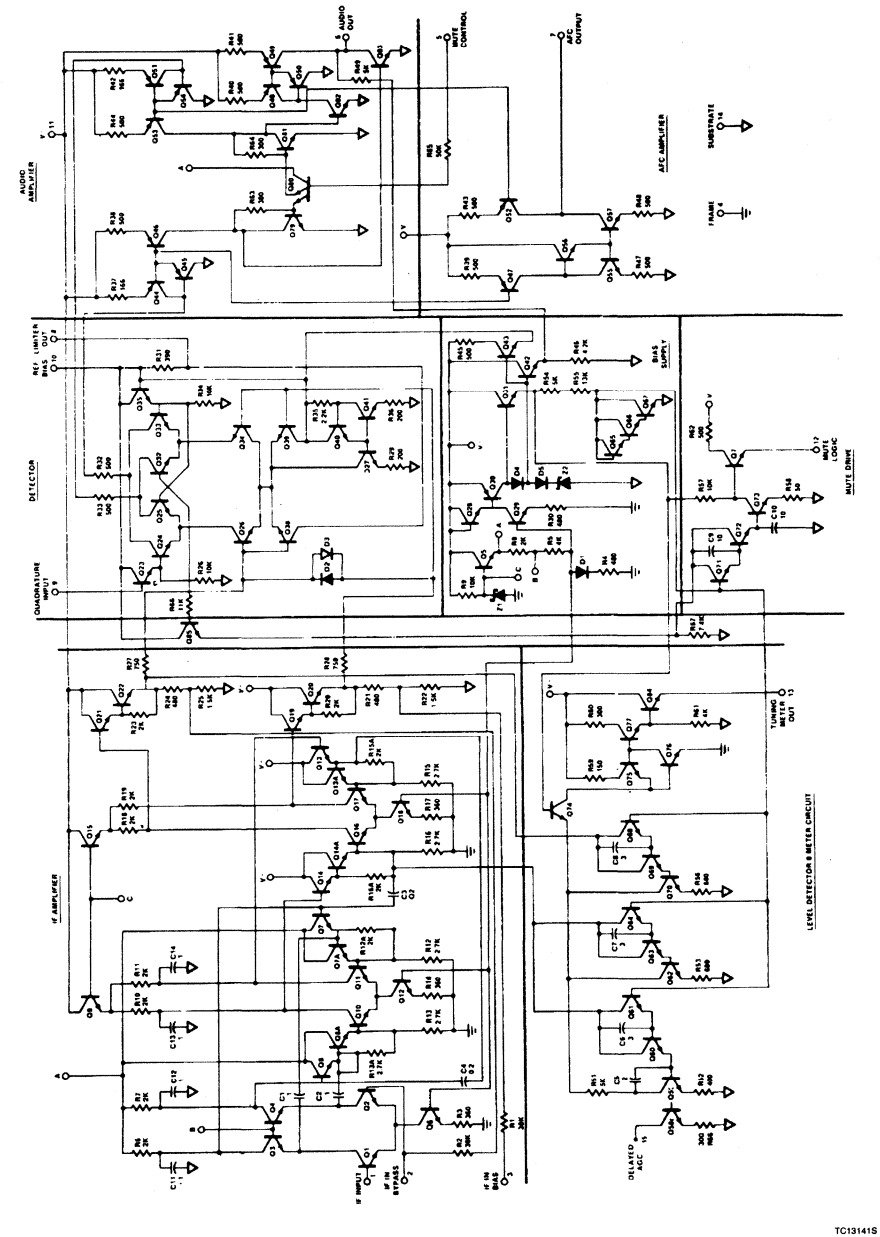
- **High-fidelity FM receivers**
- **Automotive FM receivers**
- **Communications FM receivers**

BLOCK DIAGRAM



NOTES:
1. All resistor values are typical and in ohms. $Q_O \simeq 75$ (G.I. EX27825 or equivalent)
2. L tunes with 100pF (C) at 10.7MHz

EQUIVALENT SCHEMATIC



NOTES:
1. All resistance values are typical and in ohms.
2. All capacitance values are in picofarads.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	−40°C to +85°C	CA3089N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	DC supply voltage: between terminals 11 and 4 between terminals 11 and 14	 18 18	 V V
	DC current (out of Terminal 15)	2	mA
P_D	Device dissipation: up to $T_A = 60°C$ above $T_A = 60°C$	 600 derate linearly 6.7	 mW mW/°C
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

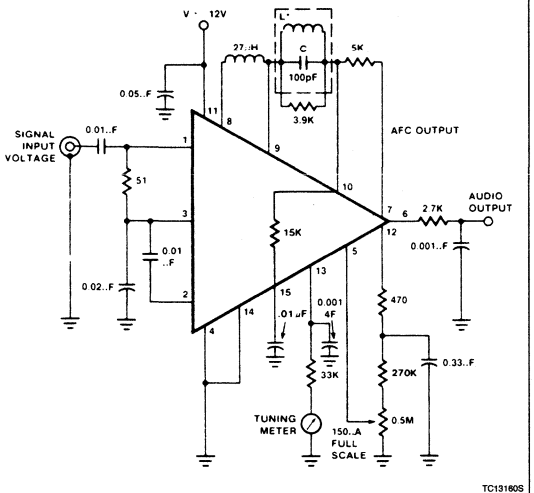
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V^+ = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Static (DC) Characteristics						
I_{11}	Quiescent circuit current	No signal input, non-muted	16	23	30	mA
DC Voltages[4]						
V_1	Terminal 1 (1F input)	No signal input, non-muted	1.2	1.9	2.4	V
V_2	Terminal 2 (AC return to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_3	Terminal 3 (DC bias to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_6	Terminal 6 (audio output)	No signal input, non-muted	5.0	5.6	6.0	V
V_7	Terminal 7 (AFC)	No signal input, non-muted	5.0	5.6	6.0	V
V_{10}	Terminal 10 (DC reference)	No signal input, non-muted	5.0	5.6	6.0	V
Dynamic Characteristics						
$V_{I(LIM)}$	Input limiting voltage (-3dB point)[3]			10	25	μV
	AMR AM rejection (Terminal 6)[4]	$V_{IN} = 0.1V$, $f_O = 10.7MHz$, $f_{MOD} = 400Hz$, AM Mod = 30%	45	55		dB
V_O	Recovered audio voltage (Terminal 6)[3]		400	500	600	mV
	Total harmonic distortion:[1]					
THD	Single tuned (Terminal 6)[3]			0.5	1.0	%
THD	Double tuned (Terminal 6)[4]	$f_{MOD} = 400Hz$, $V_{IN} = 0.1$		0.1		%
S + N/N	Signal plus noise-to-noise ratio (Terminal 6)[3]	Deviation = ± 75kHz, $V_{IN} = 0.1V$	60	70		dB
MU_{IN}	Mute input (Terminal 5)	$V_5 = 2.5V$	50	70		dB
MU_{OUT}	Mute output (Terminal 12)	$V_{IN} = 50\mu V$			0.5	V
		$V_{IN} = 0V$	4.0			V
MTR	Meter output (Terminal 13)	$V_{IN} = 0.1V$	2.5	3.5		V
		$V_{IN} = 500\mu V$	1.0	1.5		V
		$V_{IN} = 0V$			0.7	V
AGC	Delay AGC (Terminal 15)	$V_{IN} = 0.01V$			0.5	V
		$V_{IN} = 10\mu V$	4.0	5.0		V
THD	Double tuned (Terminal 6)[4]	$f_{MOD} = 400Hz$, $V_{IN} = 0.1$		0.1		%

NOTES

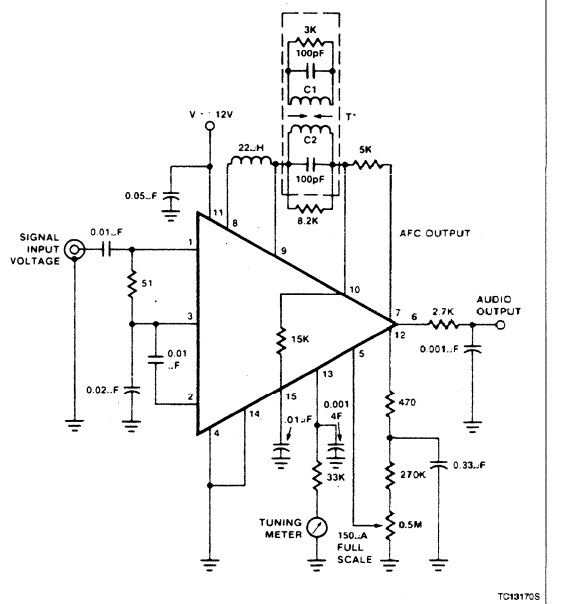
1. THD characteristics and audio level are essentially a function of the phase and Q characteristics of the network connected between Terminals 8, 9, and 10.
2. Test circuit Figure 1.
3. Test circuit Figure 2.
4. Test circuit Figures 1 and 2.

TEST CIRCUITS



NOTES:
1. L tunes with 100pF (C) at 10.7MHz.
2. All resistor values are typical and in ohms.
3. Q_O (unloaded) $\simeq$ 75 (G.I. automatic mfg. div. EX27825 or equivalent).

Figure 1. Test Circuit Using a Single-Tuned Detector Coil

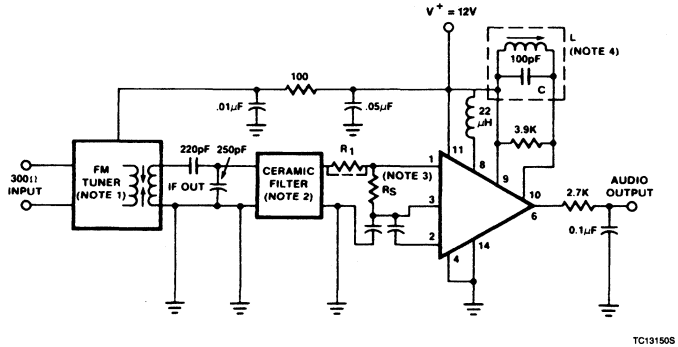


NOTES:
All resistor values are typical and in ohms.

T: Pri — Q_O (unloaded) $\simeq$ 75 (tunes with 100pF (C1) 20 † of 34a on 7/32' dia. form) Sec. – Q (unloaded) $\simeq$ 75 (tunes with 100pF (C2) 20 † of 34e on 7/32' dia. form)
kQ (percent of critical coupling) > 70%
(Adjusted for coil voltage V_C = 150mV)
Above values permit proper operation of mute (squelch) circuit 'E' type slugs, spacing 4mm

Figure 2. Test Circuit Using a Double-Tuned Detector Coil

TEST CIRCUITS



NOTES:
All resistor values are typical and in ohms.
1. Waller 4SN3FIC or equivalent.
2. Murate SFG 10.7mA or equivalent.
3. R_S will affect stability depending on circuit layout. To increase stability R_S is decreased. Range of R_S is 330 to 50Ω, $R_1 + R_S \leqslant 330\Omega$.
4. L tunes with 100pF (C) at 10.7MHz Q_O unloaded $\simeq$ 75 (G.I. EX27825 or equivalent).

Performance data at f_O = 98MHz, f_{MOD} = 400Hz, deviation = ±74kHz.

±74kHz.	
−3dB limiting sensitivity	2μV (antenna level)
20dB quieting sensitivity	1μV (antenna level)
30dB quieting sensitivity	1.5μV (antenna level)

Figure 3. Typical FM Tuner With a Single-Tuned Detector Coil

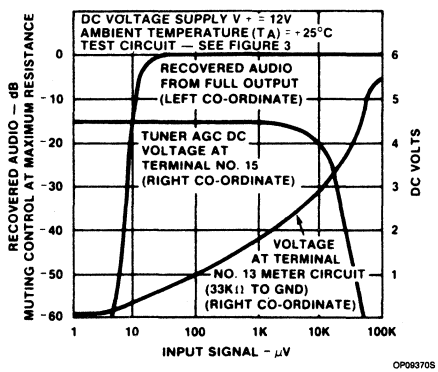
SYSTEM DESIGN CONSIDERATIONS

The CA3089 is a very high gain device and therefore careful consideration must be given to the layout of external components to minimize feedback. The input bypass capacitors should be located close to the input terminals and the values should not be large nor should the capacitors be of the type which might introduce inductive reactance to the circuit. An example of good bypass capacitors would be ceramic disc with values in the range of 0.01 to 0.05μF.

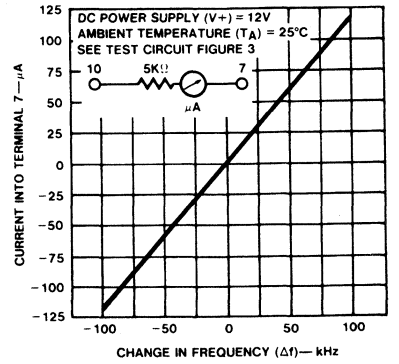
The input impedance of the CA3089 is approximately 10,000Ω. It is *not* recommended to match this impedance. The value of the input termination resistor should be as low as possible without degrading system operation. The lower the value of this resistor the greater the system stability. An input terminating resistor between 50Ω and 100Ω is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

Muting Action, Tuner AGC
(Tuning meter output as a function of input signal voltage.)



AFC Characteristics
(Current at Terminal 7 as a function of change in frequency.)



Philips Components

Data sheet	
status	Product specification
date of issue	June 1990

FCB61C65(L/LL)

8 K x 8 Fast CMOS low-power static RAM

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

FEATURES

- Operating supply voltage 5 V ± 10%
- Inputs and outputs ESD protected
- Automatic power-down after a completed read access
- Access time: 55 ns and 70 ns
- Low current consumption:
  - active 70 mA max.
  - standby (TTL) 3 mA max.
  - standby (CMOS) 100 µA max. (L-version)
  - standby (CMOS) 1 µA max. (LL-version)
- Suitable for battery back-up operation: (FCB61C65L/LL only)
  - data retention voltage 2 V min.
  - data retention current 50 µA max. (L-version)
  - data retention current 1 µA max. (LL-version)
- Latched data outputs giving stable data between consecutive accesses
- Easy memory expansion
- Common data I/O interface
- All inputs and outputs TTL and CMOS compatible
- All inputs have a Schmitt trigger switching action
- Three-state outputs
- Operating temperature 0 °C to +70 °C

GENERAL DESCRIPTION

The FCB61C65(L/LL) is a 65536-bit fast, low-power, static random access memory organized as 8192 words of 8 bits each.

The chip enable inputs $\overline{CE}1$ and CE2 are available for memory expansion and to control the low-power/ standby mode.

The device operates from a 5 V power supply and has an access time of 55 ns and 70 ns.

The FCB61C65(L/LL) is ideally suited for memory applications where fast access time, low power and ease of use are required.

The FCB61C65(L/LL) is a CMOS device which uses a 6 transistor memory cell.

The IC is fabricated in a CMOS double-metal single-poly process using ion-implanted silicon gate technology.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
FCB61C65 (L/LL)-XXP	28	DIL (600 mil)	plastic	SOT117
FCB61C65 (L/LL)-XXT	28	SO28XL (330 mil)	plastic	SOT213

8 K x 8 Fast CMOS low-power static RAM FCB61C65(L/LL)

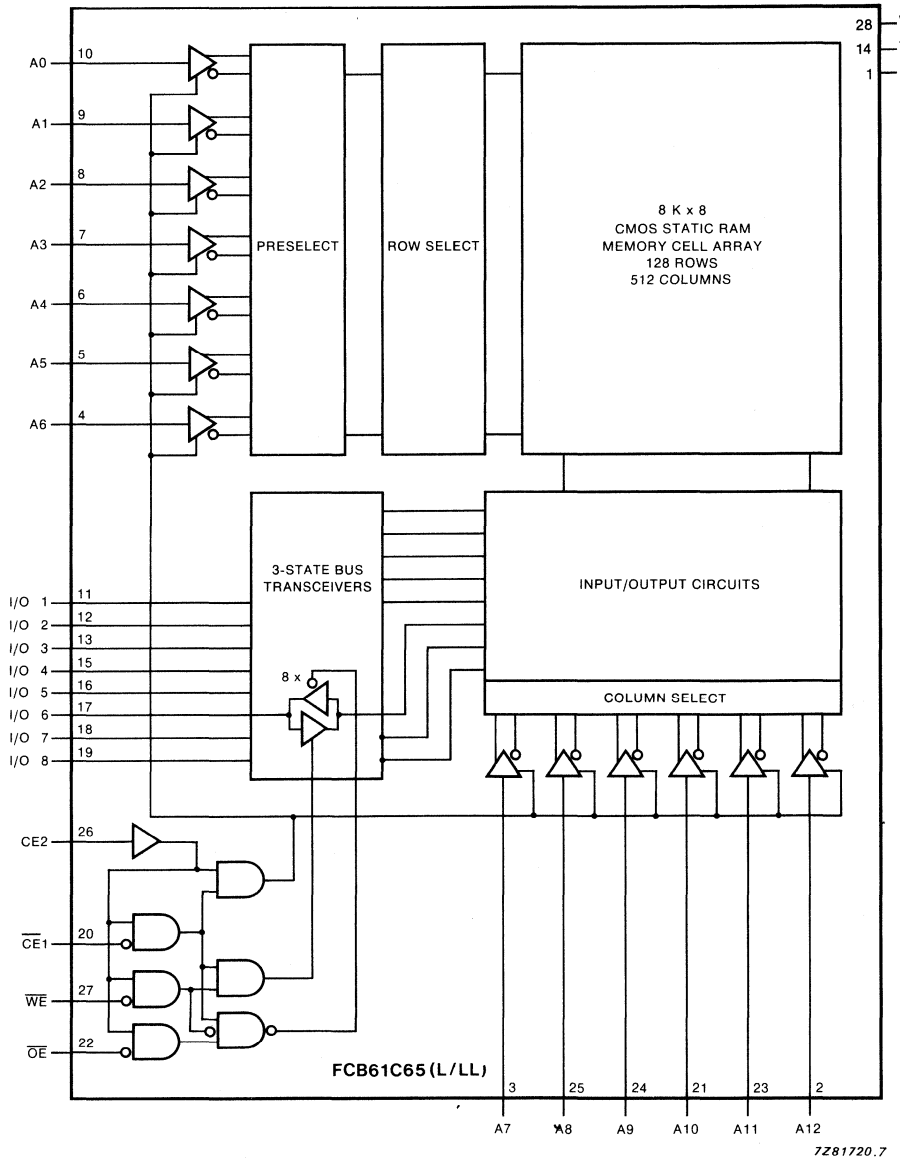


Fig.1 Block diagram.

8 K x 8 Fast CMOS low-power static RAM FCB61C65(L/LL)

TRUTH TABLE

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	I_{DD}	I/O PIN	REF. CYCLE
H	X	X	X	not selected	I_{SB}*	HIGH Z	
X	L	X	X	not selected	I_{SB}*	HIGH Z	
L	H	L	H	read	I_{DD}/I_{DD1}*	D OUT	read
L	H	H	L	write	I_{DD}	D IN	write
L	H	L	L	write	I_{DD}	D IN	write
L	H	H	H	ready-read	I_{DD}/I_{DD1}*	HIGH Z	

* Including L/LL versions if input levels are CMOS.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
A12	2	address input
A7 to A0	3 to 10	address inputs
I/O 1 to I/O 3	11 to 13	data inputs/outputs
V_{SS}	14	ground
I/O 4 to I/O 8	15 to 19	data inputs/outputs
$\overline{CE1}$	20	chip enable 1
A10	21	address input
$\overline{OE}$	22	output enable
A11, A9, A8	23 to 25	address inputs
CE2	26	chip enable 2
$\overline{WE}$	27	write enable
V_{DD}	28	+5 V supply

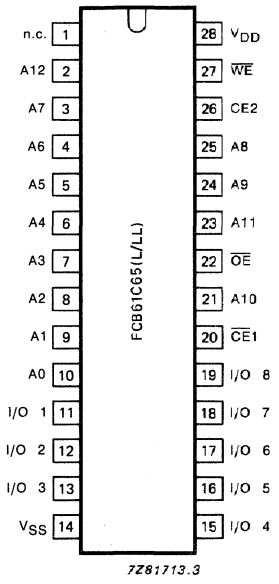


Fig.2 Pinning diagram.

DC CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C. Typical readings taken at V_{DD} = 5 V; T_{amb} = 25 °C. All voltages are referenced to V_{SS} (0 V) unless otherwise specified. DC characteristics are valid after thermal equilibrium has been established.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	input leakage current	$V_I = V_{SS}$ to V_{DD}	−1	-	1	µA
I_{LO}	output leakage current	$\overline{CE1}$ or $\overline{OE}$ = V_{IH} or CE2 = V_{IL}; $V_{I/O} = V_{SS}$ to V_{DD}	−1	-	1	µA
I_{DD}	average operating current	cycle time 55 ns; 100% duty factor; note 1 $I_{I/O}$ = 0 mA	-	40	70	mA
I_{DD}	average operating current	cycle time 70 ns; 100% duty factor; note 1 $I_{I/O}$ = 0 mA	-	35	60	mA
I_{DD1}	DC operating current	$\overline{WE}$ = V_{IH}; $I_{I/O}$ = 0 mA; f = 0 Hz	-	3	6	mA
		$\overline{WE}$ = CMOSH; V_I = CMOS; note 2				
I_{DDL}	FCB61C65L only		-	2	100	µA
I_{DDLL}	FCB61C65LL only		-	0.05	1.0	µA
I_{SB}	standby current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}	-	1.5	3.0	mA
		$\overline{CE1}$ = CMOSH and CE2 = CMOS or CE2 = CMOSL				
I_{SBL}	FCB61C65L only		-	2	100	µA
I_{SBLL}	FCB61C65LL only		-	0.05	1.0	µA
V_{OL}	output voltage LOW	I_{OL} = 4 mA	-	-	0.4	V
V_{OL}	output voltage LOW	I_{OL} = 20 µA	-	-	0.2	V
V_{OH}	output voltage HIGH	I_{OH} = −1 mA	2.4	-	-	V
V_{OH}	output voltage HIGH	I_{OH} = −20 µA	V_{DD}−0.2	-	-	V

Notes to the DC characteristics

1. $I_{DD} \leq 50$ mA at a cycle time of 100 ns and ≤ 45 mA at a cycle time of 120 ns.

2. CMOS = CMOSH: $V_{DD} - 0.2\ V \leq$ level $\leq V_{DD} + 0.2\ V$ or
   CMOSL: $-0.2\ V \leq$ level $\leq +0.2\ V$.

CAPACITANCES

f = 1 MHz; T_{amb} = 25 °C (parameters in this table are sampled and not 100% tested).

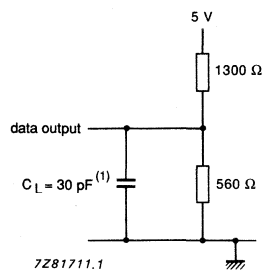
SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
	input capacitance			
C_I	$\overline{CE1}$, CE2, $\overline{WE}$, $\overline{OE}$	V_I = 0 V	8	pF
C_I	all other inputs	V_I = 0 V	7	pF
$C_{I/O}$	input/output capacitance	$V_{I/O}$ = 0 V	8	pF

TIMING CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; inputs pulse levels = 0.4 to 2.4 V; input rise and fall times = 5 ns; input and output timing reference levels = 1.5 V and output loading as in Figure 3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	55 TYPE		70 TYPE		UNIT
			MIN.	MAX.	MIN.	MAX.	
Read cycle							
t_{RC}	read cycle time		55	-	70	-	ns
t_{AA}	address access time		-	55	-	70	ns
t_{ACE}	chip enable access time		-	55	-	70	ns
t_{OE}	output enable access time		-	30	-	35	ns
t_{CLZ}	chip enable to output LOW Z	note 6	5	-	5	-	ns
t_{OLZ}	output enable to output LOW Z	note 6	5	-	5	-	ns
t_{CHZ}	chip disable to output HIGH Z	note 6	-	30	-	30	ns
t_{OHZ}	output disable to output HIGH Z	note 6	-	30	-	30	ns
t_{OH}	output hold time		10	-	10	-	ns
Write cycle							
t_{WC}	write cycle time		55	-	70	-	ns
t_{CW}	chip enable to end of write	note 11	50	-	65	-	ns
t_{AW}	address valid to end of write		50	-	65	-	ns
t_{AS}	address set up time		0	-	0	-	ns
t_{WP}	write pulse width	note 9	30	-	35	-	ns
t_{WR}	write recovery time	note 10	0	-	0	-	ns
t_{WHZ}	write enable to output HIGH Z	note 16	-	20	-	25	ns
t_{DW}	data to write time overlap		25	-	30	-	ns
t_{DH}	data hold from write time		5	-	5	-	ns
t_{OW}	end of write to output LOW Z	note 16	5	-	5	-	ns

Output load



(1) C_L = 5 pF for t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{OLZ}, t_{OHZ} and t_{OW}.

Fig.3 Output load.

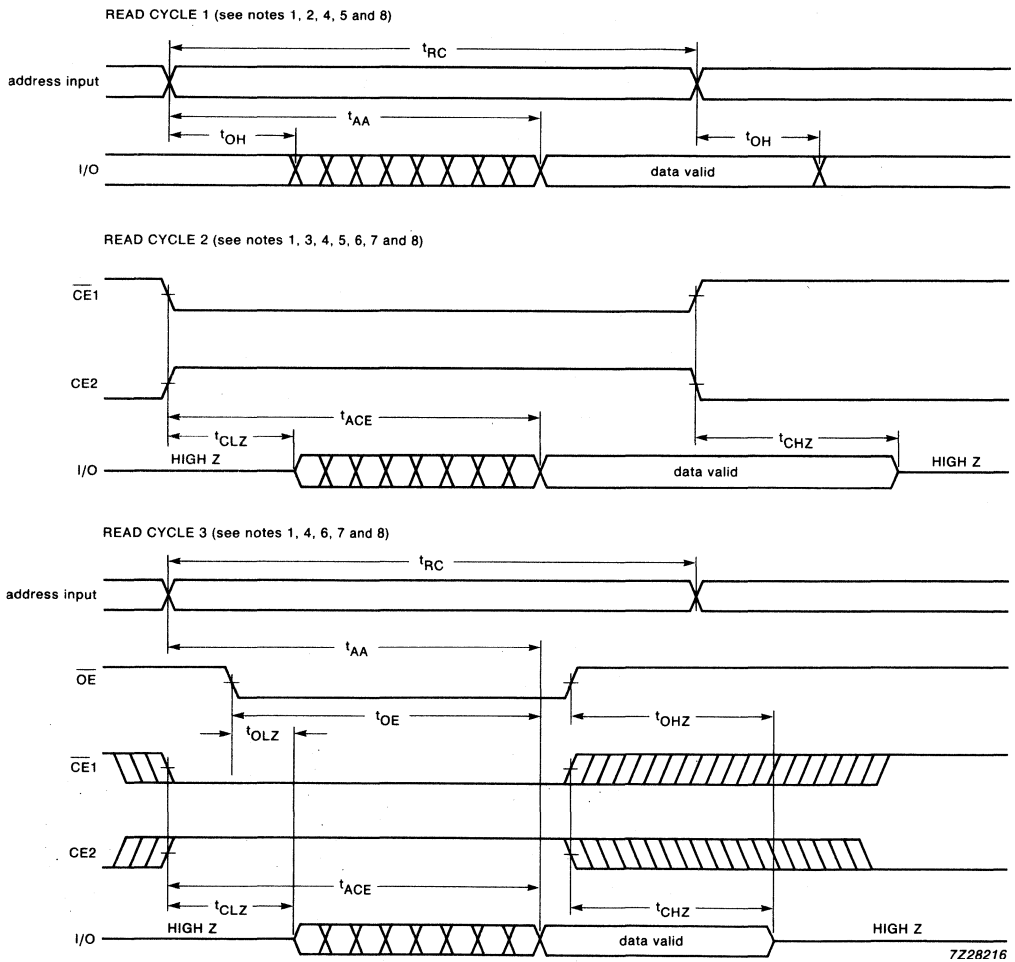


Fig.4 Read cycle timing.

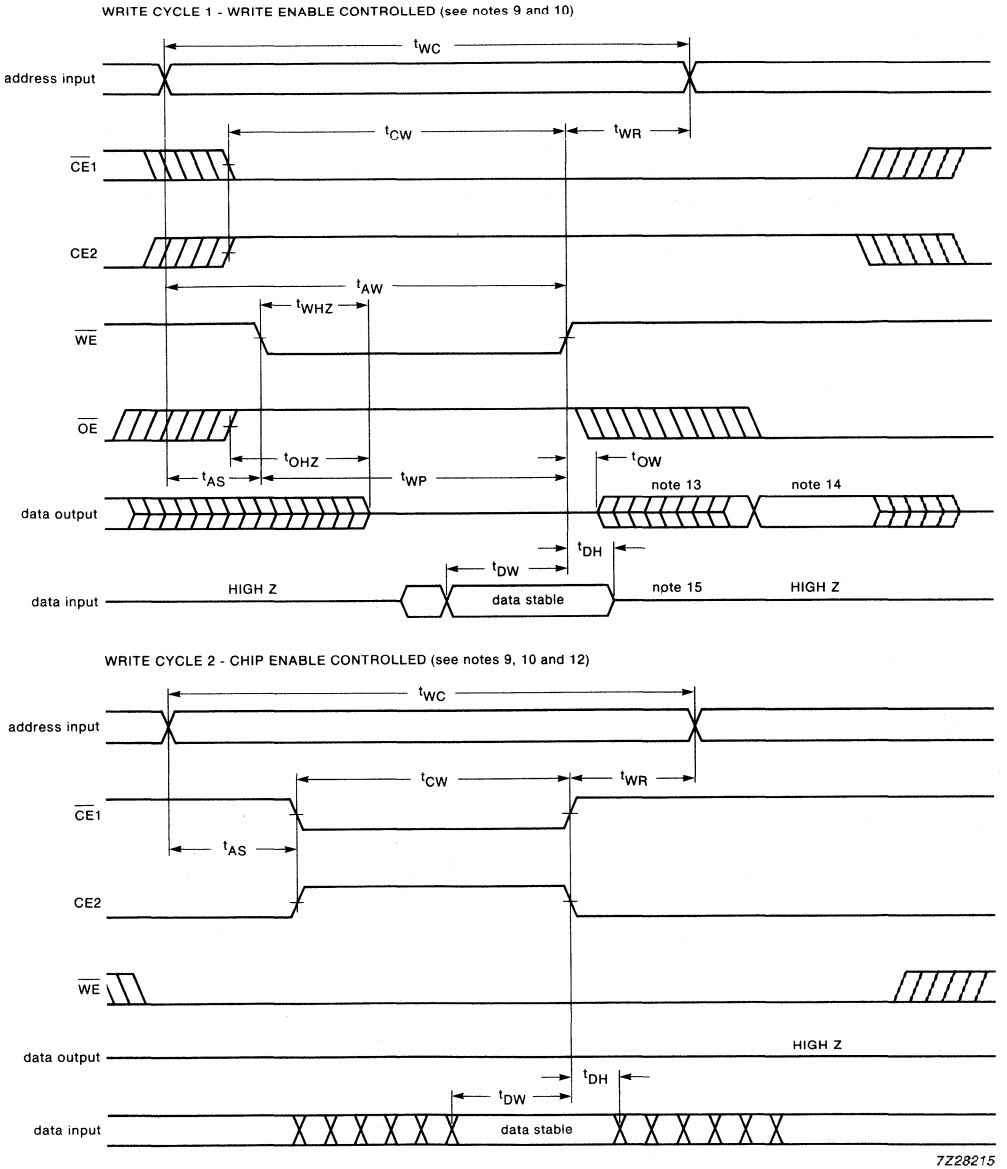


Fig.5 Write cycle timing.

Notes to the timing characteristics

Read cycle (see Fig.4)

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CE}1$ is LOW and CE2 is HIGH.
3. Address is valid prior to or coincident with $\overline{CE}1$ LOW or CE2 HIGH transition.
4. When $\overline{CE}1$ is LOW and CE2 HIGH, the address inputs may not be floating.
5. $\overline{OE}$ is LOW.
6. C_L = 5 pF for t_{CLZ}, t_{CHZ}, t_{OLZ}, output transition measured at ± 200 mV from preceding steady state. These parameters are sampled and not 100% tested.
7. t_{CLZ} and t_{ACE} are measured from the last $\overline{CE}1$ going LOW or CE2 going HIGH. t_{CHZ} is measured from the first of $\overline{CE}1$ going HIGH or CE2 going LOW.
8. If D OUT in two consecutive read cycles is the same, D OUT remains stable.

Write cycle (see Fig.5)

9. A write occurs during an overlap of LOW $\overline{CE}1$, a HIGH CE2 and a LOW $\overline{WE}$.
10. t_{WR} is measured from the earlier of CE2 going to LOW or $\overline{CE1}$ or $\overline{WE}$ going HIGH at the end of a write cycle.
11. If the $\overline{CE}1$/CE2 transition occurs simultaneously to or after the $\overline{WE}$ LOW transition the outputs remain in a high impedance state.
12. $\overline{OE}$ is continuously LOW.
13. D OUT is in the same phase as the write data of this write cycle.
14. D OUT is the read data of the next address.
15. If $\overline{CE}1$ is LOW (CE2 is HIGH) and I/O pins are in the output state during this period then input data signals of opposite phase to the outputs must not be applied.
16. C_L = 5 pF for t_{WHZ} and t_{OW}, measured at ± 200 mV from steady state. These parameters are sampled and not 100% tested.

DATA RETENTION CHARACTERISTICS FOR LOW POWER/STANDBY MODE

(FCB61C65L/LL only)

T_{amb} = 0 to +70 °C; $I_{DRL/LL}$ measurements are valid after thermal equilibrium has been established.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DR}	supply voltage for data retention	$\overline{CE1}$ = CMOSH or CE2 = CMOSL with other V_I = CMOS; note 1	2.0	-	5.5	V
	supply current during data retention	V_{DR} = 3 V; CE2 = CMOSL; other V_I = CMOS or $\overline{CE1}$ = CMOSH; other V_I = CMOS				
I_{DRL}	FCB61C65L only		-	2	50	µA
I_{DRLL}	FCB61C65LL only		-	0.05	1	µA
Timing						
t_{CDR}	chip disable to data retention time		0	-	-	ns
t_R	recovery time to fully active	note 2	t_{RC}	-	-	ns

Notes to the data retention characteristics

1. CMOS = CMOSH: $V_{DR} - 0.2\ V \leq$ level $\leq V_{DR} + 0.2\ V$ or
   CMOSL: $-0.2\ V \leq$ level $\leq +0.2\ V$.

2. t_{RC} = read cycle time.

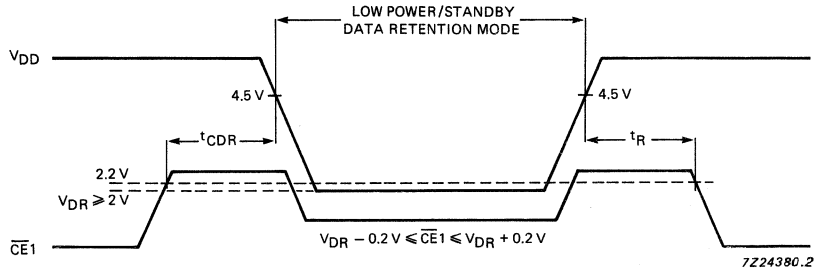


Fig.6 Data retention waveform ($\overline{CE1}$ controlled).

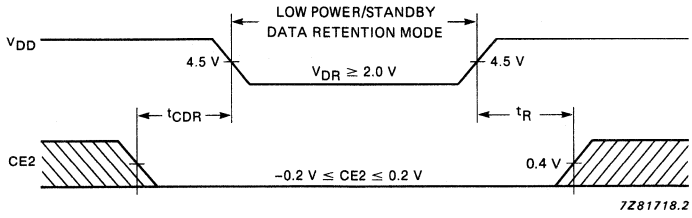


Fig.7 Data retention waveform (CE2 controlled).

Philips Components

Data sheet	
status	Product specification
date of issue	August 1990

FCF61C65(L/LL)

8 K x 8 Fast CMOS low-power static RAM for extended temperature range

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

FEATURES

- Operating supply voltage 5 V ± 10%
- Inputs and outputs ESD protected
- Automatic power-down after a completed read access
- Access time: 85 ns
- Low current consumption:
  - active 60 mA max.
  - standby (TTL) 3 mA max.
  - standby (CMOS) 200 µA max. (L-version)
  - standby (CMOS) 4 µA max. (LL-version)
- Suitable for battery back-up operation: (FCF61C65L/LL only)
  - data retention voltage 2 V min.
  - data retention current 100 µA max. (L-version)
  - data retention current 4 µA max. (LL-version)
- Latched data outputs giving stable data between consecutive accesses
- Easy memory expansion
- Common data I/O interface
- All input and outputs TTL and CMOS compatible
- All inputs have a Schmitt trigger switching action
- Three-state outputs
- Operating temperature –40 °C to +85 °C

GENERAL DESCRIPTION

The FCF61C65(L/LL) is a 65536-bit, fast, low-power, static random access memory organized as 8192 words of 8 bits each.

The chip enable inputs $\overline{CE}1$ and CE2 are available for memory expansion and to control the lower-power/ standby mode.

The device operates from a 5 V power supply and has an access time of 85 ns.

The FCF61C65(L/LL) is ideally suited for memory applications for the extended temperature range of –40 to +85°C where fast access time, low power and ease of use are required.

The FCF61C65(L/LL) is a full CMOS device using a 6 transistor memory cell.

The IC is fabricated in a CMOS double-metal single-poly process using ion-implanted silicon gate technology.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
FCF61C65 (L/LL)-85T	28	SO28XL(330mil)	plastic	SOT213

8 K x 8 Fast CMOS low-power static RAM for extended temperature range

FCF61C65(L/LL)

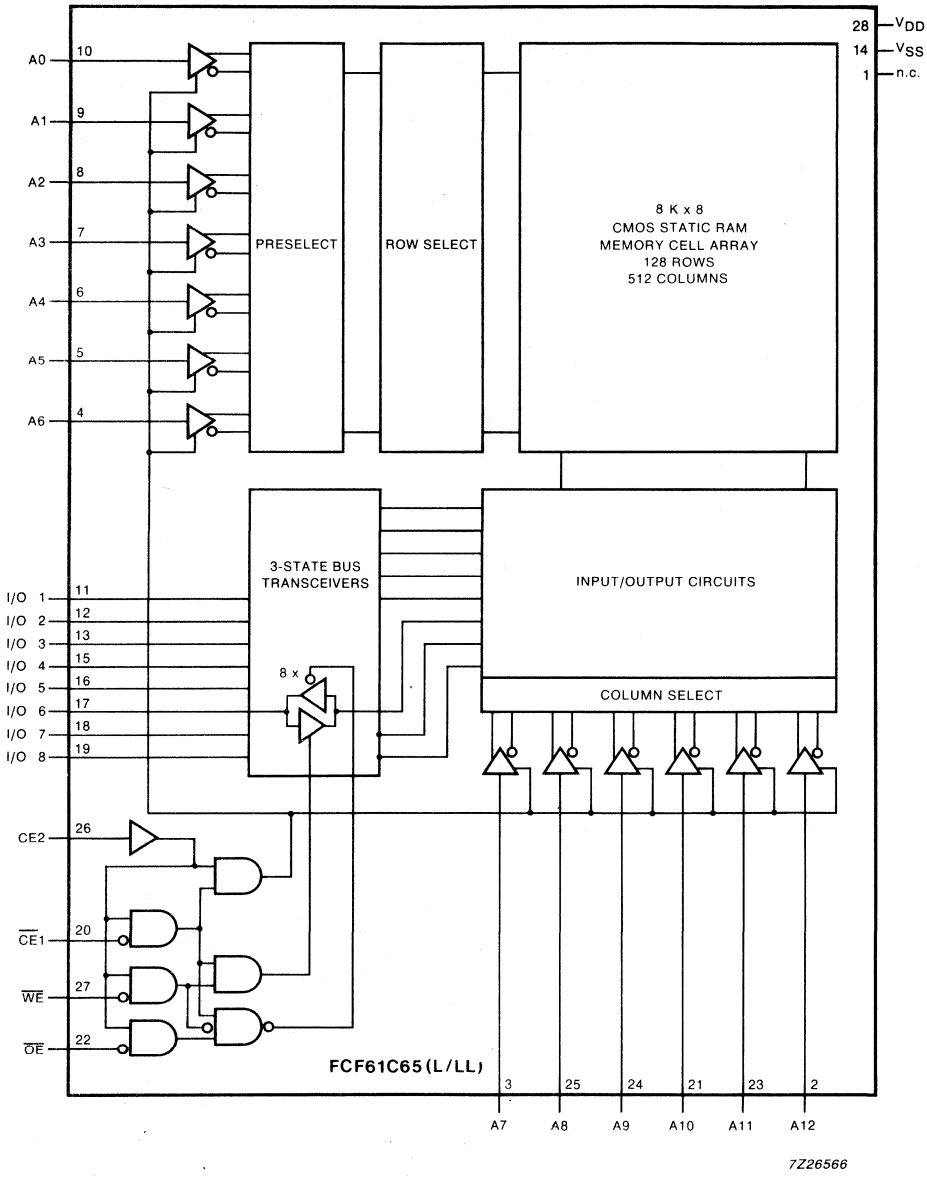


Fig.1 Block diagram.

8 K x 8 Fast CMOS low-power static RAM for extended temperature range

FCF61C65(L/LL)

TRUTH TABLE

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	I_{DD}	I/O PIN	REF. CYCLE
H	X	X	X	not selected	I_{SB}*	HIGH Z	
X	L	X	X	not selected	I_{SB}*	HIGH Z	
L	H	L	H	read	I_{DD}/I_{DD1}*	D OUT	read
L	H	H	L	write	I_{DD}	D IN	write
L	H	L	L	write	I_{DD}	D IN	write
L	H	H	H	ready-read	I_{DD}/I_{DD1}*	HIGH Z	

* Including L/LL versions if input levels are CMOS.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
A12	2	address input
A7 to A0	3 to 10	address inputs
I/O 1 to I/O 3	11 to 13	data inputs/outputs
V_{SS}	14	ground
I/O 4 to I/O 8	15 to 19	data inputs/outputs
$\overline{CE1}$	20	chip enable 1
A10	21	address input
$\overline{OE}$	22	output enable
A11, A9, A8	23 to 25	address inputs
CE2	26	chip enable 2
$\overline{WE}$	27	write enable
V_{DD}	28	+5 V supply

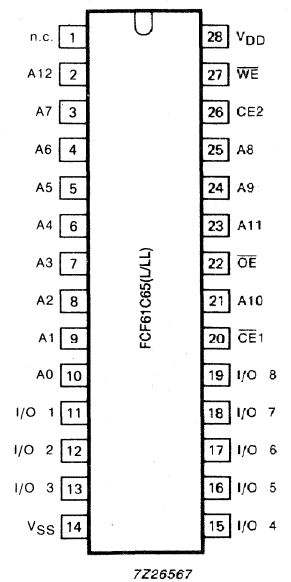


Fig.2 Pinning diagram.

DC CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −40 to +85 °C. Typical readings taken at V_{DD} = 5 V; T_{amb} = 25 °C. All voltages are referenced to V_{SS} (0 V) unless otherwise specified. DC characteristics are valid after thermal equilibrium has been established.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	input leakage current	$V_I = V_{SS}$ to V_{DD}	−2	-	2	µA
I_{LO}	output leakage current	$\overline{CE1}$ or $\overline{OE}$ = V_{IH} or CE2 = V_{IL}; $V_{I/O} = V_{SS}$ to V_{DD}	−2	-	2	µA
I_{DD}	average operating current	cycle time 85 ns; 100% duty factor; note 1 $I_{I/O}$ = 0 mA	-	35	60	mA
I_{DD1}	DC operating current	$\overline{WE}$ = V_{IH}; $I_{I/O}$ = 0 mA; f = 0 Hz	-	3	10	mA
		$\overline{WE}$ = CMOSH; V_I = CMOS; notes 2 and 3				
I_{DDL}	FCF61C65L only		-	2	200	µA
I_{DDLL}	FCF61C65LL only		-	0.05	4	µA
I_{SB}	standby current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}	-	1.5	3.0	mA
		$\overline{CE1}$ = CMOSH and CE2 = CMOS or CE2 = CMOSL; notes 2 and 3				
I_{SBL}	FCF61C65L only			2	200	µA
I_{SBLL}	FCF61C65LL only		-	0.05	4	µA
V_{OL}	output voltage LOW	I_{OL} = 4 mA	-	-	0.4	V
V_{OL}	output voltage LOW	I_{OL} = 20 µA	-	-	0.2	V
V_{OH}	output voltage HIGH	I_{OH} = −1 mA	2.4	-	-	V
V_{OH}	output voltage HIGH	I_{OH} = −20 µA	V_{DD}−0.2	-	-	V

Notes to the DC characteristics

1. I_{DD} ≤ 55 mA at a cycle time of 100 ns and ≤ 50 mA at a cycle time of 120 ns.

2. CMOS = CMOSH: V_{DD} − 0.2 V ≤ level ≤ V_{DD} + 0.2 V or
   CMOSL: −0.2 V ≤ level ≤ +0.2 V.

3. At T_{amb} = 70 °C: I_{SBL}/I_{DDL} ≤ 100 µA max. and
   I_{SBLL}/I_{DDLL} ≤ 1 µA max.

CAPACITANCES

f = 1 MHz; T_{amb} = 25 °C (parameters in this table are sampled and not 100% tested).

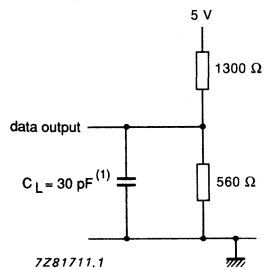
SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
	input capacitance			
C_I	$\overline{CE1}$, CE2, $\overline{WE}$, $\overline{OE}$	V_I = 0 V	8	pF
C_I	all other inputs	V_I = 0 V	7	pF
$C_{I/O}$	input/output capacitance	$V_{I/O}$ = 0 V	8	pF

TIMING CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −40 to +85 °C; inputs levels = 0.4 to 2.4 V, input rise and fall times = 5 ns; input and output timing reference levels = 1.5 V and output loading as in Figure 3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Read cycle					
t_{RC}	read cycle time		85	-	ns
t_{AA}	address access time		-	85	ns
t_{ACE}	chip enable access time		-	85	ns
t_{OE}	output enable access time		-	40	ns
t_{CLZ}	chip enable to output LOW Z	note 6	5	-	ns
t_{OLZ}	output enable to output LOW Z	note 6	5	-	ns
t_{CHZ}	chip disable to output HIGH Z	note 6	-	35	ns
t_{OHZ}	output disable to output HIGH Z	note 6	-	35	ns
t_{OH}	output hold time		10	-	ns
Write cycle					
t_{WC}	write cycle time		85	-	ns
t_{CW}	chip enable to end of write	note 11	70	-	ns
t_{AW}	address valid to end of write		70	-	ns
t_{AS}	address set-up time		0	-	ns
t_{WP}	write pulse width	note 9	40	-	ns
t_{WR}	write recovery time	note 10	5	-	ns
t_{WHZ}	write enable to output HIGH Z	note 16	-	35	ns
t_{DW}	data to write time overlap		35	-	ns
t_{DH}	data hold from write time		5	-	ns
t_{OW}	end of write to output LOW Z	note 16	5	-	ns

Output load



(1) C_L = 5 pF for t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{OLZ}, t_{OHZ} and t_{OW}.

Fig.3 Output load.

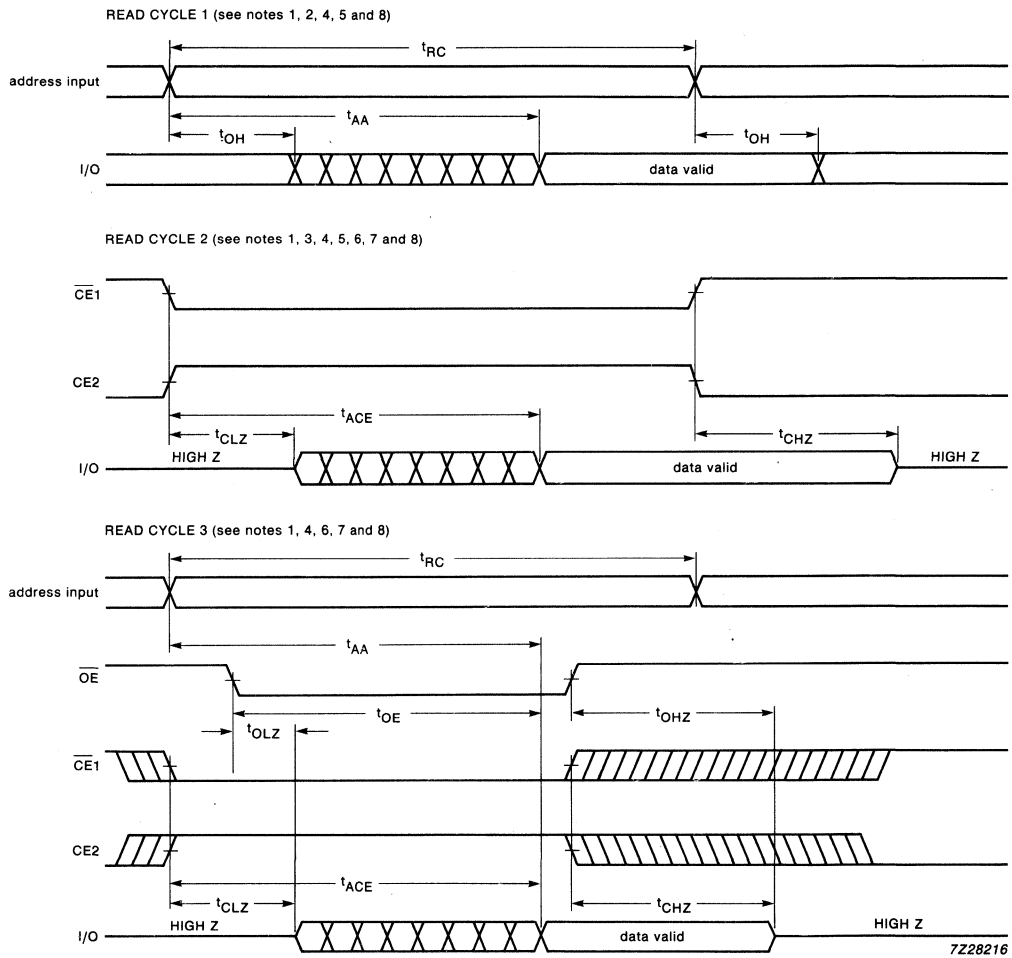


Fig.4 Read cycle timing.

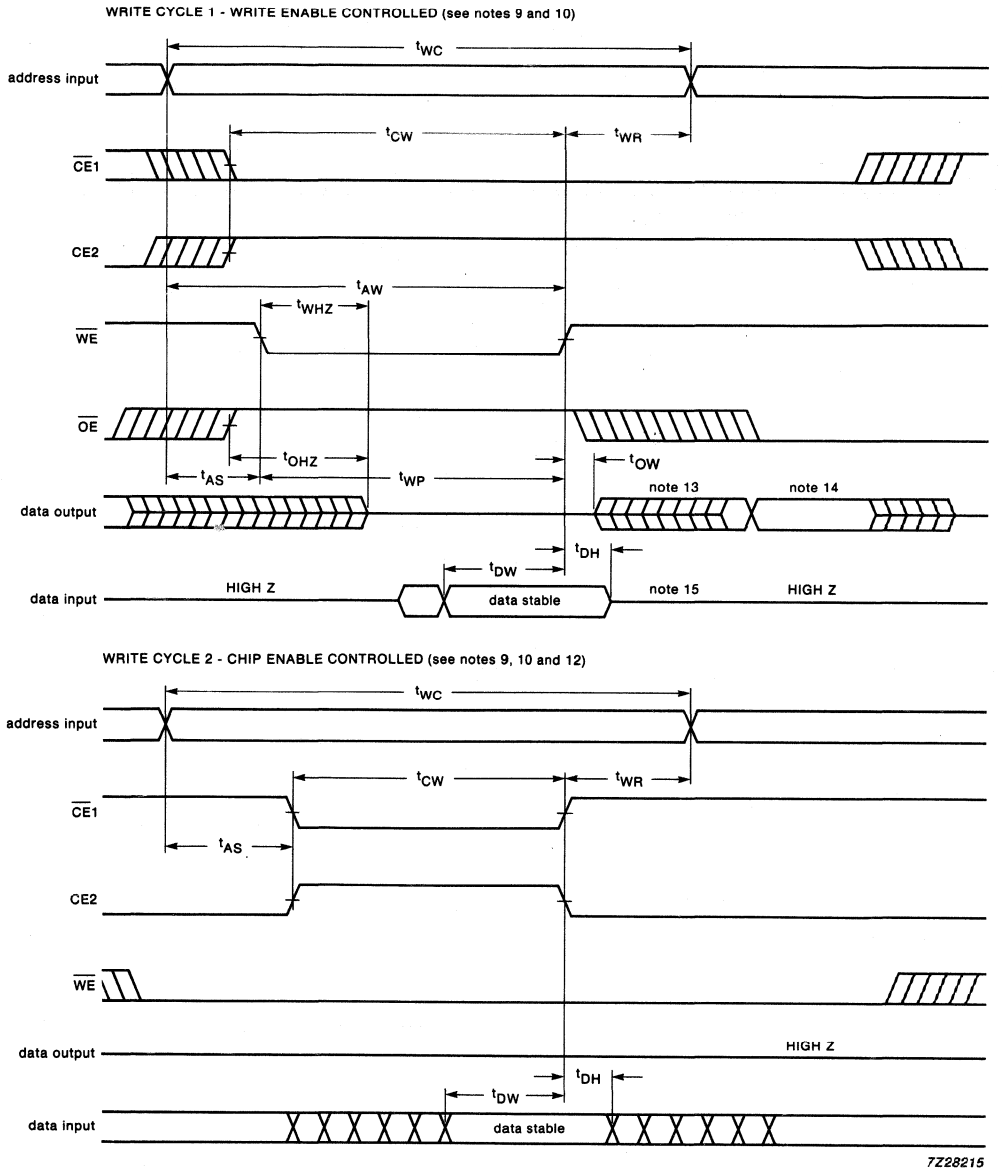


Fig.5 Write cycle timing.

Notes to the timing characteristics

Read cycle (see Fig.4)

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CE}1$ is LOW and CE2 is HIGH.
3. Address is valid prior to or coincident with $\overline{CE}1$ LOW or CE2 HIGH transition.
4. When $\overline{CE}1$ is LOW and CE2 HIGH, the address inputs may not be floating.
5. $\overline{OE}$ is LOW.
6. C_L = 5 pF for t_{CLZ}, t_{CHZ}, t_{OLZ}, output transition measured at ± 200 mV from preceding steady state. These parameters are sampled and not 100% tested.
7. t_{CLZ} and t_{ACE} are measured from the last $\overline{CE}1$ going LOW or CE2 going HIGH. t_{CHZ} is measured from the first of $\overline{CE}1$ going HIGH or CE2 going LOW.
8. If D OUT in two consecutive read cycles is the same, D OUT remains stable.

Write cycle (see Fig.5)

9. A write occurs during an overlap of LOW $\overline{CE}1$, a HIGH CE2 and a LOW $\overline{WE}$.
10. t_{WR} is measured from the earlier of CE2 going to LOW or $\overline{CE}1$ or $\overline{WE}$ going HIGH at the end of a write cycle.
11. If the $\overline{CE}1$/CE2 transition occurs simultaneously to or after the $\overline{WE}$ LOW transition the outputs remain in a high impedance state.
12. $\overline{OE}$ is continuously LOW.
13. D OUT is in the same phase as the write data of this write cycle.
14. D OUT is the read data of the next address.
15. If $\overline{CE}1$ is LOW (CE2 is HIGH) and I/O pins are in the output state during this period then input data signals of opposite phase to the outputs must not be applied.
16. C_L = 5 pF for t_{WHZ} and t_{OW}, measured at ± 200 mV from steady state. These parameters are sampled and not 100% tested.

8 K x 8 Fast CMOS low-power static RAM for extended temperature range

FCF61C65(L/LL)

DATA RETENTION CHARACTERISTICS FOR LOW POWER/STANDBY MODE

(FCF61C65L/LL only)

T_{amb} = −40 to +85 °C; $I_{DRL/LL}$ measurements are valid after thermal equilibrium has been established.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DR}	supply voltage for data retention	$\overline{CE1}$ = CMOSH or CE2 = CMOSL with other V_I = CMOS; note 1	2.0	-	5.5	V
	supply current during data retention	V_{DR} = 3 V; $\overline{CE2}$ = CMOSL; other V_I = CMOS or $\overline{CE1}$ = CMOSH; other V_I = CMOS				
I_{DRL}	FCF61C65L only	note 2	-	2	100	µA
I_{DRLL}	FCF61C65LL only	note 2	-	0.05	4	µA
Timing						
t_{CDR}	chip disable to data retention time		0	-	-	ns
t_R	recovery time to fully active	note 3	t_{RC}	-	-	ns

Notes to the data retention characteristics

1. CMOS = CMOSH: $V_{DR} - 0.2\ V \leq level \leq V_{DR} + 0.2\ V$ or
   CMOSL: $-0.2\ V \leq level \leq +0.2\ V$.

2. At T_{amb} = 70 °C: $I_{DRL} \leq 50\ \mu A$ and $I_{DRLL} \leq 1\ \mu A$.

3. t_{RC} = read cycle time.

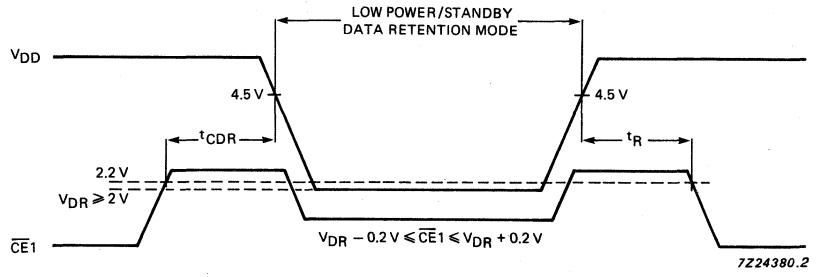


Fig.6 Data retention waveform ($\overline{CE1}$ controlled).

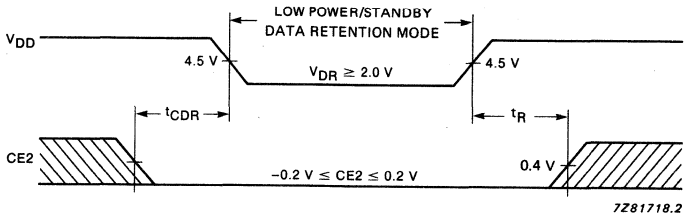


Fig.7 Data retention waveform (CE2 controlled).

MC3361
Low Power FM IF

Objective Specification

Linear Products

DESCRIPTION

The MC3361 is a monolithic low-power FM IF signal processing system consisting of an oscillator, mixer, limiting amplifier, quadrature detector, filter amplifier, squelch, scan control and mute switch. It is intended for use in narrow band FM dual conversion communications equipment. The MC3361 is available in a 16-lead, dual-in-line plastic package and 16-lead SO (surface-mounted miniature package).

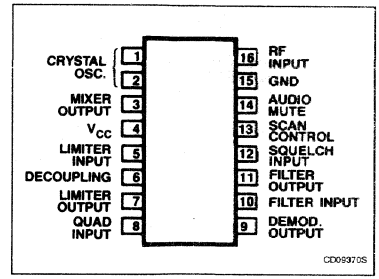
FEATURES

- **2.0V to 8.0V operation**
- **Low current: 4.2mA typ at V_{CC} = 4.0V_{DC}**
- **Excellent sensitivity: 2.0μV for −3dB limiting typ**
- **Low external parts count**
- **Operation to 60MHz**

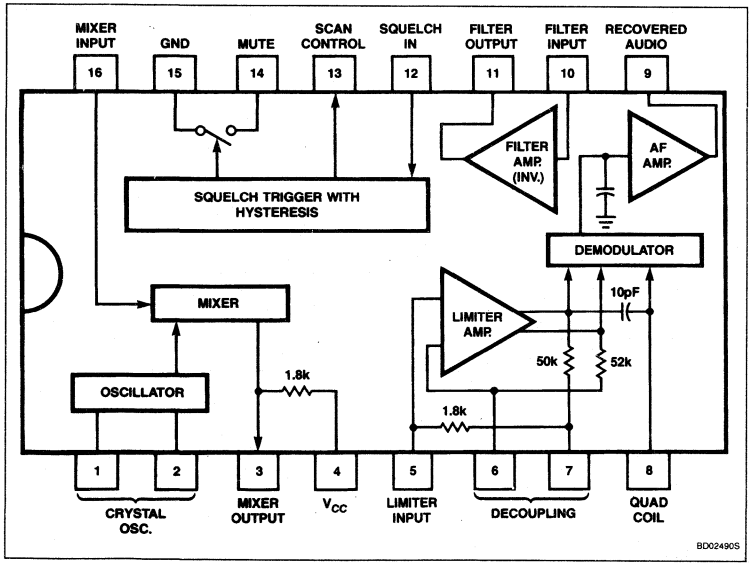
APPLICATIONS

- **Cordless telephone**
- **Narrow band receivers**
- **Remote control**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	MC3361N
16-Pin Plastic; SO (surface-mounted miniature package)	0 to +70°C	MC3361D

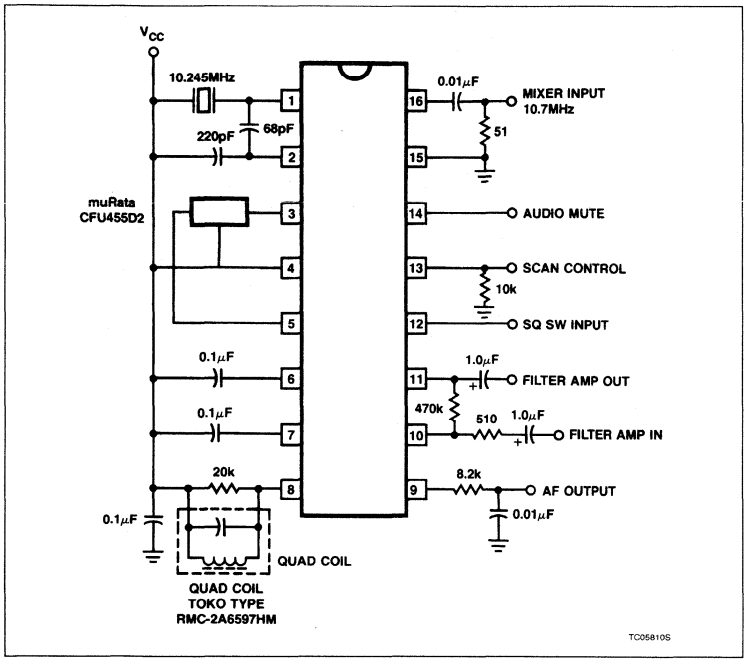
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

SYMBOL	PARAMETER	PIN	RATING	UNIT
V_{CC} (Max)	Power supply voltage	4	10	V_{DC}
V_{CC}	Generating supply voltage range	4	2.0 to 8.0	V_{DC}
	Detector input voltage	8	1.0	V_{P-P}
V_{16}	Input voltage (V_{CC}≥4.0V)	16	1.0	V_{RMS}
V_{14}	Mute function	14	−0.5 to 5.0	V_{PK}
T_J	Junction temperature		150	°C
T_A	Operating ambient temperature range		−30 to +75	°C
T_{STG}	Storage temperature range		−65 to +150	°C

AC AND DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0V_{DC}, f_O = 10.7MHz, Δf = ±3.0kHz, f_{MOD} = 1.0kHz, T_A = 25°C unless otherwise noted.)

PARAMETER	PIN	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Drain current (no signal) squelch off squelch on	4			 4.2 5.4	 7.0 9.0	mA
Input limiting voltage	16	−3.0dB limiting		2.0	6.0	μV
Detector output voltage	9			2.0		V_{DC}
Detector output impedance				450		Ω
Recovered audio output voltage	9	V_{IN} = 10mV_{RMS}	100	150	270	mV_{RMS}
Filter gain (10kHz)		V_{IN} = 1.0mV_{RMS}	40	46		dB
Filter output voltage	11			1.7		V_{DC}
Trigger hysteresis				50		mV
Mute function low	14			10		Ω
Mute function high	14			10		MΩ
Scan function low (mute off)	13	V_{12} = 1.0V_{DC}			0.5	V_{DC}
Scan function high (mute on)	13	V_{12} = GND	3.5			V_{DC}
Mixer conversion gain	3			27		dB
Mixer input resistance	16			3.6		kΩ
Mixer input capacitance	16			2.2		pF

TEST CIRCUIT



NE542
Dual Low-Noise Preamplifier

Product Specification

DESCRIPTION

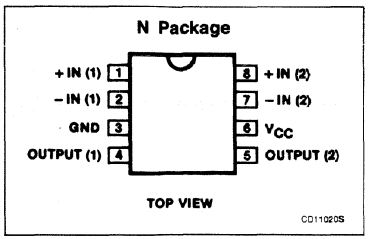
The NE542 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 110dB supply rejection and 70dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing (V_{CC}–$2V_{P-P}$), and internal compensation to 10dB. The NE542 operates from a single supply across a range of 9 to 24V.

The NE542 is ideal for use in stereo phono, tape, or microphone preamps and other applications requiring low noise amplification of small signals.

FEATURES

- **Low noise — 0.7μV total input noise**
- **High gain — 104dB open-loop**
- **Single supply operation**
- **Wide supply range 9 to 24V**
- **Power supply rejection 110dB**
- **Large output voltage swing (V_{CC}–$2V_{P-P}$)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 100kHz ($15V_{P-P}$)**
- **Internally-compensated (stable at 10dB)**
- **Short-circuit protected**
- **High slew rate 5V/μs**

PIN CONFIGURATION



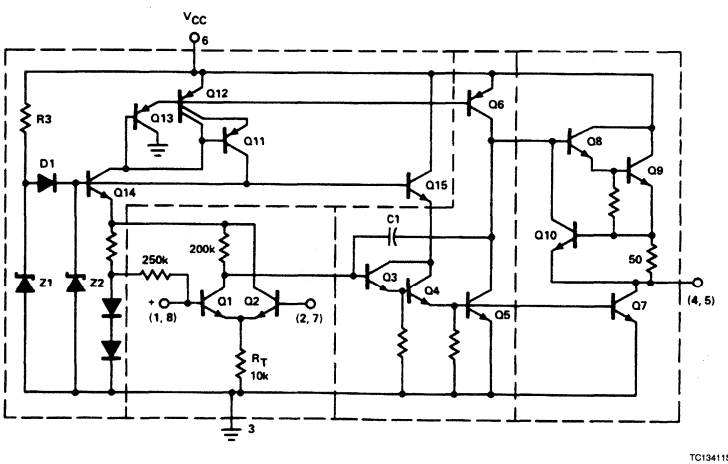
APPLICATIONS

- **Tape preamplifier**
- **Phono preamplifier**
- **Microphone preamplifier**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE542N

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+24	V
P_D	Power dissipation	500	mW
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	= dc

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 14V$, unless otherwise specified.

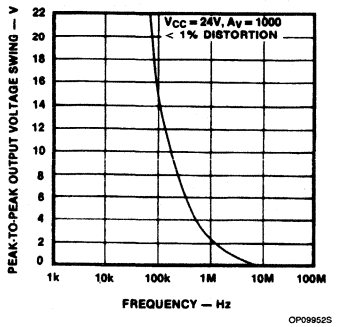
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		9		24	V
I_{CC}	Supply current	$V_{CC} = 9$ to 18V, $R_L = \infty$		9	15	mA
R_{IN}	Input resistance Positive input Negative input			 100 200		 kΩ kΩ
R_{OUT}	Output resistance	Open-loop		150		Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 14V$, unless otherwise specified.

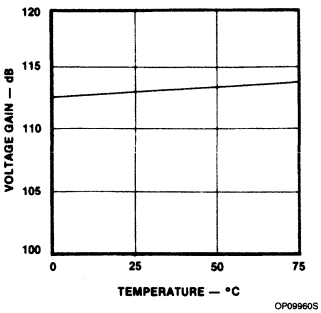
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
A_V	Voltage gain	Open-loop		160,000		V/V
I_{IN}	Negative Input current				0.5	
I_{OUT}	Output current	Source Sink (linear operation)	8 2	14 3		mA mA
V_{OUT}	Output voltage swing		V_{CC} −2.5	V_{CC} −2		V
SR	Small signal bandwidth Slew rate			15 5		MHz V/μs
P_{BW}	Power bandwidth	$15V_{P-P}$		100		kHz
V_{IN}	Maximum input voltage	Linear operation, < 2.5% distortion			300	mV_{RMS}
PSRR	Power supply rejection ratio	f = 60, 120Hz f = 1kHz		100 110		dB dB
	Channel separation	f = 1kHz	40	70		dB
THD	Total harmonic distortion	40dB gain, f = 1kHz		0.1	0.3	%
	Total equivalent input noise	$R_S = 600Ω$, 100 – 10,000Hz		0.7	1.2	$μV_{RMS}$
	Noise figure	$R_S = 50kΩ$, 10 – 10,000Hz $R_S = 20kΩ$, 10 – 10,000Hz $R_S = 10kΩ$, 10 – 10,000Hz $R_S = 5kΩ$, 10 – 10,000Hz		1.2 1.2 1.5 2.4		dB dB dB dB

TYPICAL PERFORMANCE CHARACTERISTICS

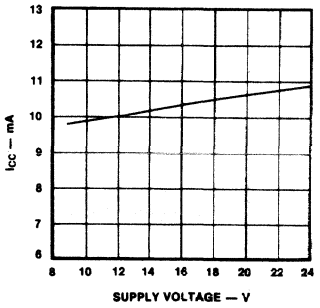
Large-Signal Frequency Response



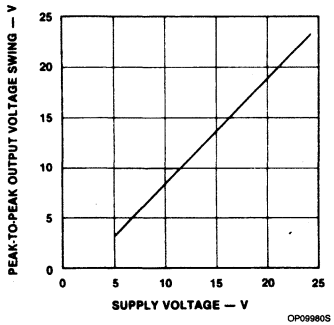
Gain vs Temperature



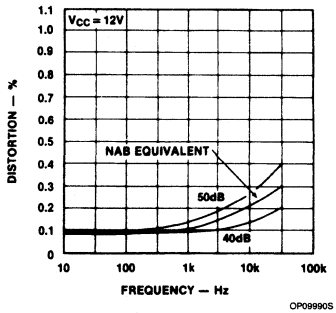
VCC vs ICC



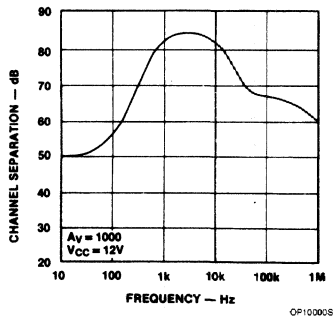
Peak-to-Peak Output Voltage Swing vs VCC



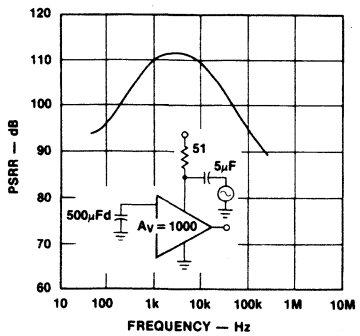
% Distortion



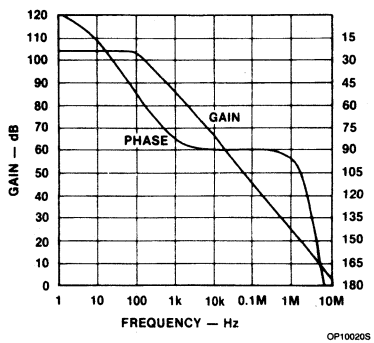
Channel Separation



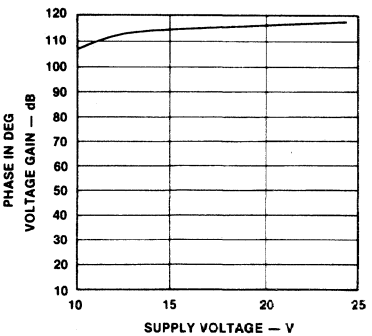
PSRR vs Frequency



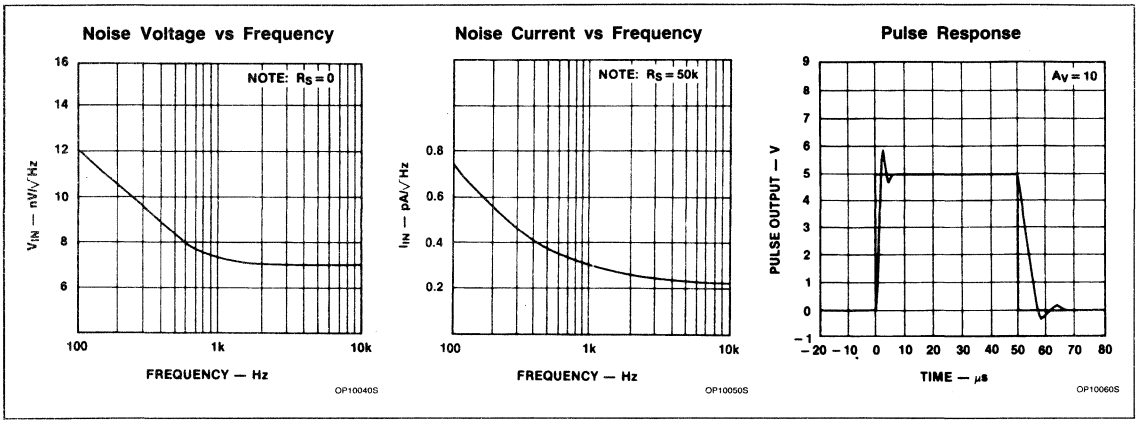
Gain and Phase Response



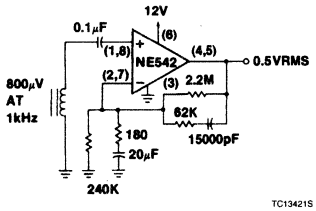
Voltage Gain vs Supply Voltage



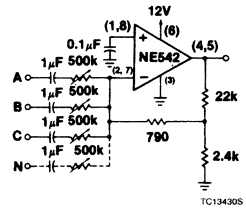
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



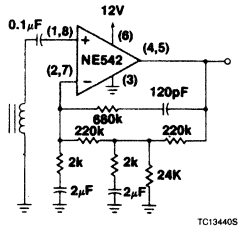
TYPICAL APPLICATIONS



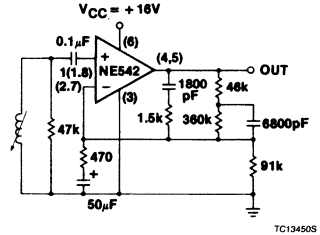
Typical Tape Playback Amplifier



Audio Mixer



Two-Pole Fast Turn-On NAB Tape Preamp



RIAA Magnetic Phono Preamp

NOTE:
All resistor values are typical and in ohms.

Document	853–0908
ECN No.	93801
Date of Issue	July 8, 1988
Status	Product Specification
Application Specific Product	

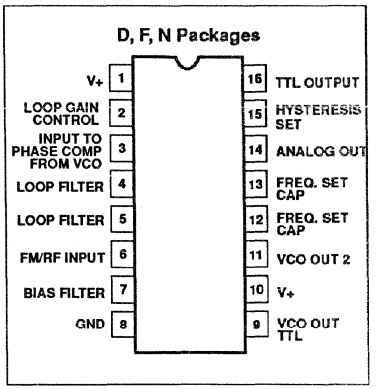
NE/SE564
Phase–locked loop

DESCRIPTION
The NE/SE564 is a versatile, high guaranteed frequency phase–locked loop designed for operation up to 50MHz. As shown in the Block Diagram, the NE/SE564 consists of a VCO, limiter, phase comparator, and post detection processor.

FEATURES
- Operation with single 5V supply
- TTL–compatible inputs and outputs
- Guaranteed operation to 50MHz
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications
- Can be used as a modulator
- Variable loop gain (externally controlled)

APPLICATIONS
- High speed modems
- FSK receivers and transmitters
- Frequency Synthesizers
- Signal generators
- Various satcom/TV systems

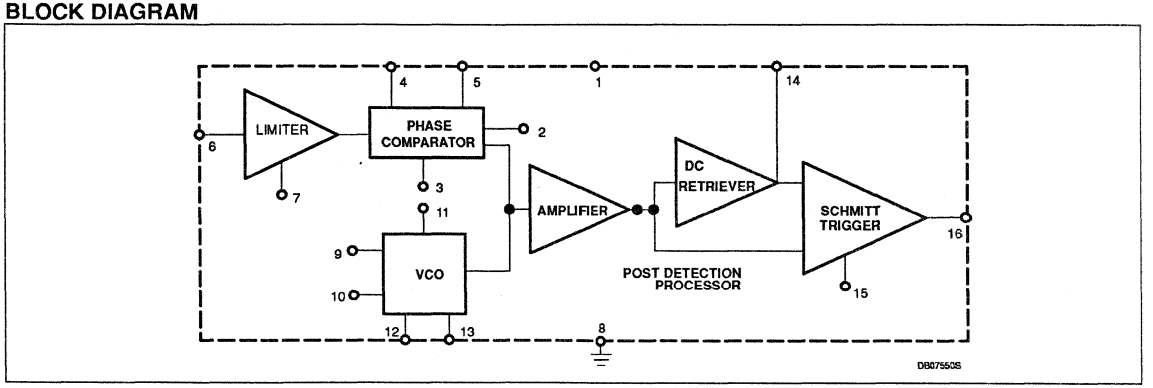
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16–Pin Plastic SO	0 to +70°C	NE564D
16–Pin Plastic DIP	0 to +70°C	NE564N
16–Pin Plastic DIP	–55 to +125°C	SE564N
16–Pin Cerdip	–55 to +125°C	SE564F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V+	Supply voltage Pin 1 Pin 10	 14 6	 V V
I_{OUT}	(Sink) Max (Pin 9)	10	mA
P_D	Power dissipation	600	mW
T_A	Operating ambient temperature NE SE	 0 to +70 –55 to +125	 °C °C
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
Operation above 5V will require heatsinking of the case.

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V; T_A = 0 to 70°C; f_O = 5MHz, I_2 = 400µA; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SE564			LIMITS NE564			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Maximum VCO frequency	C_1 = 0 (stray)	45	60		45	60		MHz
	Lock range	Input ≥ 200mV_{RMS} T_A = 25°C T_A = 125°C T_A = –55°C T_A = 0°C T_A = 70°C	 40 20 50	 70 30 80		 40	 70 70 40		% of f_O
	Capture range	Input ≥ 200mV_{RMS}, R_2 = 27Ω	20	30		20	30		% of f_O
	VCO frequency drift with temperature	f_O = 5MHz, T_A = –55°C to +125°C T_A = 0 to +70°C = 0 to +70°C f_O = 5MHz, T_A = –55°C to +125°C T_A = 0 to +70°C		 500 300	 1500 800		 600 500		PPM/°C
	VCO free–running frequency	C_1 = 91pF R_C = 100Ω "Internal"	4	5	6	3.5	5	6.5	MHz
	VCO frequency change with supply voltage	V_{CC} = 4.5V to 5.5V		3	8		3	8	% of f_O
	Demodulated output voltage	Modulation frequency: 1kHz f_O = 5MHz, input deviation: 2%T = 25°C 1%T = 25°C 1%T = 0°C 1%T = –55°C 1%T = 70°C 1%T = 125°C	 16 8 6 12	 28 14 10 16		 16 8	 28 14 13 15		 mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS}
	Distortion	Deviation: 1% to 8%		1			1		%
S/N	Signal–to–noise ratio	Std. condition, 1% to 10% dev.		40			40		dB
	AM rejection	Std. condition, 30% AM		35			35		dB
	Demodulated output at operating voltage	Modulation frequency: 1kHz f_O = 5MHz, input deviation: 1% V_{CC} = 4.5V V_{CC} = 5.5V	 7 8	 12 14		 7 8	 12 14		 mV_{RMS} mV_{RMS}

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SE564			LIMITS NE564			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_{CC} = 5V I_1, I_{10}		45	60		45	60	mA
	Output "1" output leakage current "0" output voltage	V_{OUT} = 5V, Pins 16, 9 I_{OUT} = 2mA, Pins 16, 9 I_{OUT} = 6mA, Pins 16, 9		1 0.3 0.4	20 0.6 0.8		1 0.3 0.4	20 0.6 0.8	μA V V

FUNCTIONAL DESCRIPTION (Figure 1)

The NE564 is a monolithic phase–locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz.

In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{IN} - f_O)}{K_{VCO}} \quad (1)$$

K_{VCO} = conversion gain of the VCO
f_{IN} = frequency of the input signal
f_O = free–running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{IN} from f_O. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at Pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free–running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the DC levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrowband signals where the deviation in f_{IN} itself may be less than the change in f_O due to temperature. This effect can be eliminated if the DC or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the DC levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high–frequency performance, an emitter–coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q21 and Q23 with current sources Q25 – Q26 form the basic oscillator. The approximate free–running frequency of the oscillator is shown in the following equation:

$$f_O \cong \frac{1}{22\,R_C\,(C_1 + C_S)} \quad (2)$$

$R_C = R_{19} = R_{20} = 100\Omega$ (INTERNAL)
C_1 = external frequency setting capacitor
C_S = stray capacitance

Variation of V_D (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase detection processor consists of a doubled–balanced modulator with a limiter amplifier to improve AM rejection. Schottky–clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at Pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a DC retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the DC retriever is formed by the transconductance amplifier Q_{42} – Q_{43} together with an external capacitor which is connected at the amplifier output (Pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_M}{C_2} \int V_{IN} dt \quad (3)$$

g_M = transconductance of the amplifier
C_2 = capacitor at the output (Pin 14)
V_{IN} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the DC or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of Q_{49} – Q_{50} with positive feedback being provided by Q_{47} – Q_{48}. The hysteresis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a DC control, provides symmetric variation around the nominal value.

Design Formula

The free–running frequency of the VCO is shown by the following equation:

$$f_O \cong \frac{1}{22\,R_C\,(C_1 + C_S)} \quad (4)$$

$R_C = 100\Omega$
C_1 = external cap in farads
C_S = stray capacitance

The loop filter diagram shown is explained by the following equation:

$$f_S = \frac{1}{1 + sRC_3} \text{ (First Order)} \quad (5)$$

$R = R_{12} = R_{13} = 1.3k\Omega$ (Internal)*

By adding capacitors to Pins 4 and 5, a pole is added to the loop transfer at

$$\omega = \frac{1}{RC_3}$$

NOTE:
*Refer to Figure 1.

APPLICATIONS

FM Demodulator

The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in Figures 2 and 3, respectively. The

input signal is AC coupled with the output signal being extracted at Pin 14. Loop filtering is provided by the capacitors at Pins 4 and 5 with additional filtering being provided by the capacitor at Pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be 1% or higher.

Modulation Techniques

The NE564 phase–locked loop can be modulated at either the loop filter ports (Pins 4 and 5) or the input port (Pin 6) as shown in Figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in Figure 5. This curve will be appropriate for signals injected into Pins 4 and 5 as shown in Figure 4.

FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5V power supply. Demodulated DC voltages associated with the mark and space frequencies are recovered with a single external capacitor in a DC retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high–frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 5 shows a high–frequency FSK decoder designed for input frequency deviations of ±1.0MHz centered around a free–running frequency of 10.8MHz. the value of the timing capacitance required was estimated from Figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_O' 10.8MHz.

The lock range graph indicates that the +1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero Pin 2 bias current. (While strictly this figure is appropriate only for 50MHz, it can be used as a guide for lock range estimates at other f_O' frequencies).

The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in Figure 7 for 20k, 500k, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators' output voltages with respect to each other and to the FSK output. The high–frequency sum components of the input and VCO frequency also are viable as noise on the phase comparator's outputs.

OUTLINE OF SETUP PROCEDURE

1. Determine operating frequency of the VCO:
   IF+ N in feedback loop, then
   $f_O = N \times f_{IN}$.
2. Calculate value of the VCO frequency set capacitor:
   $$C_O \cong \frac{1}{2200\, f_O}$$
3. Set I_2 (current sinking into Pin 2) for ≅ 100μA. After operation is obtained, this value may be adjusted for best dynamic behavior.
4. Check VCO output frequency with digital counter at Pin 9 of device (loop open, VCO to ϕ det.). Adjust C_O trim or frequency adj. Pins 4 – 5 for exact center frequency, if needed.
5. Close loop and inject input signal to Pin 6. Monitor Pins 3 and 6 with two–channel scope. Lock should occur with $\Delta\phi_{3-6}$ equal to 90° (phase error).
6. If pulsed burst or ramp frequency is used for input signal, special loop filter design may be required in place of simple single capacitor filter on Pins 4 and 5. (See PLL application section)
7. The input signal to Pin 6 and the VCO feedback signal to Pin 3 must have a duty cycle of 50% for proper operation of the phase detector. Due to the nature of a balanced mixer if signals are not 50% in duty cycle, DC offsets will occur in the loop which tend to create an artificial or biased VCO.
8. For multiplier circuits where phase jitter is a problem, loop filter capacitors may be increased to a value of 10 – 50μF on Pins 4, 5. Also, careful supply decoupling may be necessary. This includes the counter chain V_{CC} lines.

Phase–locked loop | NE/SE564

EQUIVALENT SCHEMATIC

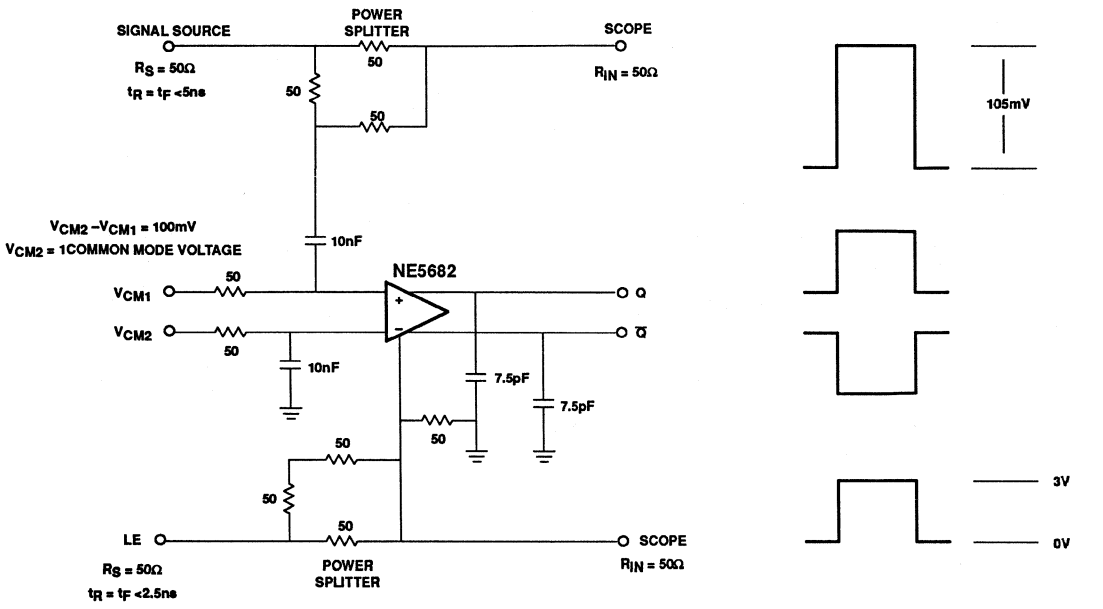


Figure 1. Test Circuit for AC Parameters

Phase–locked loop | NE/SE564

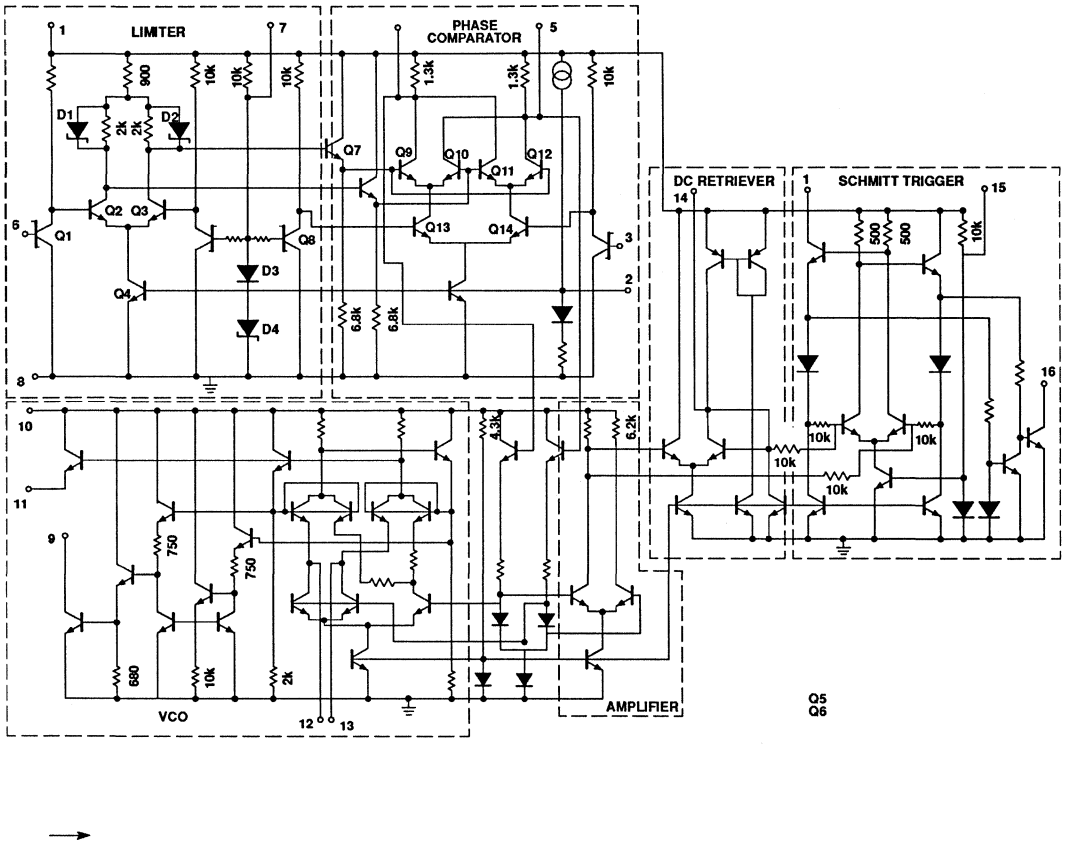


Figure 1.

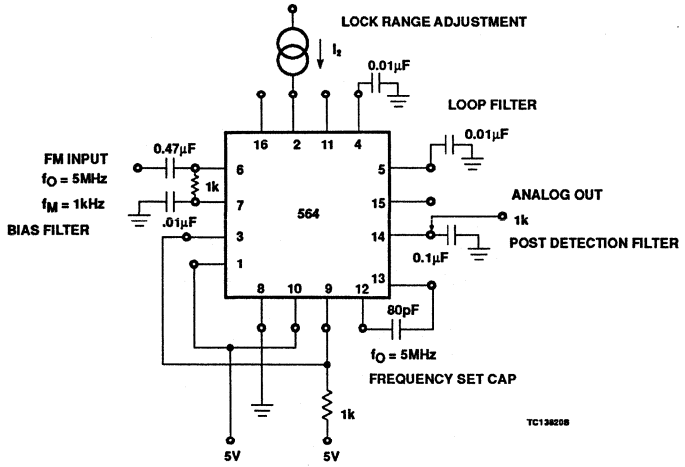


Figure 2. FM Demodulator at 5V

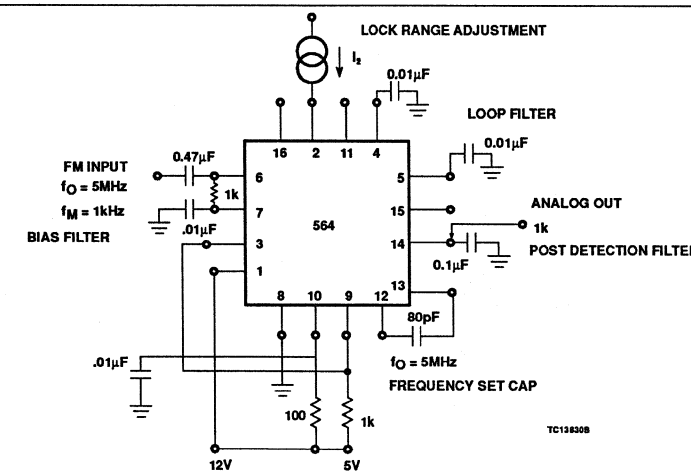


Figure 3. FM Demodulator at 12V

Phase–locked loop | NE/SE564

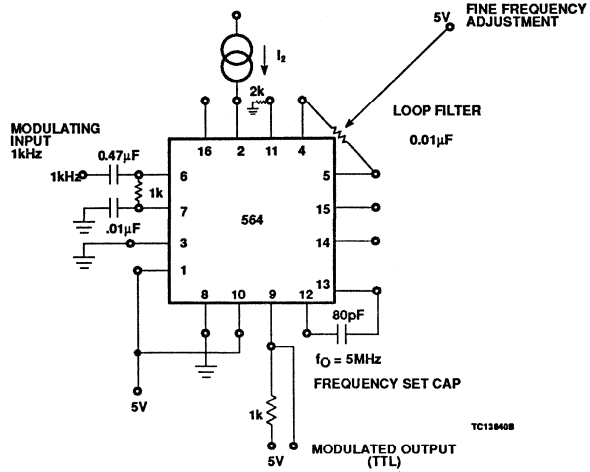


Figure 4. Modulator

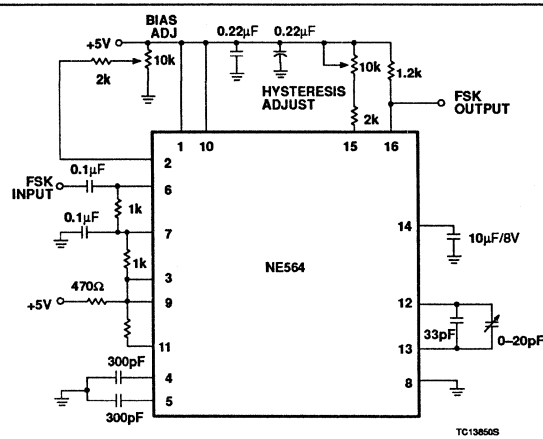
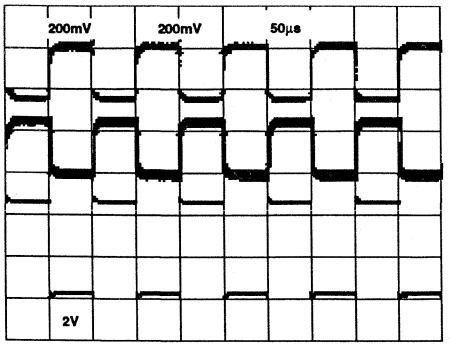
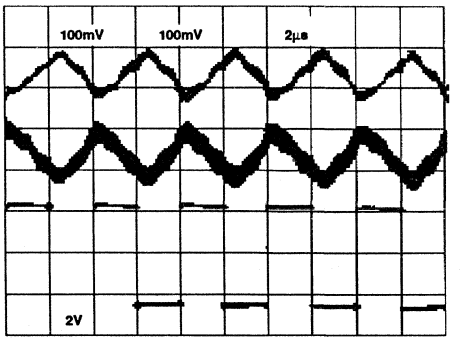


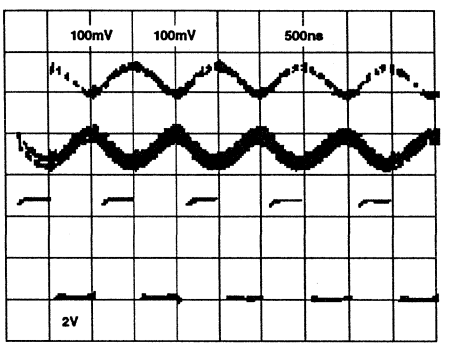
Figure 5. 10.8MHz FSK Decoder Using the 564



a. Data Rate = 20k Baud



b. Data Rate = 500k Baud



c. Data Rate = 2.0m Baud

NOTES:
1. Top trace = Pin 4
2. Center trace = Pin 5
3. Bottom trace = Pin 16

Figure 6. Phase Comparator (Pins 4 and 5) and FSK (Pin 16) Outputs

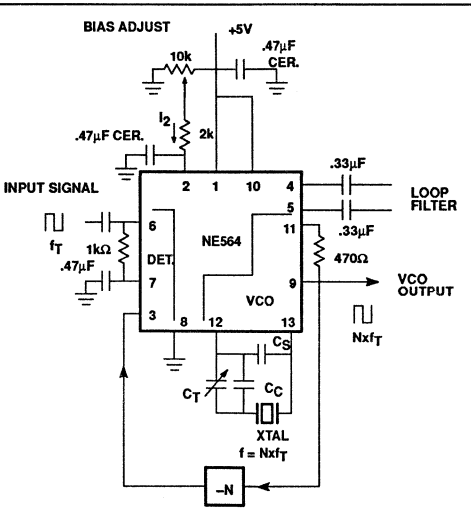


Figure 7. NE564 Phase–Locked Frequency Multiplier with VCXO

NE/SE565
Phase-Locked Loop

Product Specification

DESCRIPTION

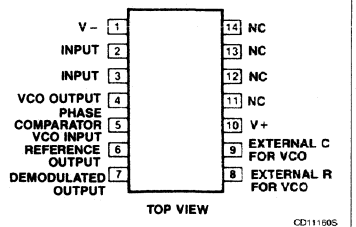
The NE/SE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low pass filter as shown in the Block Diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

FEATURES

- **Highly stable center frequency (200ppm/°C typ.)**
- **Wide operating voltage range (± 6V to ± 12V)**
- **Highly linear demodulated output (0.2% typ.)**
- **Center frequency programming by means of a resistor or capacitor, voltage or current**
- **TTL and DTL compatible square wave output; loop can be opened to insert digital frequency divider**
- **Highly linear triangle wave output**
- **Reference output for connection of comparator in frequency discriminator**
- **Bandwidth adjustable from $< \pm 1\%$ to $> \pm 60\%$**
- **Frequency adjustable over 10 to 1 range with same capacitor**

PIN CONFIGURATIONS

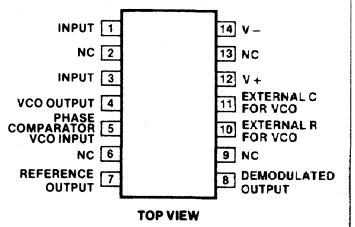
F, N Packages



TOP VIEW

CD11160S

D Package[1]

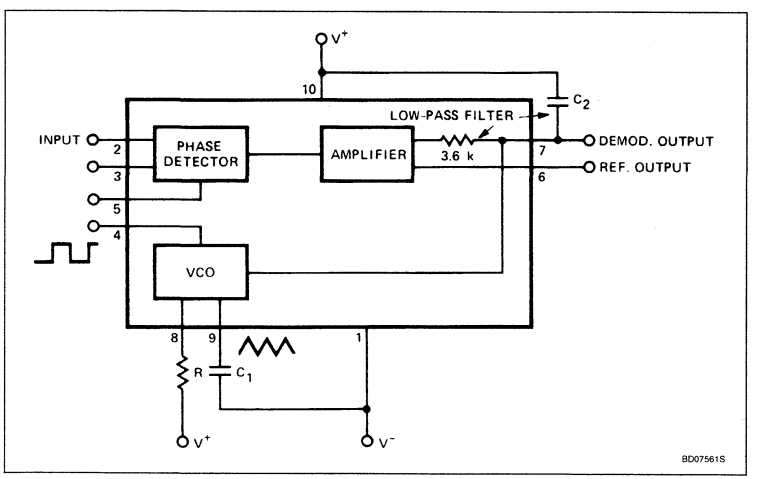


TOP VIEW

CD11170S

NOTE:
1. SO and non-standard pin out.

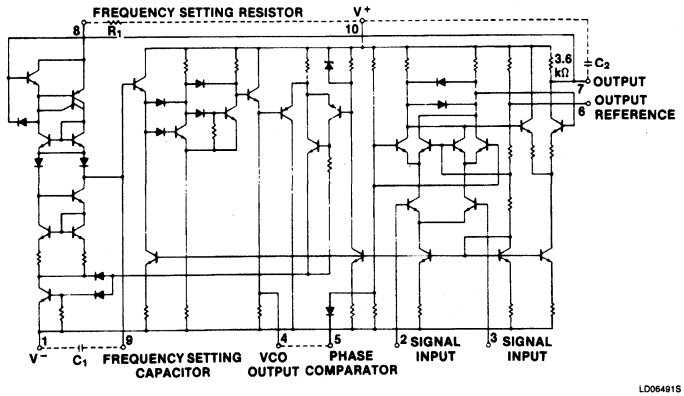
BLOCK DIAGRAM



APPLICATIONS

- **Frequency shift keying**
- **Modems**
- **Telemetry receivers**
- **Tone decoders**
- **SCA receivers**
- **Wide-band FM discriminators**
- **Data synchronizers**
- **Tracking filters**
- **Signal restoration**
- **Frequency multiplication & division**

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE565D
14-Pin Cerdip	0 to +70°C	NE565F
14-Pin Plastic DIP	0 to +70°C	NE565N
14-Pin Cerdip	−55°C to +125°C	SE565F
14-Pin Plastic DIP	−55°C to +125°C	SE565N

ABSOLUTE MAXIMUM RATINGS T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V+	Maximum operating voltage	26	V
V_{IN}	Input voltage	3	V_{P-P}
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range NE565 SE565	 0 to +70 −55 to +125	 °C °C
P_D	Power dissipation	300	mW

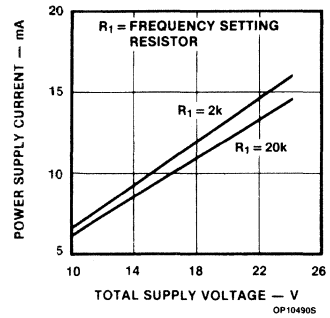
DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 6V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE565			NE565			UNIT
			Min	Typ	Max	Min	Typ	Max	
Supply requirements									
V_{CC}	Supply voltage		±6		±12	±6		±12	V
I_{CC}	Supply current			8	12.5		8	12.5	mA
Input characteristics									
	Input impedance[1]		7	10		5	10		kΩ
	Input level required for tracking	f_O = 50kHz, ±10% frequency deviation	10			10			mV_{RMS}
VCO characteristics									
f_C	Center frequency Maximum value distribution[2]	 Distribution taken about f_O = 50kHz, R_1 = 5.0kΩ, C_1 = 1200pF	300 −10	500 0	 +10	 −30	500 0	 +30	kHz %
	Drift with temperature Drift with supply voltage	f_O = 50kHz f_O = 50kHz, V_{CC} = ±6 to ±7V		500 0.1	 1.0		600 0.2	 1.5	ppm/°C %/V
	Triangle wave output voltage level linearity		1.9	2.4 0.2	3	1.9	2.4 0.5	3	V_{P-P} %
	Square wave logical "1" output voltage logical "0" output voltage	 f_O = 50kHz f_O = 50kHz	 +4.9	 +5.2 −0.2	 +0.2	 +4.9	 +5.2 −0.2	 +0.2	 V V
	Duty cycle	f_O = 50kHz	45	50	55	40	50	60	%
t_R	Rise time			20	100		20		ns
t_F	Fall time			50	200		50		ns
I_{SINK}	Output current (sink)		0.6	1		0.6	1		mA
I_{SOURCE}	Output current (source)		5	10		5	10		mA
Demodulated output characteristics									
V_{OUT}	Output voltage level	Measured at Pin 7	4.25	4.5	4.75	4.0	4.5	5.0	V
	Maximum voltage swing[3]			2			2		V_{P-P}
	Output voltage swing	±10% frequency deviation	250	300		200	300		mV_{P-P}
THD	Total harmonic distortion			0.2	0.75		0.4	1.5	%
	Output impedance[4]			3.6			3.6		kΩ
V_{OS}	Offset voltage (V6 − V7)			30	100		50	200	mV
	Offset voltage vs temperature (drift)			50			100		µV/°C
	AM rejection		30	40			40		dB

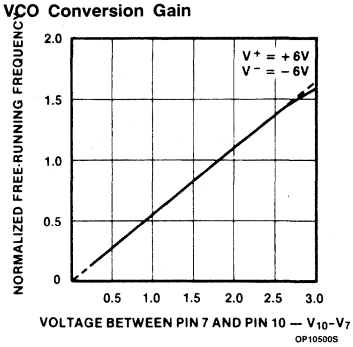
NOTES:
1. Both input terminals (Pins 2 and 3) must receive identical DC bias. This bias may range from 0V to −4V.
2. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20kΩ.
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

TYPICAL PERFORMANCE CHARACTERISTICS

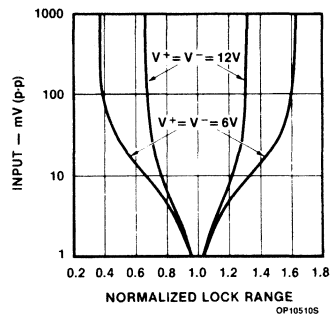
Power Supply Current as a Function of Supply Voltage



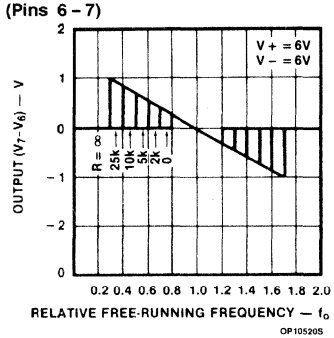
VCO Conversion Gain



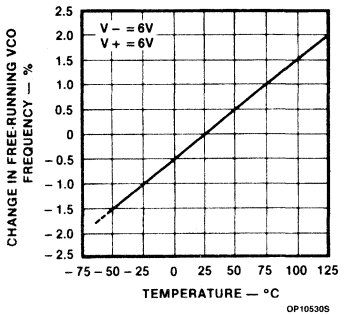
Lock Range as a Function of Input Voltage



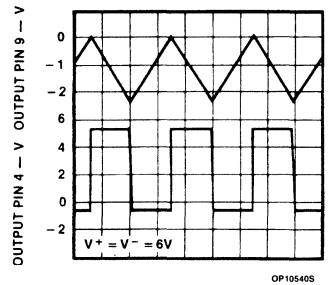
Lock Range as a Function of Gain Setting Resistance (Pins 6 - 7)



Change in Free-Running VCO Frequency as a Function of Temperature



VCO Output Waveform



DESIGN FORMULAS (See Figure 1)

Free-running frequency of VCO:

$$f_O \simeq \frac{1.2}{4R_1C_1} \text{ in Hz}$$

Lock range: $f_L = \pm \frac{8f_O}{V_{CC}}$ in Hz

Capture range: $f_C \simeq \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6 \times 10^3) \times C_2$

TYPICAL APPLICATIONS

FM Demodulation

The 565 Phase-Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average DC level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$$f_O \simeq \frac{1.2}{4R_1C_1}$$

and should be adjusted to be at the center of the input signal frequency range. C_1 can be any value, but R_1 should be within the range of 2000 to 20,000Ω with an optimum value on the order of 4000Ω. The source can be direct coupled if the DC resistances seen from Pins 2 and 3 are equal and there is no DC voltage difference between the pins. A short between Pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a DC reference voltage that is close to the DC potential of the demodulated output (Pin 7). Thus, if a resistance is connected between Pins 6 and 7, the gain of the output stage can be reduced with little change in the DC voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ±60% of f_O to approximately ±20% of f_O (at ±6V).

A small capacitor (typically 0.001μF) should be connected between Pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between Pin 7 and the positive supply, and an internal resistance of approximately 3600Ω.

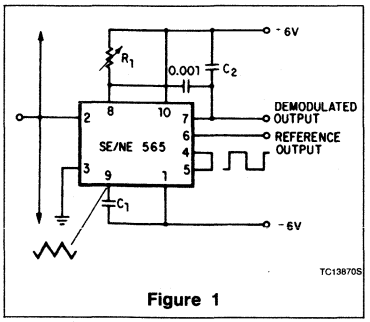


Figure 1

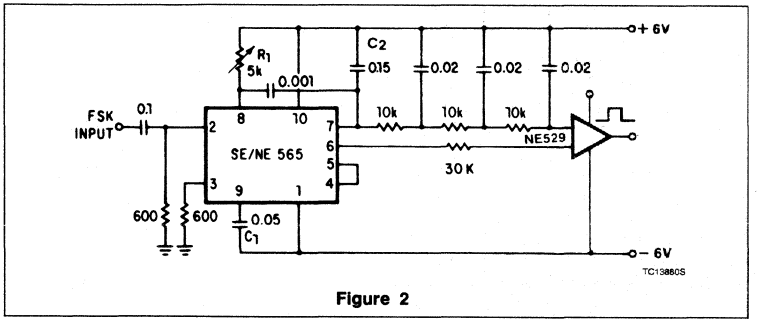


Figure 2

Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" to "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding DC shift at the output.

The loop filter capacitor C_2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150Hz) and twice the input frequency (approximately 2200Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and Pin 6 of the loop. The free-running frequency is adjusted with R_1 so as to result in a slightly-positive voltage at the output with f_{IN} = 1070Hz.

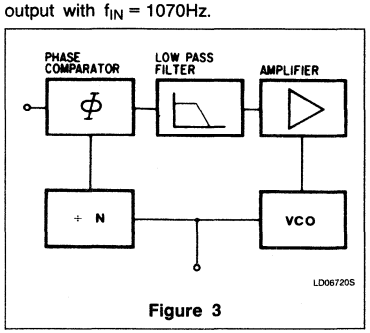


Figure 3

The input connection is typical for cases where a DC voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect at 600Ω input impedance).

Frequency Multiplication

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R_1 and C_1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C_2, should be large enough to eliminate variations in the demodulated output voltage (at Pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_{IN}) as long as the loop is in lock.

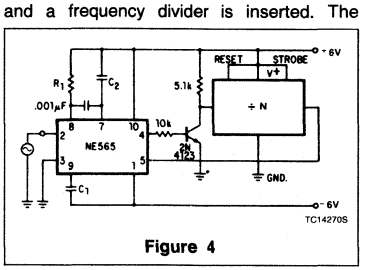


Figure 4

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commercial use. To do this, a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase-Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (Pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000Ω.

The Phase-Locked Loop is tuned to 67kHz with a 5000Ω potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (Pin 7) passes through a three-stage low pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at Pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz.

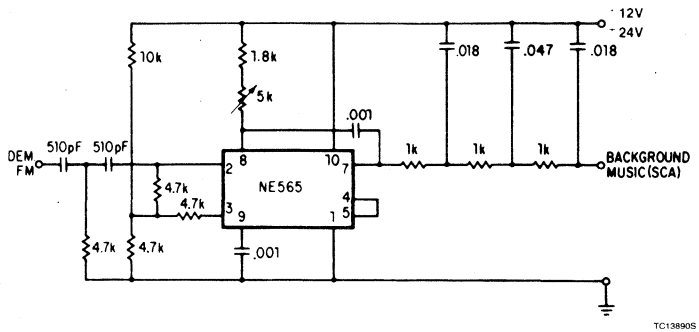


Figure 5

NE/SE566
Function Generator

Product Specification

DESCRIPTION

The NE/SE566 Function Generator is a voltage-controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten-to-one frequency range by proper selection of an external resistance and modulated over a ten-to-one range by the control voltage, with exceptional linearity.

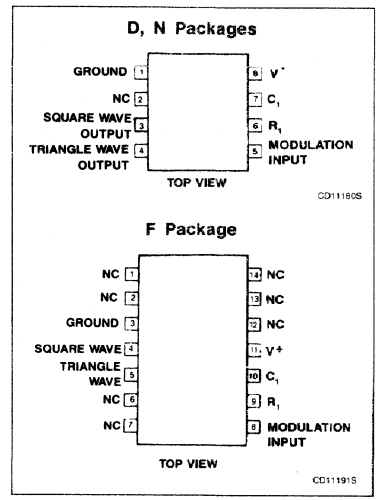
FEATURES

- **Wide range of operating voltage (up to 24V; single or dual)**
- **High linearity of modulation**
- **Highly stable center frequency (200ppm/°C typical)**
- **Highly linear triangle wave output**
- **Frequency programming by means of a resistor or capacitor, voltage or current**
- **Frequency adjustable over 10-to-1 range with same capacitor**

APPLICATIONS

- **Tone generators**
- **Frequency shift keying**
- **FM modulators**
- **Clock generators**
- **Signal generators**
- **Function generators**

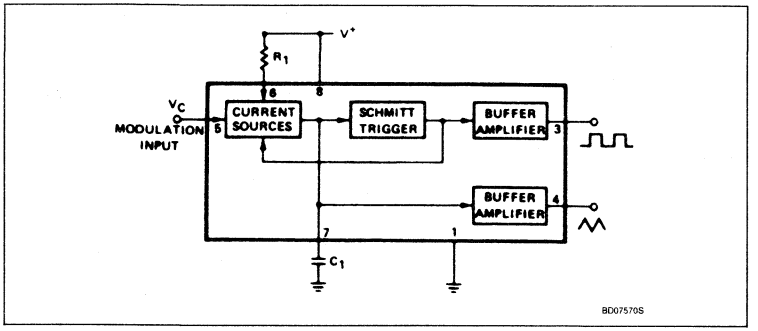
PIN CONFIGURATIONS



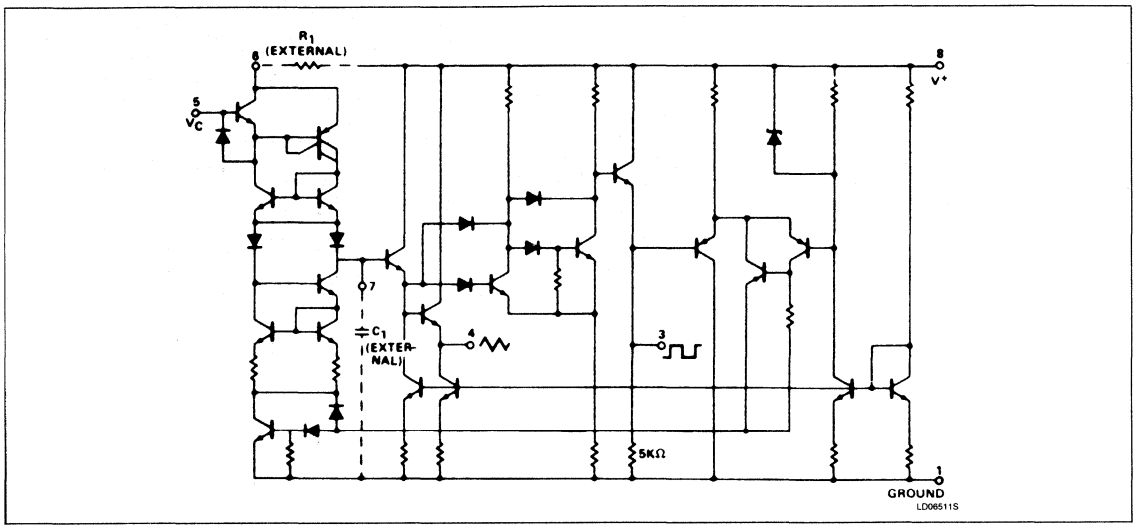
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE566D
14-Pin Cerdip	0 to +70°C	NE566F
8-Pin Plastic DIP	0 to +70°C	NE566N
14-Pin Cerdip	−55°C to +125°C	SE566F
8-Pin Plastic DIP	−55°C to +125°C	SE566N

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+	Maximum operating voltage	26	V
V_{IN}	Input voltage	3	V_{P-P}
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range NE566 SE566	 0 to +70 −55 to +125	 °C °C
P_D	Power dissipation	300	mW

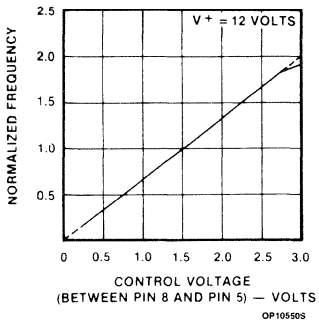
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = \pm 6V$, unless otherwise specified.

SYMBOL	PARAMETER	SE566			NE566			UNIT
		Min	Typ	Max	Min	Typ	Max	
General								
T_A	Operating ambient temperature range	−55		125	0		70	°C
V_{CC}	Operating supply voltage	±6		±12	±6		±12	V
I_{CC}	Operating supply current		7	12.5		7	12.5	mA
VCO[1]								
f_{MAX}	Maximum operating frequency		1			1		MHz
	Frequency drift with temperature		500			600		ppm/°C
	Frequency drift with supply voltage		0.1	1		0.2	2	%/V
	Control terminal input impedance[2]		1			1		MΩ
	FM distortion (±10% deviation)		0.2	0.75		0.4	1.5	%
	Maximum sweep rate		1			1		MHz
	Sweep range		10:1			10:1		
Output								
	Triangle wave output							
	impedance		50			50		Ω
	voltage	1.9	2.4		1.9	2.4		V_{P-P}
	linearity		0.2			0.5		%
	Square wave input							
	impedance		50			50		Ω
	voltage	5	5.4		5	5.4		V_{P-P}
	duty Cycle	45	50	55	40	50	60	%
t_R	Rise time		20			20		ns
t_F	Fall Time		50			50		ns

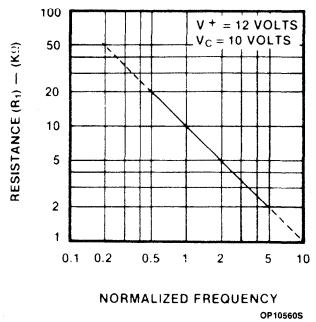
NOTES:
1. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20kΩ.
2. The bias voltage (V_C) applied to the control terminal (Pin 5) should be in the range $\frac{3}{4}V+ \leq V_C \leq V+$.

TYPICAL PERFORMANCE CHARACTERISTICS

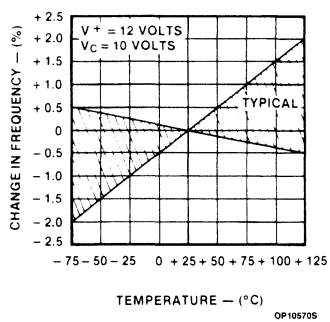
Normalized Frequency as a Function of Control Voltage



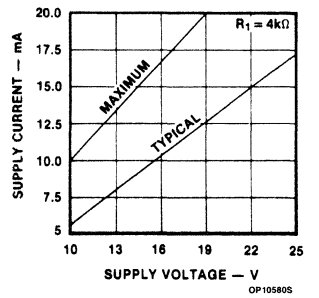
Normalized Frequency as a Function of Resistance (R1)



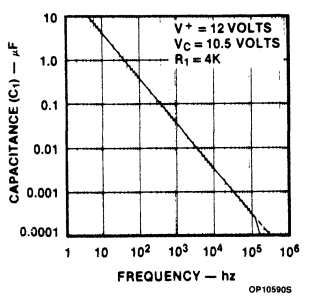
Change in Frequency as a Function of Temperature



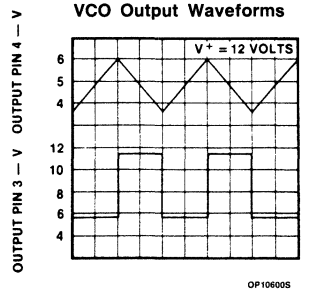
Power Supply Current as a Function of Supply Voltage



Frequency as a Function of Capacitance (C1)



VCO Output Waveforms



OPERATING INSTRUCTIONS

The NE/SE566 Function Generator is a general purpose voltage-controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1MHz. A typical connection diagram is shown in Figure 1. The control terminal (Pin 5) must be biased externally with a voltage (V_C) in the range

$$\tfrac{3}{4}V+ \leq V_C \leq V+$$

where V_{CC} is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with R_2 and R_3. The modulating signal is then AC coupled with the capacitor C_2. The modulating signal can be direct coupled as well, if the appropriate DC bias voltage is applied to the control terminal. The frequency is given approximately by

$$f_O = \frac{2[(V+) - (V_C)]}{R_1 C_1 V+}$$

and R_1 should be in the range $2k\Omega < R_1 < 20k\Omega$.

A small capacitor (typically $0.001\mu F$) should be connected between Pins 5 and 6 to eliminate possible oscillation in the control current source.

If the VCO is to be used to drive standard logic circuitry, it may be desirable to use a dual supply as shown in Figure 2. In this case the square wave output has the proper DC levels for logic circuitry. RTL can be driven directly from Pin 3. For DTL or TTL gates, which require a current sink of more than 1mA, it is usually necessary to connect a $5k\Omega$ resistor between Pin 3 and negative supply. This increases the current sinking capability to 2mA. The third type of interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for TTL circuitry which requires a fast fall time (< 50ns) and a large current sinking capability.

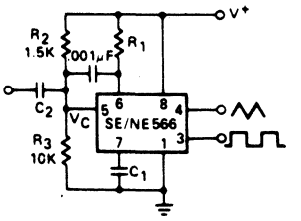


Figure 1

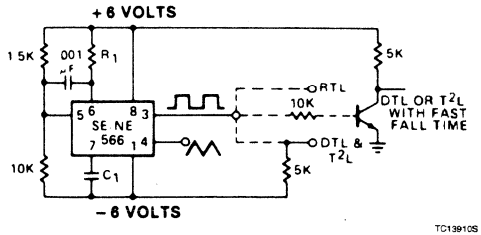


Figure 2

NE/SE567
Tone Decoder/Phase-Locked Loop

Product Specification

DESCRIPTION

The NE/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency and output delay are independently determined by means of four external components.

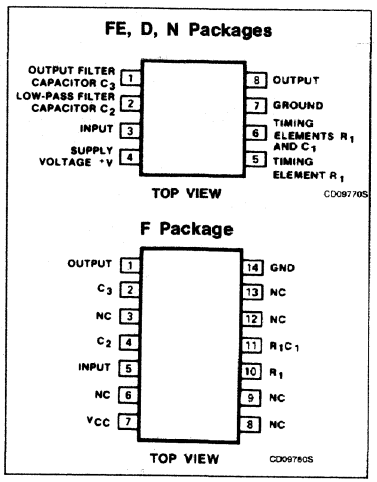
FEATURES

- **Wide frequency range (.01Hz to 500kHz)**
- **High stability of center frequency**
- **Independently controllable bandwidth (up to 14%)**
- **High out-band signal and noise rejection**
- **Logic-compatible output with 100mA current sinking capability**
- **Inherent immunity to false signals**
- **Frequency adjustment over a 20–to-1 range with an external resistor**
- **Military processing available**

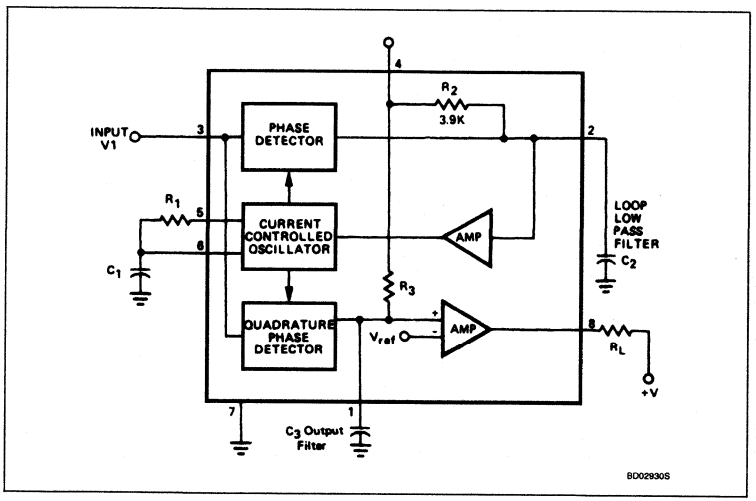
APPLICATIONS

- **Touch-Tone® decoding**
- **Carrier current remote controls**
- **Ultrasonic controls (remote TV, etc.)**
- **Communications paging**
- **Frequency monitoring and control**
- **Wireless intercom**
- **Precision oscillator**

PIN CONFIGURATIONS

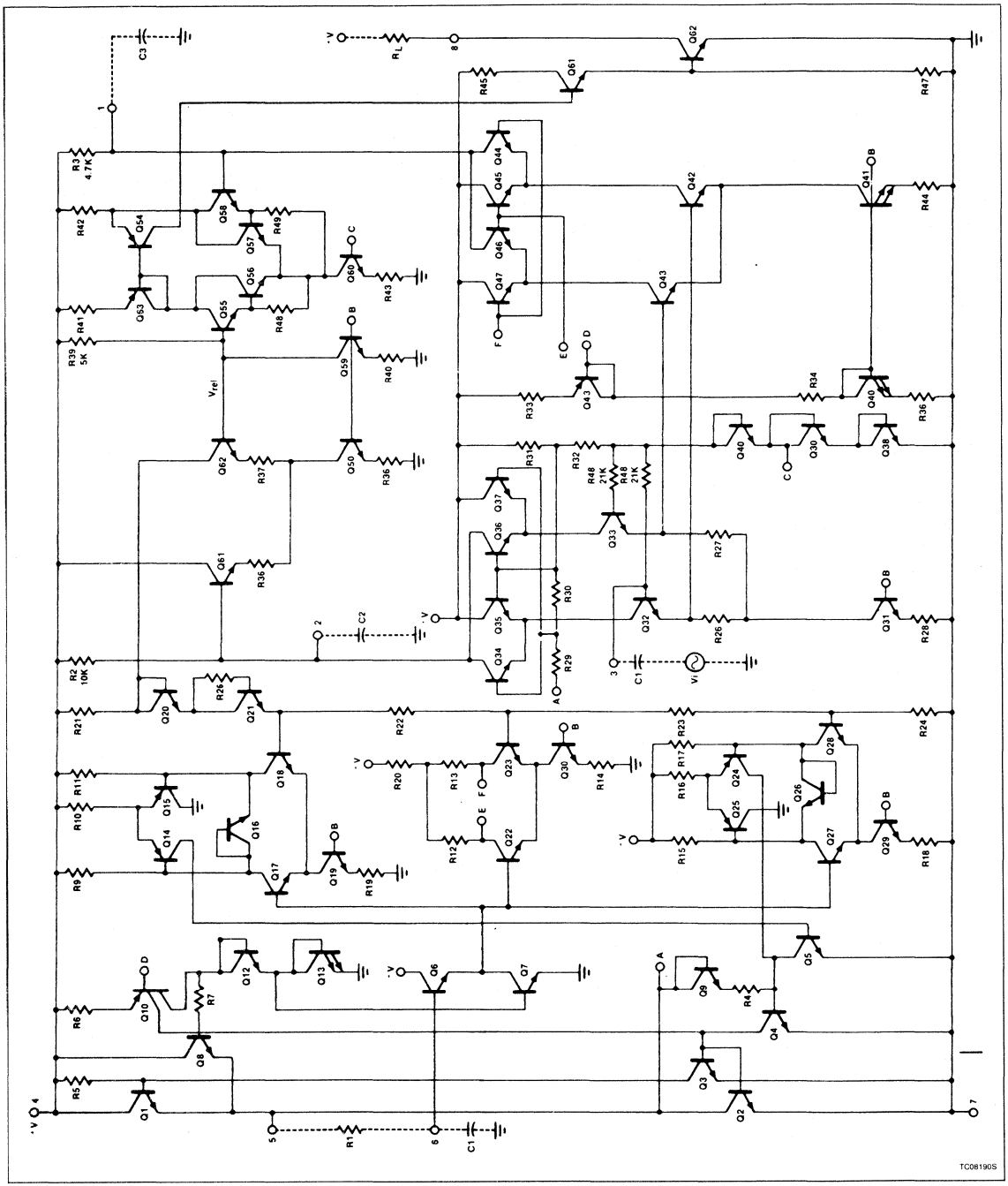


BLOCK DIAGRAM



®Touch-Tone is a registered trademark of AT & T.

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE567D
14-Pin Cerdip	0 to +70°C	NE567F
8-Pin Cerdip	0 to +70°C	NE567FE
8-Pin Plastic DIP	0 to +70°C	NE567N
8-Pin Plastic SO	−55°C to +125°C	SE567D
14-Pin Cerdip	−55°C to +125°C	SE567F
8-Pin Cerdip	−55°C to +125°C	SE567FE
8-Pin Plastic DIP	−55°C to +125°C	SE567N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature NE567 SE567	 0 to +70 −55 to +125	 °C °C
V_{CC}	Operating voltage	10	V
V+	Positive voltage at input	0.5 + V_S	V
V−	Negative voltage at input	−10	V_{DC}
V_{OUT}	Output voltage (collector of output transistor)	15	V_{DC}
T_{STG}	Storage temperature range	−65 to +150	°C
P_D	Power dissipation	300	mW

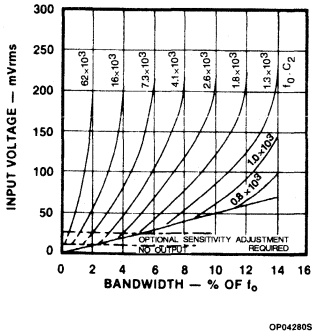
DC ELECTRICAL CHARACTERISTICS $V+ = 5.0V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
			Min	Typ	Max	Min	Typ	Max	
Center frequency[1]									
f_O	Highest center frequency			500			500		kHz
f_O	Center frequency stability[2]	−55 to +125°C 0 to +70°C		35 ±140 35 ±60			35 ±140 35 ±60		ppm/°C ppm/°C
f_O	Center frequency distribution	$f_O = 100kHz = \frac{1}{1.1\ R_1C_1}$	−10	0	+10	−10	0	+10	%
f_O	Center frequency shift with supply voltage	$f_O = 100kHz = \frac{1}{1.1\ R_1C_1}$		0.5	1		0.7	2	%/V
Detection bandwidth									
BW	Largest detection bandwidth	$f_O = 100kHz = \frac{1}{1.1\ R_1C_1}$	12	14	16	10	14	18	% of f_O
BW	Largest detection bandwidth skew			2	4		3	6	% of f_O
BW	Largest detection bandwidth — variation with temperature	$V_I = 300mV_{RMS}$		±0.1			±0.1		%/°C
BW	Largest detectionbandwidth — variation with supply voltage	$V_I = 300mV_{RMS}$		±2			±2		%/V
Input									
R_{IN}	Input resistance		15	20	25	15	20	25	kΩ
V_I	Smallest detectable input voltage[4]	$I_L = 100mA$, $f_I = f_O$		20	25		20	25	mV_{RMS}
	Largest no-output input voltage[4]	$I_L = 100mA$, $f_I = f_O$	10	15		10	15		mV_{RMS}
	Greatest simultaneous out-band signal-to-in-band signal ratio			+6			+6		dB
	Minimum input signal to wide-band noise ratio	$B_n = 140kHz$		−6			−6		dB
Output									
	Fastest on-off cycling rate			$f_O/20$			$f_O/20$		
	"1" output leakage current	$V_8 = 15V$		0.01	25		0.01	25	μA
	"0" output voltage	$I_L = 30mA$ $I_L = 100mA$		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V V
t_F	Output fall time[3]	$R_L = 50Ω$		30			30		ns
t_R	Output rise time[3]	$R_L = 50Ω$		150			150		ns
General									
V_{CC}	Operating voltage range		4.75		9.0	4.75		9.0	V
	Supply current quiescent			6	8		7	10	mA
	Supply current — activated	$R_L = 20kΩ$		11	13		12	15	mA
t_{PD}	Quiescent power dissipation			30			35		mW

NOTES:
1. Frequency determining resistor R_1 should be between 2 and 20kΩ.
2. Applicable over 4.75V to 5.75V. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.
4. With $R_2 = 130kΩ$ from Pin 1 to V+. See Figure 1.

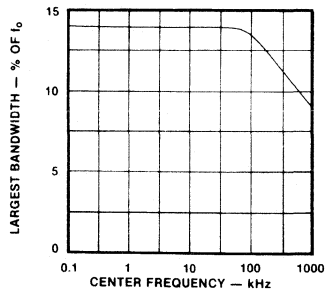
TYPICAL PERFORMANCE CHARACTERISTICS

Bandwidth vs Input Signal Amplitude



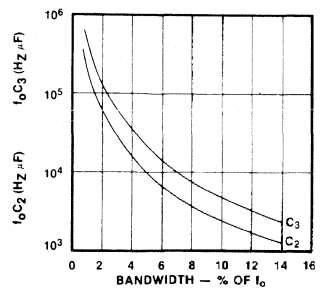
OP04280S

Largest Detection Bandwidth vs Operating Frequency



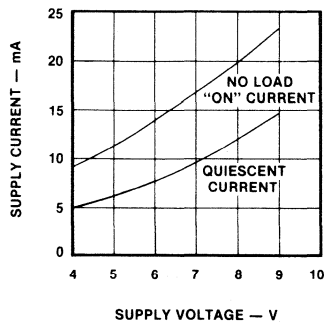
OP04290S

Detection Bandwidth as a Function of C_2 and C_3



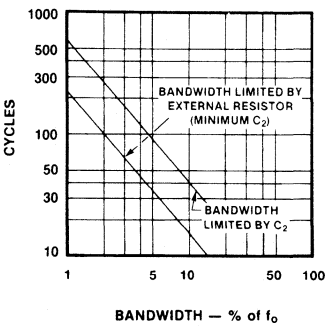
OP04300S

Typical Supply Current vs Supply Voltage



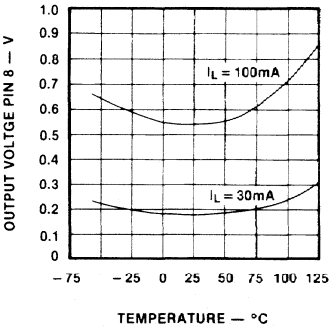
OP04310S

Greatest Number of Cycles Before Output

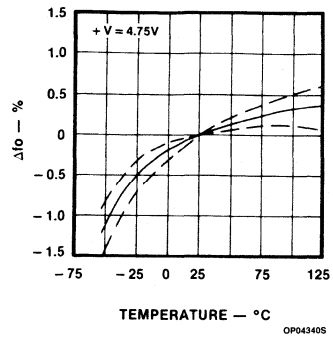


OP04320S

Typical Output Voltage vs Temperature

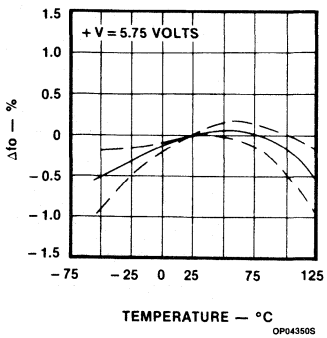


Typical Frequency Drift With Temperature (Mean and SD)



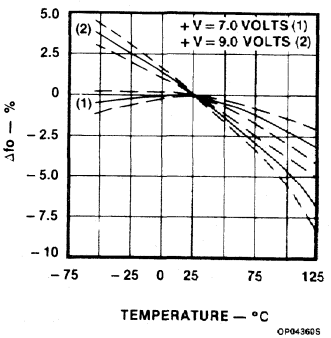
OP04340S

Typical Frequency Drift With Temperature (Mean and SD)



OP04350S

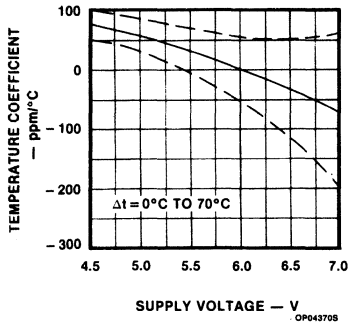
Typical Frequency Drift With Temperature (Mean and SD)



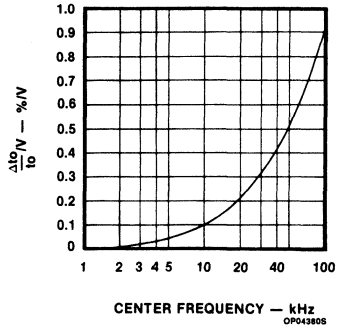
OP04360S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

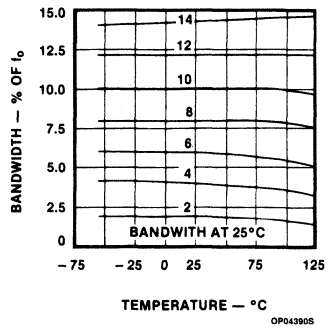
Center Frequency Temperature Coefficient (Mean and SD)



Center Frequency Shift With Supply Voltage Change vs Operating Frequency



Typical Bandwidth Variation Temperature



DESIGN FORMULAS

$$f_O \cong \frac{1}{1.1R_1C_1}$$

$$BW \simeq 1070\sqrt{\frac{V_I}{f_OC_2}} \text{ in \% of } f_O,$$

$$V_I \leq 200mV_{RMS}$$

Where

V_I = Input voltage (V_{RMS})

C_2 = Low-pass filter capacitor (μF)

PHASE-LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (f_O)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_O, within which an input signal above the threshold voltage (typically $20mV_{RMS}$) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

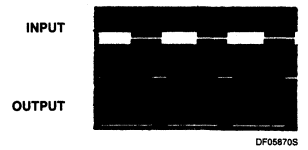
A measure of how well the detection band is centered about the center frequency, f_O. The skew is defined as $(f_{MAX}+f_{MIN}-2f_O)/2f_O$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R_1C_1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.

TYPICAL RESPONSE



NOTE:
$R_L = 100\Omega$

Response to $100mV_{RMS}$ Tone Burst

NOTES:
S/N = –6dB
$R_L = 100\Omega$
Noise Bandwidth = 140Hz

Response to Same Input Tone Burst With Wideband Noise

2. Select the low-pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude Variation is known, the appropriate value of f_OC_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constand bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_OC_2 product (f_O (Hz), $C_2(\mu F)$).
3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low-pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the

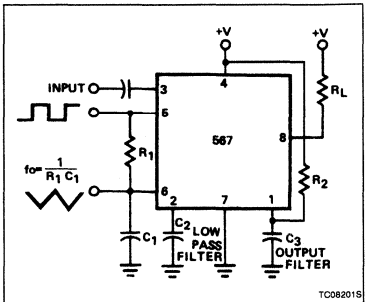


Figure 1

output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

4. Optional resistor R_2 sets the threshold for the largest "no output" input voltage. A value of 130kΩ is used to assure the tested limit of $10mV_{RMS}$ min. This resistor can be referenced to ground for increased sensitivity. The explanation can be found in the "optional controls" section which follows.

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, Pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at Pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_O with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{BE}) \approx (+V - 1.4V)$ having a DC average of $+V/2$. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of $1V_{P-P}$ with an average DC level of $+V/2$. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

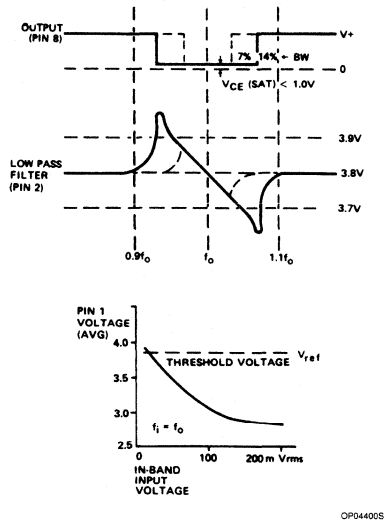


Figure 2

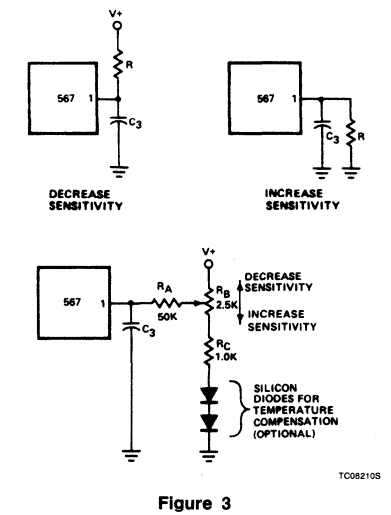


Figure 3

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the inband signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_O/3$, $f_O/5$, etc.
2. The 567 will lock onto signals near $(2n + 1)$ f_O, and will give an output for signals near $(4n + 1)$ f_O where $n = 0, 1, 2$, etc. Thus, signals at $5f_O$ and $9f_O$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and out-band signals is afforded in the low input level (below $200mV_{RMS}$) and reduced bandwidth operating mode. However, decreased loop damping causes the worst-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can

cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_O/10$ baud.

$$C_2 = \frac{130}{f_O}\mu F$$

$$C_3 = \frac{260}{f_O}\mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emmitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

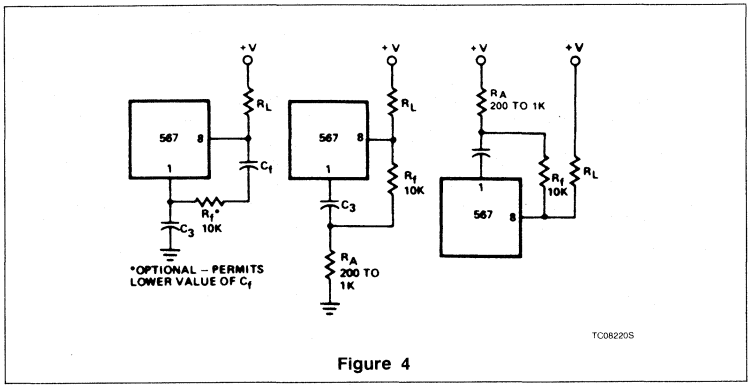


Figure 4

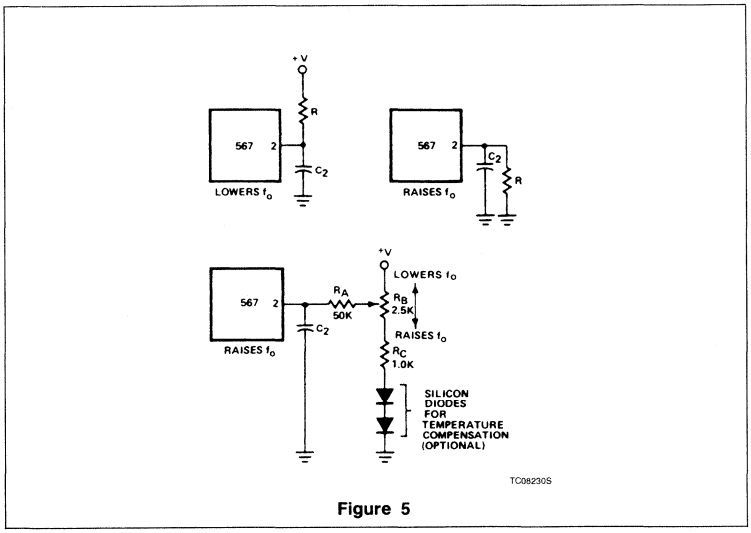


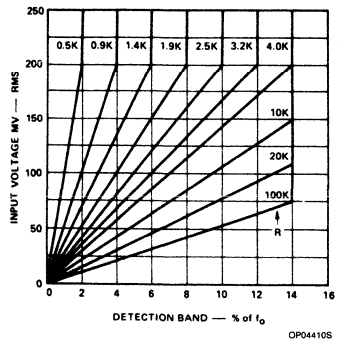
Figure 5

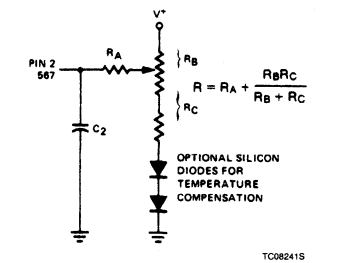
SENSITIVITY ADJUSTMENT

(Figure 3)

When operated as a very narrow-band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and out-band signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the out-band beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.





NOTE:

$$\frac{130}{f_O}\left(\frac{10k+R}{R}\right) < C_2 < \frac{1300}{f_O}\left(\frac{10k+R}{R}\right)$$

Adjust control for symmetry of detection band edges about f_O.

Figure 6

CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (Pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

(Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION

(Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between Pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

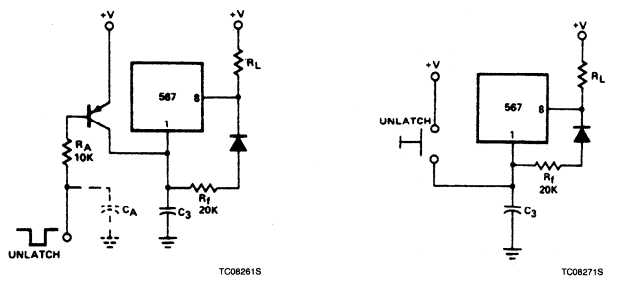
REDUCTION OF C1 VALUE

(Figure 8)

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage-follower between the R_1 C_1 junction and Pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

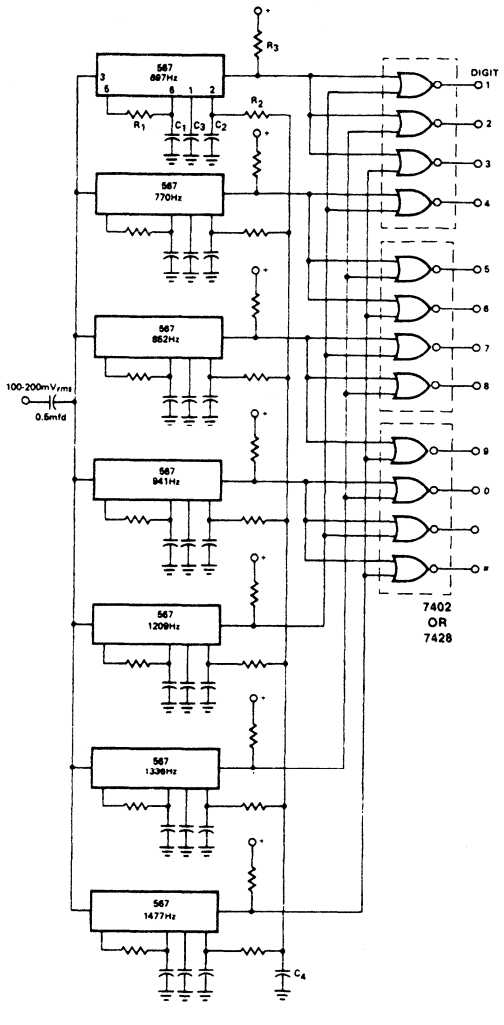
To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating NPN transistors.



NOTE:
C_A prevents latch-up when power supply is turned on.

Figure 7. Output Latching

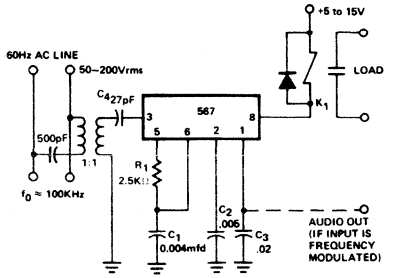
TYPICAL APPLICATIONS



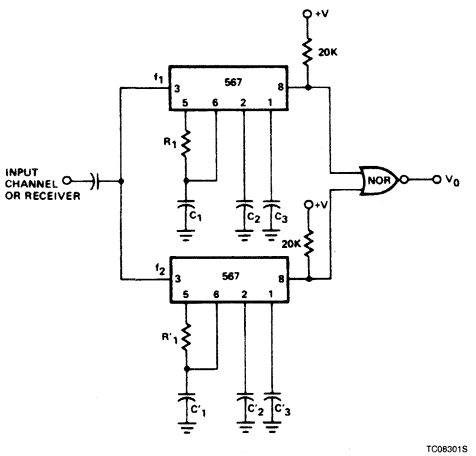
Touch-Tone® Decoder

NOTES:
Component values (Typical)
R_1 = 26.8 to 15kΩ
R_2 = 24.7kΩ
R_3 = 20kΩ
C_1 = 0.10mF
C_2 = 1.0mF 5V
C_3 = 2.2mF 6V
C_4 = 250μF 6V

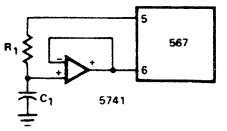
TYPICAL APPLICATIONS (Continued)



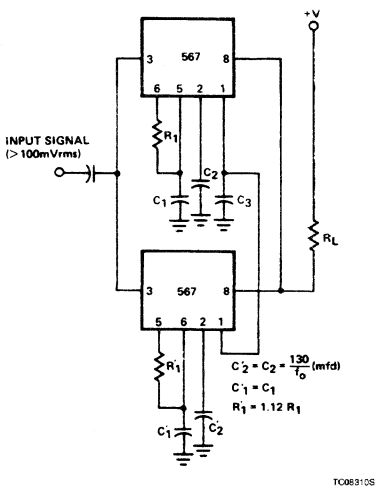
Carrier-Current Remote Control or Intercom



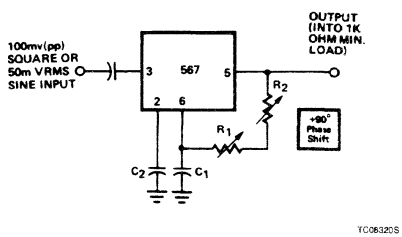
Dual-Tone Decoder



Precision VLF



24% Bandwidth Tone Decoder

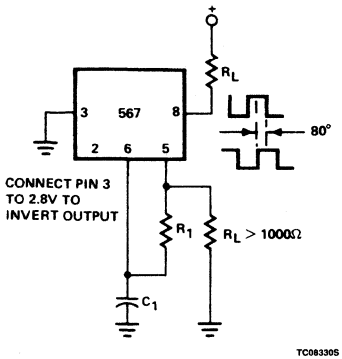


NOTES
$R_2 = R_1/5$
Adjust R_1 so that $\phi = 90°$ with control midway.

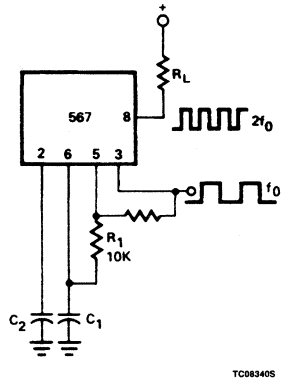
0° to 180° Phase Shifter

NOTES:
1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

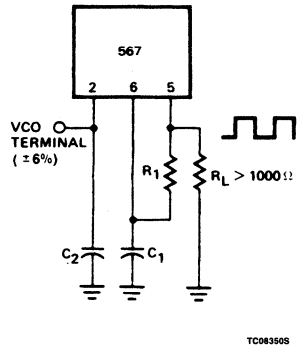
TYPICAL APPLICATIONS (Continued)



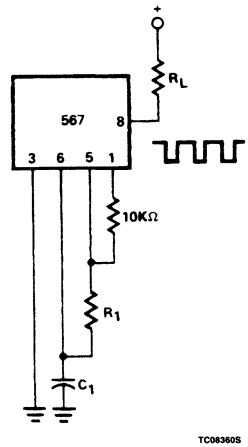
Oscillator With Quadrature Output



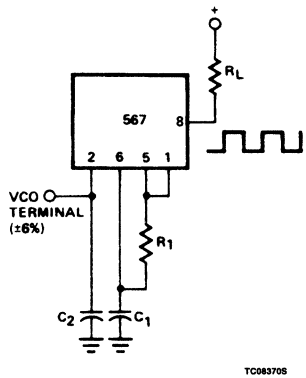
Oscillator With Double Frequency Output



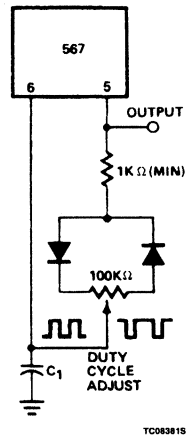
Precision Oscillator With 20ns Switching



Pulse Generator With 25% Duty Cycle



Precision Oscillator to Switch 100mA Loads



Pulse Generator

NE568
150MHz Phase-Locked Loop

Preliminary Specification

DESCRIPTION

The NE568 is a monolithic phase-locked loop (PLL) which operates from 1Hz to frequencies in excess of 150MHz. The integrated circuit consists of a limiting amplifier, a current-controlled oscillator (ICO), a phase detector, a level shift circuit, V/I and I/V converters, an output buffer, and bias circuitry with temperature and frequency compensating characteristics. The design of the NE568 is particularly well-suited for demodulation of FM signals with extremely large deviation in systems which require a highly linear output. In satellite receiver applications with a 70MHz IF, the NE568 will demodulate ±20% deviations with less than 1.0% typical non-linearity. In addition to high linearity, the circuit has a loop filter which can be configured with series or shunt elements to optimize loop dynamic performance. The NE568 is available in 20-pin dual in-line and 20-pin SO (surface-mounted) plastic packages.

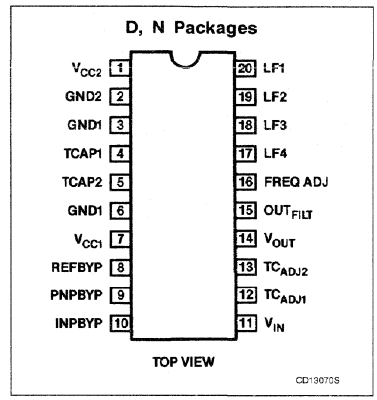
FEATURES

- **Operation to 150MHz**
- **High linearity buffered output**
- **Series or shunt loop filter component capability**
- **Temperature compensated**

APPLICATIONS

- **Satellite receivers**
- **Fiber-optic video links**
- **VHF FSK demodulators**
- **Clock recovery**

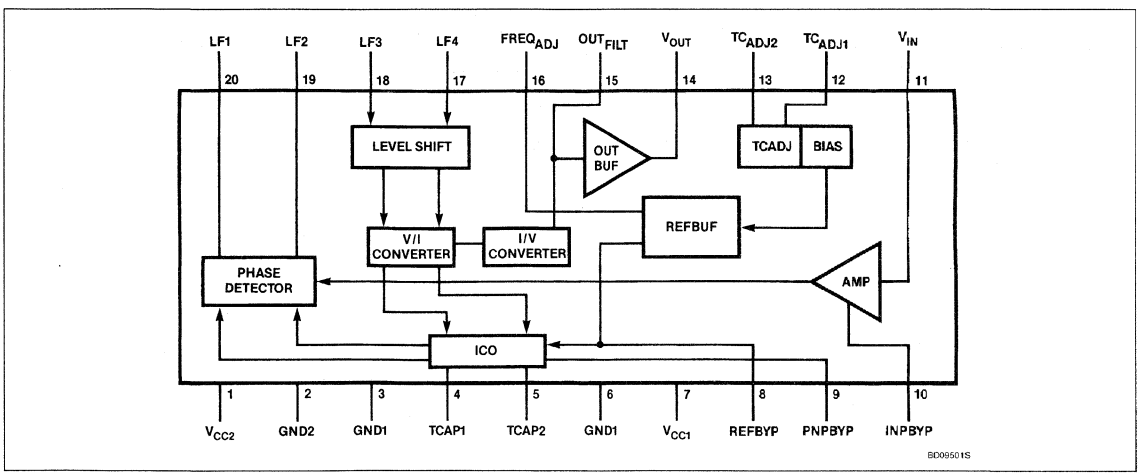
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL Package	0 to +70°C	NE568D
20-Pin Plastic DIP	0 to +70°C	NE568N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	6	V
T_A	Operating free-air ambient temperature range	0 to +70	°C
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_{DMAX}	Maximum power dissipation	500	mW

ELECTRICAL CHARACTERISTICS

The electrical characteristics listed below are actual tests (unless otherwise stated) performed on each device with an automatic IC tester prior to shipment. Performance of the device in automated test setup is not necessarily optimum. The NE568 is layout-sensitive. Evaluation of performance for correlation to the data sheet should be done with the circuit and layout of Figures 1 – 3 with the evaluation unit soldered in place. (Do not use a socket!)

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 5V$, $f_O = 70MHz$, Test Circuit Figure 1, $f_{IN} = -20dBm$, $R_4 = 0\Omega$ (ground), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{CC}	Supply current			60	75	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_{OSC}	Maximum oscillator operating frequency[3]		150			MHz
	Input signal level		50 −20[1]		2000 +10	mV_{P-P} dBm
BW	Demodulated bandwidth			$f_O/7$		MHz
	Non-linearity[5]	Dev = ±20%, Input = −20dBm		1.0	4.0	%
	Lock range[2]	Input = −20dBm	±25	±35		% of f_O
	Capture range[2]	Input = −20dBm	±20	±30		% of f_O
	TC of f_O	Figure 1		100		ppm/°C
R_{IN}	Input resistance[4]		1			kΩ
	Output impedance			6		Ω
	Demodulated V_{OUT}	Dev = ±20% of f_O measured at Pin 14	0.40	0.52		V_{P-P}
	AM rejection	V_{IN} = −20dBm (30% AM) referred to ±20% deviation		50		dB
f_O	Distribution[6]	Centered at 70MHz, $R_2 = 1.2k\Omega$, $C_2 = 17pF$, $R_4 = 0\Omega$ ($C_2 + C_{STRAY} = 20pF$)	−15	0	+15	%
f_O	Drift with supply	4.75V to 5.25V		1		%/V

NOTES:

1. Signal level to assure all published parameters. Device will continue to function at lower levels with varying performance.
2. Limits are set symmetrical to f_O. Actual characteristics may have asymmetry beyond the specified limits.
3. Not 100% tested, but guaranteed by design.
4. Input impedance depends on package and layout capacitance. See Figures 4 and 5.
5. Linearity is tested with incremental changes in input frequency and measurement of the DC output voltage at Pin 14 (V_{OUT}). Nonlinearity is then calculated from a straight line over the deviation range specified.
6. Free-running frequency is measured as feedthrough to Pin 14 (V_{OUT}) with no input signal applied.

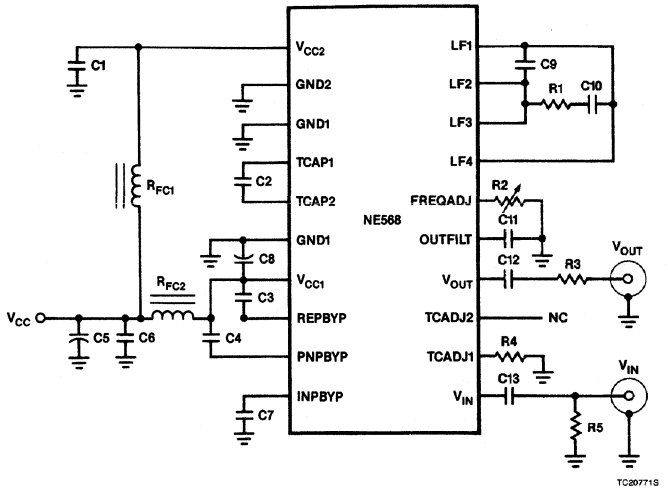


Figure 1. Test and Application Circuit

FUNCTIONAL DESCRIPTION

The NE568 is a high-performance phase-locked loop (PLL). The circuit consists of conventional PLL elements, with special circuitry for linearized demodulated output, and high-frequency performance. The process used has NPN transistors with $f_T > 6GHz$. The high gain and bandwidth of these transistors make careful attention to layout and bypass critical for optimum performance. The performance of the PLL cannot be evaluated independent of the layout. The use of the application layout in this data sheet and surface-mount capacitors are highly recommended as a starting point.

The input to the PLL is through a limiting amplifier with a gain of 200. The input of this amplifier is differential (Pins 10 and 11). For single-ended applications, the input must be coupled through a DC-blocking capacitor with low impedance at the frequency of interest. The single-ended input is normally applied to Pin 11 with Pin 10 AC-bypassed with a low-impedance capacitor. The input impedance is characteristically slightly above 500Ω. Impedance match is not necessary, but loading the signal source should be avoided. When the source is 50 or 75Ω, a DC-blocking capacitor is usually all that is needed.

Input amplification is low enough to assure reasonable response time in the case of large signals, but high enough for good AM rejection. After amplification, the input signal drives one port of a multiplier-cell phase detector. The other port is driven by the current-controlled oscillator (ICO). The output of the phase comparator is a voltage proportional to the phase difference of the input and ICO signals. The error signal is filtered with a low-pass filter to provide a DC-correction voltage, and this voltage is converted to a current which is applied to the ICO, shifting the frequency in the direction which causes the input and ICO to have a 90° phase relationship.

The oscillator is a current-controlled multivibrator. The current control affects the charge/discharge rate of the timing capacitor. It is common for this type of oscillator to be referred to as a voltage-controlled oscillator (VCO), because the output of the phase comparator and the loop filter is a voltage. To control the frequency of an integrated ICO multivibrator, the control signal must be conditioned by a voltage-to-current converter. In the NE568, special circuitry predistorts the control signal to make the change in frequency a linear function over a large control-voltage range.

The free-running frequency of the oscillator depends on the value of the timing capacitor connected between Pins 4 and 5. The value of the timing capacitor depends on internal resistive components and current sources. When $R_2 = 1.2k\Omega$ and $R_4 = 0\Omega$, a very close approximation of the correct capacitor value is:

$$C^* = \frac{0.0014}{f_O} \text{ F}$$

where

$$C^* = C_2 + C_{STRAY}.$$

The temperature-compensation resistor, R_4, affects the actual value of capacitance. This equation is normalized to 70MHz. See Figure 6 for correction factors.

The loop filter determines the dynamic characteristics of the loop. In most PLLs, the phase detector outputs are internally connected to the ICO inputs. The NE568 was designed with filter output to input connections from Pins 20 (ϕ DET) to 17 (ICO), and Pins 19 (ϕ DET) to 18 (ICO) external. This allows the use of both series and shunt loop-filter elements. The loop constants are:

$K_D = 0.127V/Radian$ (Phase Detector Constant)

$K_O = 4.2 \times 10^9 \frac{\text{Radians}}{\text{V-sec}}$ (ICO Constant)

The loop filter determines the general characteristics of the loop. Capacitors C_9, C_{10}, and resistor R_1, control the transient output of the phase detector. Capacitor C_9 suppresses 70MHz feedthrough by interaction with 100Ω load resistors internal to the phase detector.

$$C_9 = \frac{1}{2\pi\ (50)(f_O)} \text{ F}$$

At 70MHz, the calculated value is 45pF. Empirical results with the test and application board were improved when a 56pF capacitor was used.

The natural frequency for the loop filter is set by C_{10} and R_1. If the center frequency of the loop is 70MHz and the full demodulated bandwidth is desired, i.e., $f_{BW} = f_O/7 = 10MHz$, and a value for R_1 is chosen, the value of C_{10} can be calculated.

$$C_{10} = \frac{1}{2\pi\ R_1 f_{BW}} \text{ F}$$

PARTS LIST AND LAYOUT 70MHz APPLICATION NE568D

C_1	100nF	±10%	Ceramic chip	1206
C_2[1]	18pF	±2%	Ceramic chip	0805
C_2[2]	34pF	±2%	Ceramic OR chip	
C_3	100nF	±10%	Ceramic chip	1206
C_4	100nF	±10%	Ceramic chip	1206
C_5	6.8μF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic chip	1206
C_7	100nF	±10%	Ceramic chip	1206
C_8	100nF	±10%	Ceramic chip	1206
C_9	56pF	±2%	Ceramic chip	0805 or 1206
C_{10}	560pF	±2%	Ceramic chip	0805 or 1206
C_{11}	47pF	±2%	Ceramic chip	0805 or 1206
C_{12}	100nF	±10%	Ceramic chip	1206
C_{13}	100nF	±10%	Ceramic chip	1206
R_1	27Ω	±10%	Chip	1/8W
R_2	1.2kΩ		Trim pot	1/8W
R_3[3]	43Ω	±10%	Chip	1/8W
R_4[4]	4.7kΩ	±10%	Chip	1/8W
R_5[3]	50Ω	±10%	Chip	1/8W
RFC_1[5]	10μH	±10%	Surface mount	
RFC_2[5]	10μH	±10%	Surface mount	

NOTES:
1. $C_2 + C_{STRAY} = 20pF$.
2. $C_2 + C_{STRAY} = 36pF$ for temperature-compensated configuration with $R_4 = 4.7k\Omega$.
3. For 50Ω setup. $R_1 = 62\Omega$, $R_3 = 62\Omega$, $R_5 = 75\Omega$ for 75Ω application.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 18pF$.
5. 0Ω chip resistors (jumpers) may be substituted with minor degradation of performance.

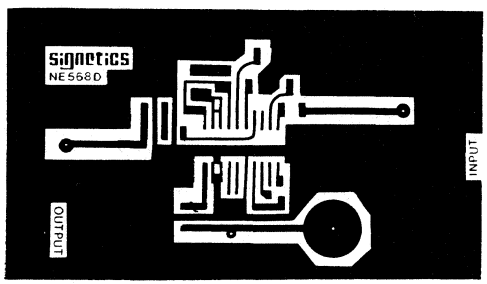
For the test circuit, R_1 was chosen to be 27Ω. The calculated value of C_{10} is 590pF; 560pF was chosen as a production value. (In actual satellite receiver applications, improved video with low carrier/noise has been observed with a wider loop-filter bandwidth.)

A typical application of the NE568 is demodulation of FM signals. In this mode of operation, a second single-pole filter is available at Pin 15 to minimize high frequency feedthrough to the output. The roll-off frequency is set by an internal resistor of 350Ω ±20%, and an external capacitor from Pin 15 to ground. The value of the capacitor is:

$$C11 = \frac{1}{2\pi\ (350)f_{BW}}\ F$$

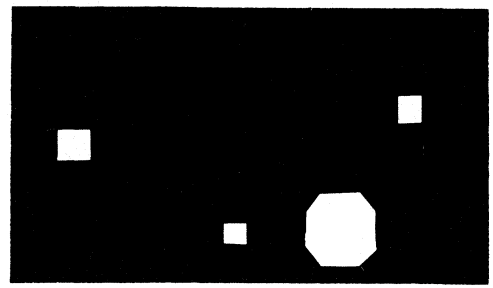
Two final components complete the active part of the circuitry. A resistor from Pin 12 to ground sets the temperature stability of the circuit, and a potentiometer from Pin 16 to ground permits fine tuning of the free-running oscillator frequency. The Pin 16 potentiometer is normally 1.2kΩ. Adjusting this resistance controls current sources which affect the charge and discharge rates of the timing capacitor and, thus, the frequency. The value of the temperature stability resistor is chosen from the graph in Figure 6; the respective timing capacitor needs to be changed.

The final consideration is bypass capacitors for the supply lines. The capacitors should be ceramic chips, preferably surface-mount types. They must be kept very close to the device. The capacitors from Pins 8 and 9 return to V_{CC1} before being bypassed with a separate capacitor to ground. This assures that no differential loops are created which might cause instability. The layouts for the test circuits are recommended.



DF07740S

a. Component Side Top of Board



DF07730S

b. Back of Board

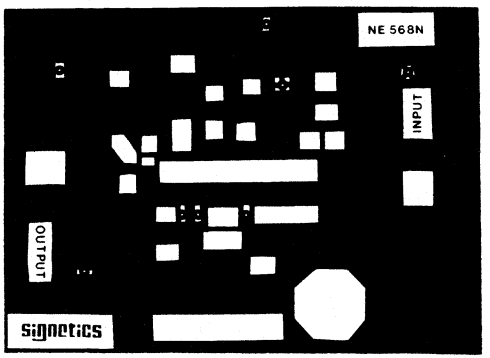
NOTES:
1. Board is laid out for King BNC Connector P/N KC-79-243-M06 or equivalent. Mount on bottom (back) of board. Add stand-off in each corner.
2. Back and top side ground must be connected at 8 point minimum.

Figure 2

PARTS LIST AND LAYOUT 70MHz APPLICATION NE568N

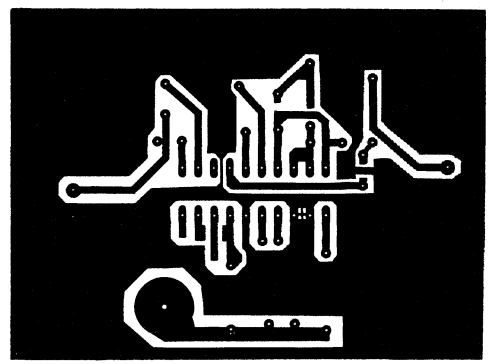
C_1	100nF	±10%	Ceramic chip	50V
C_2[1]	17pF	±2%	Ceramic OR chip	50V
C_2[2]	34pF	±2%	Ceramic chip	0805
C_3	100nF	±10%	Ceramic chip	50V
C_4	100nF	±10%	Ceramic chip	50V
C_5	6.8μF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic OR chip	50V
C_7	100nF	±10%	Ceramic chip	50V
C_8	100nF	±10%	Ceramic chip	50V
C_9	56pF	±2%	Ceramic chip	50V
C_{10}	560pF	±2%	Ceramic chip	50V
C_{11}	47pF	±2%	Ceramic OR chip	50V
C_{12}	100nF	±10%	Ceramic OR chip	50V
C_{13}	100nF	±10%	Ceramic OR chip	50V
R_1	27Ω	±10%	Carbon	¼W
R_2	1.2kΩ		Trim pot	
R_3[3]	43Ω	±10%	Carbon	¼W
R_4[4]	4.7kΩ	±10%	Carbon	¼W
R_5[3]	50Ω	±10%	Carbon	¼W
RFC_1	10μH	±10%		
RFC_2	10μH	±10%		

NOTES:
1. $C_2 + C_{STRAY} = 20pF$ for test configuration with $R_4 = 0\Omega$.
2. $C_2 = 34pF$ for temperature-compensated configuration with $R_4 = 4.7k\Omega$.
3. For 50Ω setup. $R_1 = 62\Omega$; $R_3 = 75\Omega$ for 75Ω applications.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 17pF$.



DF07750S

a. Component Side for Leaded Components



DF07760S

b. Solder Side of Board and Chip Capacitors

NOTES:
1. Board is laid out for King BNC Connector P/N KC-79-243-M06 or equivalent mounted on the component side of the board.
2. Component side and solder side ground planes must be connected at 8 points minimum.

Figure 3

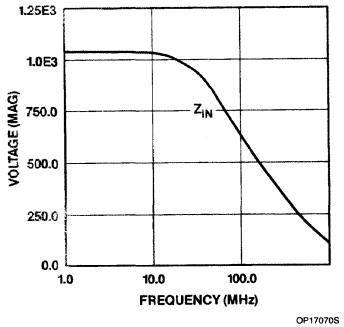


Figure 4. NE568 Input Impedance with CP = 0.5pF 20-Pin SO Package

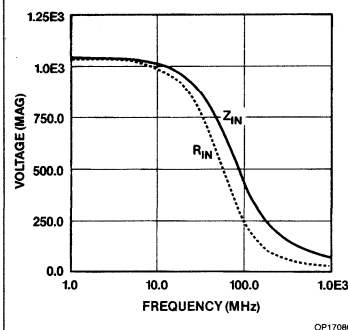


Figure 5. NE568 Input Impedance with CP = 1.49pF 20-Pin Dual In-Line Plastic Package

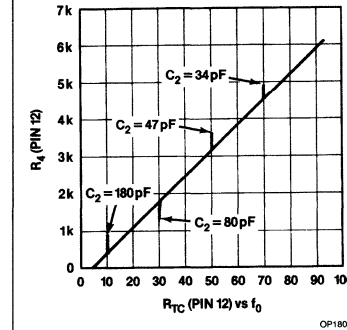


Figure 6

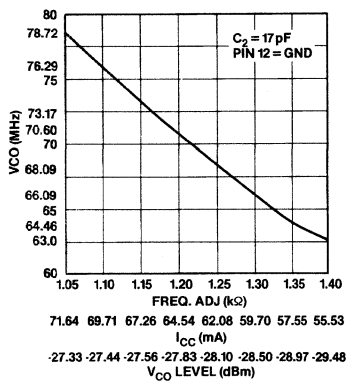


Figure 7. Typical VCO Frequency vs R_2 Adjustment

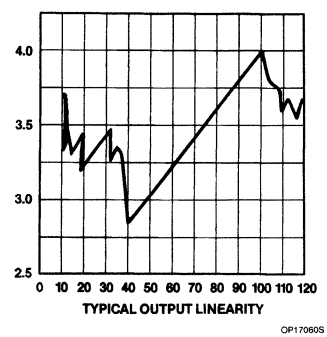


Figure 8. Typical Output Linearity

NE570/571/SA571
Compandor

Product Specification

Linear Products

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|_{avg}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|_{avg}}{R_1}$$

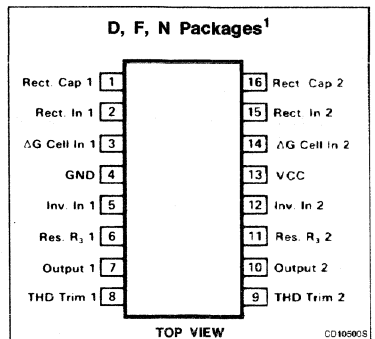
FEATURES

- **Complete compressor and expandor in one IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to $6V_{DC}$**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Cellular radio**
- **Telephone trunk compandor — 570**
- **Telephone subscriber compandor — 571**
- **High level limiter**
- **Low level expandor — noise gate**
- **Dynamic noise reduction systems**
- **Voltage-controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

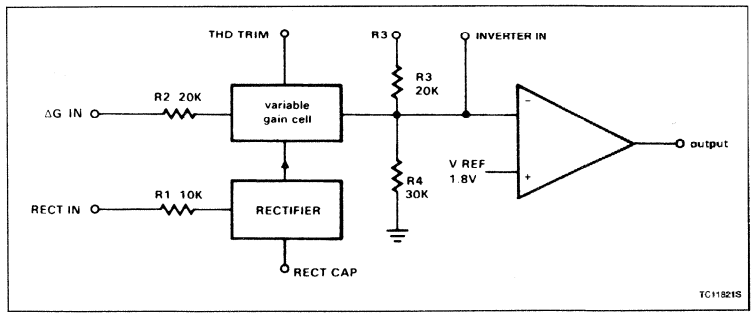


NOTE:
1. SOL - Released in Large SO Package Only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE570F
16-Pin Plastic DIP	0 to +70°C	NE570N
16-Pin Plastic SOL	0 to +70°C	NE571D
16-Pin Cerdip	0 to +70°C	NE571F
16-Pin Plastic Cerdip	0 to +70°C	NE571N
16-Pin Cerdip	-40°C to +85°C	SA571F
16-Pin Plastic DIP	-40°C to +85°C	SA571N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Positive supply 570 571	 24 18	V_{DC}
T_A	Operating ambient temperature range NE SA	 0 to +70 −40 to +85	 °C °C
P_D	Power dissipation	400	mW

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 15V$. Except where indicated, the 571 specifications are identical to those of the 570.

SYMBOL	PARAMETER	TEST CONDITIONS	NE570			NE/SA571[5]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		24	6		18	V
I_{CC}	Supply current	No signal		3.2	4.8		3.2	4.8	mA
I_{OUT}	Output current capability		±20			±20			mA
SR	Output slew rate			±.5			±.5		V/μs
	Gain cell distortion[2]	Untrimmed Trimmed		0.3 0.05	1.0		0.5 0.1	2.0	%
	Resistor tolerance			±5	±15		±5	±15	%
	Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
	Output DC shift[3]	Untrimmed		±20	±50		±30	±100	mV
	Expandor output noise	No signal, 15Hz − 20kHz[1]		20	45		20	60	μV
	Unity gain level		−1	0	+1	−1.5	0	+1.5	dBm
	Gain change[2, 4]	−40°C < T < 70°C 0°C < T < 70°C		±0.1 ±0.1	 ±0.2		±0.1 ±0.1	 ±0.4	dB
	Reference drift[4]	−40°C < T < 70°C 0°C < T < 70°C		+2, −25 ±5	+10, −40 ±10		+2, −25 ±5	+20, −50 ±20	mV
	Resistor drift[4]	−40°C < T < 70°C 0°C < T < 70°C		+8, −0 +1.−0					%
	Tracking error (measured relative to value at unity gain) equals [$V_O - V_O$ (unity gain)] dB − V_2dBm	Rectifier input, V_2 = +6dBm, V_1 = 0dB V_2 = −30dBm, V_1 = 0dB		±0.2 +0.2	 −0.5, +1		 +0.2	 −1, +1.5	dB
	Channel separation			60			60		dB

NOTES:
1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor AC input change from no signal to 0dBm.
4. Relative to value at $T_A = 25°C$.
5. Electrical characteristics for the SA571 only are specified over −40 to +85°C temperature range.

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\, e^{-t/\tau} + G_{final;}\ \tau = 10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

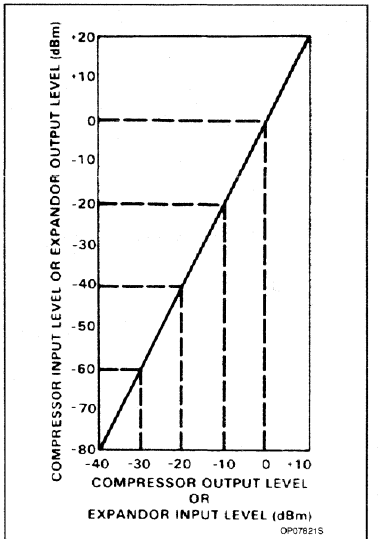
The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

The output stage is capable of ± 20mA output current. This allows a +13dBm ($3.5V_{RMS}$) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

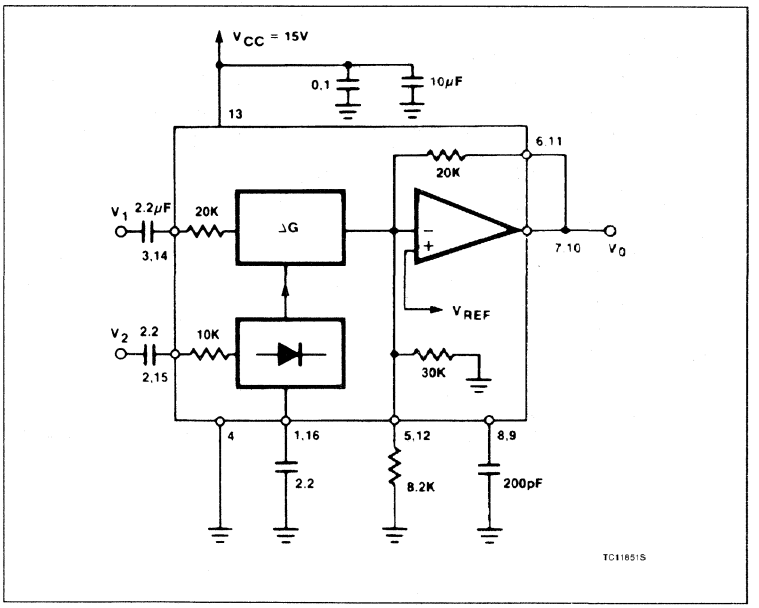
The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS



Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT



INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components. This paper describes an inexpensive integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (< 0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to −80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expandor are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

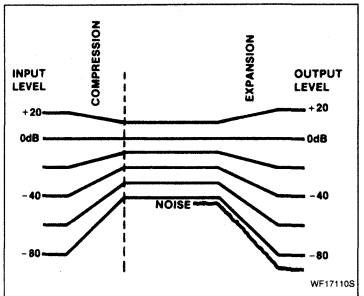


Figure 1. Restricted Dynamic Range Channel

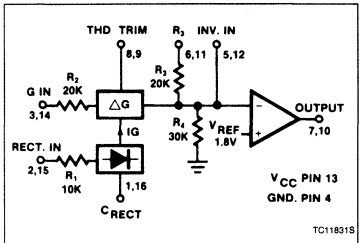


Figure 2. Chip Block Diagram (1 of 2 Channels)

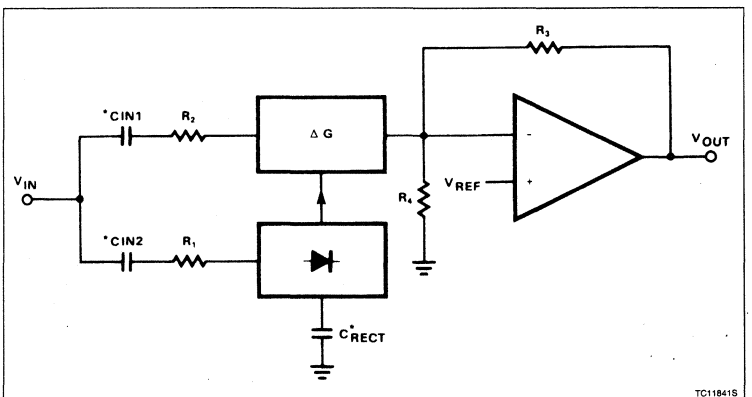
The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap reference provides a very stable, low noise 1.8V reference denoted V_{REF}. The non-inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2-to-1 expansion.

Figure 4 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\ DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

$$V_{REF} = \left(1 + \frac{R_{DC\ TOT}}{30k}\right) 1.8V$$



NOTES:

$$GAIN = \frac{2\ R_3\ V_{IN}\ (avg.)}{R_1\ R_2\ I_B}$$

$I_B = 140\mu A$

*External components

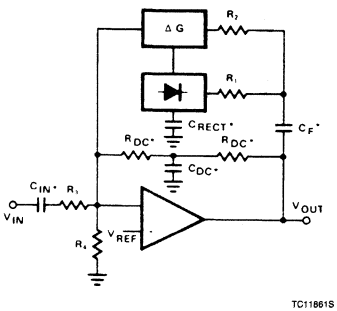
Figure 3. Basic Expandor

The output of the expandor will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4}\ V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k}\right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.



NOTES:

$$GAIN = \left(\frac{R_1 R_2 I_B}{2 R_3 V_{IN}\ (avg)}\right)^{1/2}$$

$I_B = 140\mu A$
*external components

Figure 4. Basic Compressor

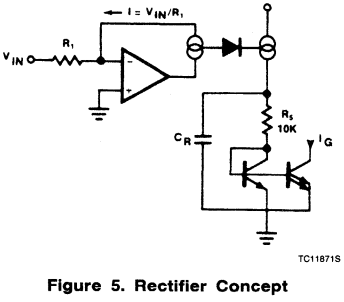
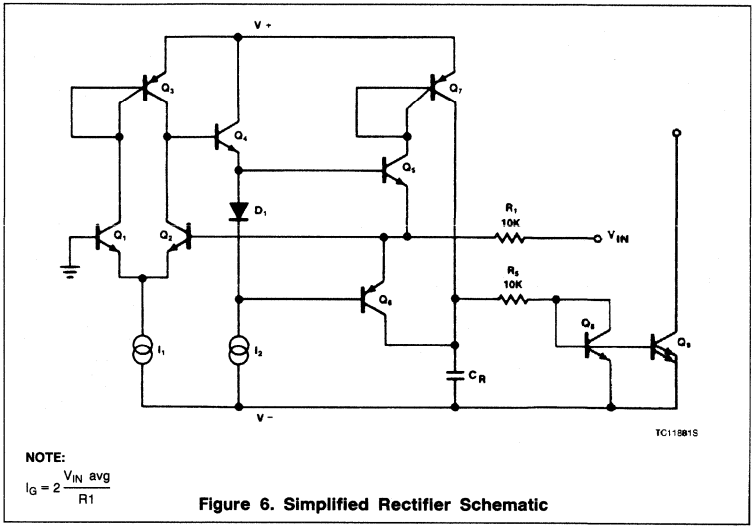


Figure 5. Rectifier Concept

CIRCUIT DETAILS — RECTIFIER

Figure 5 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.



NOTE:

$$I_G = 2\frac{V_{IN}\ avg}{R1}$$

Figure 6. Simplified Rectifier Schematic

Figure 6 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the α of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The α's of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

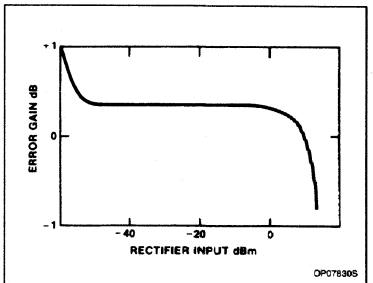


Figure 7. Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, −20dBm, and −40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

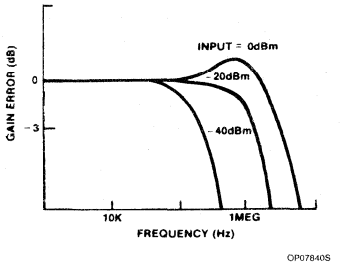


Figure 8. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linearized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} ($= V_{IN}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1} = I_1 + I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

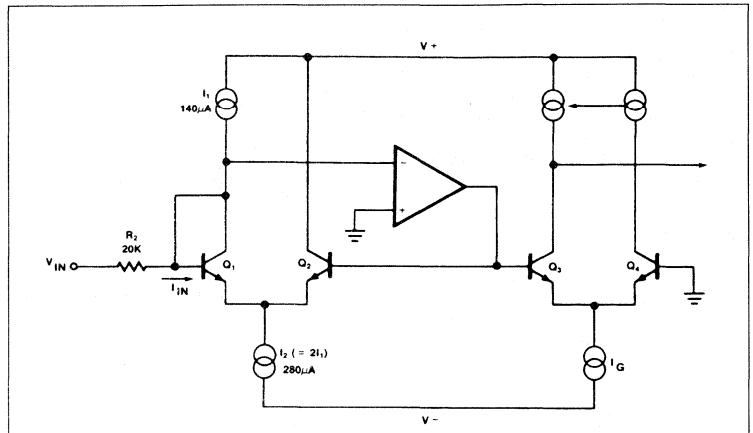
$$I_2 - (I_1 + I_{IN}) = I_1 - I_{IN} = I_{C2}.$$

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G = I_{C3} + I_{C4}$ and $I_{OUT} = I_{C4} - I_{C3}$ will yield the multiplier transfer function,



NOTE:

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{I_G V_{IN}}{I_2 R_2}$$

Figure 9. Simplified ΔG Cell Schematic

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN}}{R_2} \frac{I_G}{I_1}.$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.

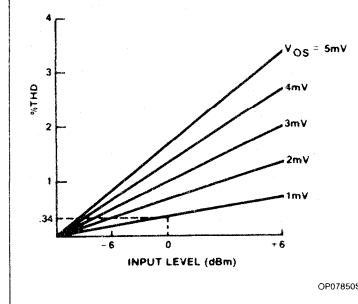


Figure 10. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 10 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about ½mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

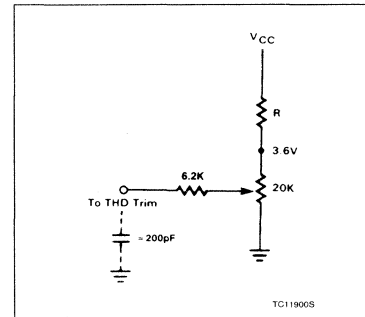


Figure 11. THD Trim Network

Figure 12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 13 shows such a trim network.

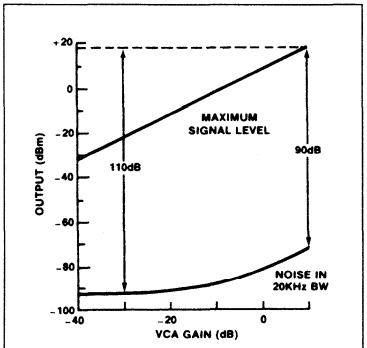


Figure 12. Dynamic Range of NE570

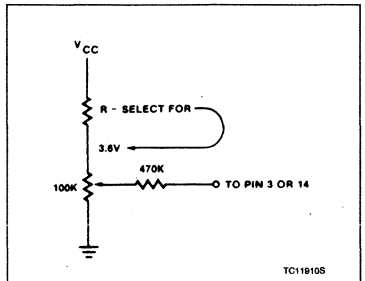


Figure 13. Control Signal Feedthrough Trim

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 14 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

RESISTORS

Inspection of the gain equations in Figures 3 and 4 will show that the basic compressor and expandor circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made 1/7 the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

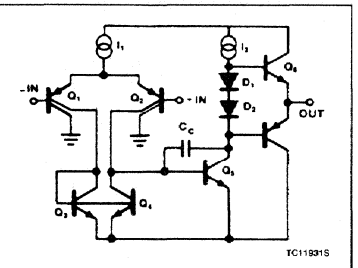


Figure 14. Operational Amplifier

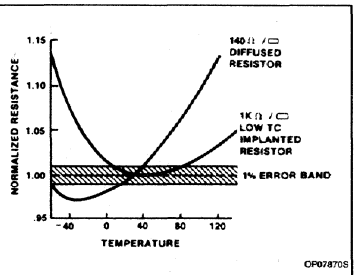


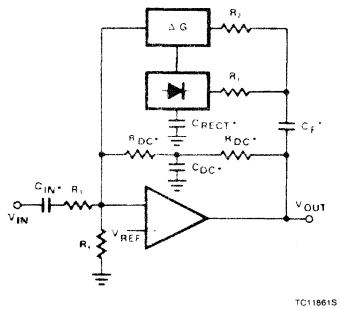
Figure 15. Resistance vs Temperature

The output of the expandor will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4}\ V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k} \right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.



NOTES:

$$GAIN = \left(\frac{R_1 R_2 I_B}{2 R_3 V_{IN}\ (avg)} \right)^{1/2}$$

$I_B = 140\mu A$

*external components

Figure 4. Basic Compressor

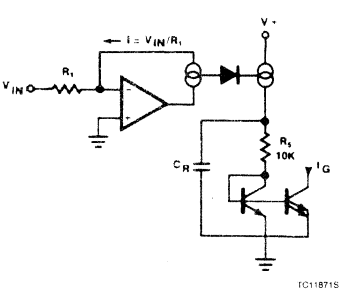


Figure 5. Rectifier Concept

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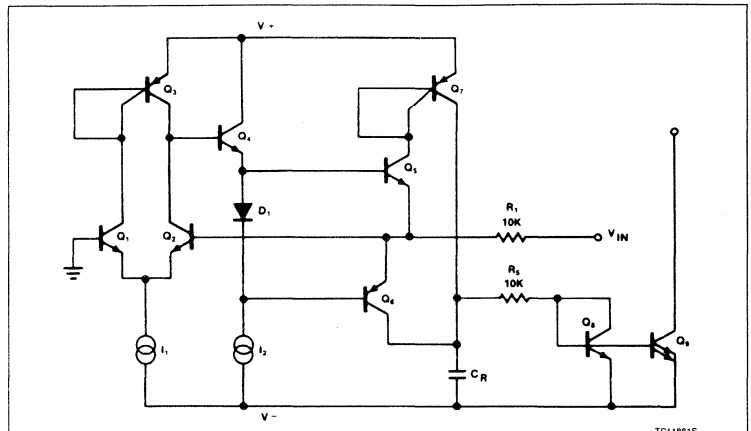

NOTE:

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Figure 6. Simplified Rectifier Schematic

Figure 6 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the α of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The α's of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

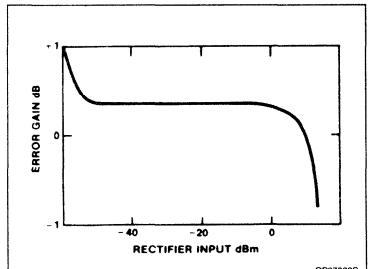


Figure 7. Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

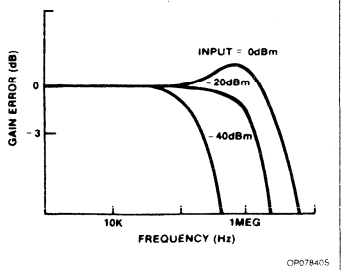


Figure 8. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linerarized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} ($= V_{IN}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1} = I_1 + I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

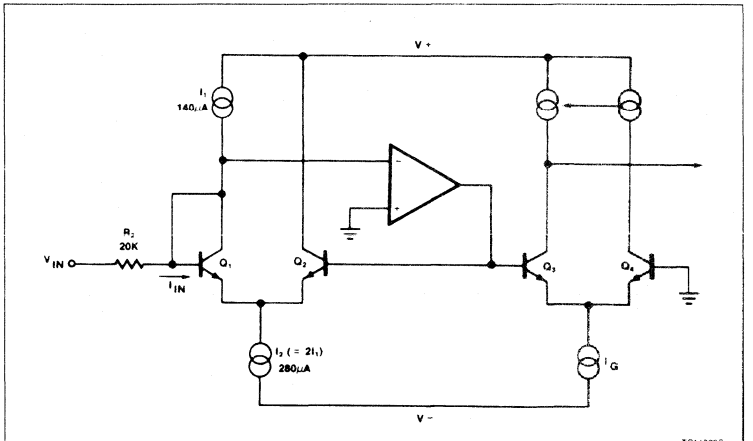
$$I_2 - (I_1 + I_{IN}) = I_1 - I_{IN} = I_{C2}.$$

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G = I_{C3} + I_{C4}$ and $I_{OUT} = I_{C4} - I_{C3}$ will yield the multiplier transfer function,



NOTE:

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{I_G\ V_{IN}}{I_2\ R_2}$$

Figure 9. Simplified ΔG Cell Schematic

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN}\ I_G}{R_2\ I_1}.$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.

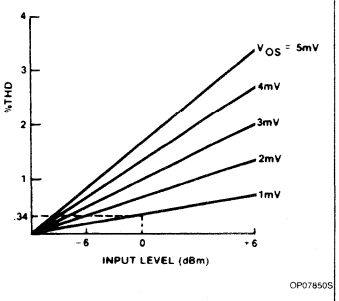


Figure 10. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 10 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about ½mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

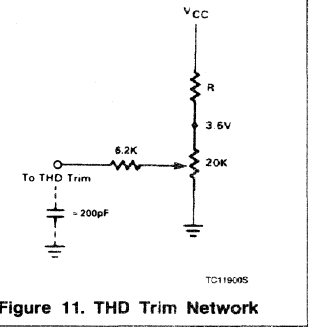


Figure 11. THD Trim Network

NE/SA572
Programmable Analog Compandor

Product Specification

DESCRIPTION

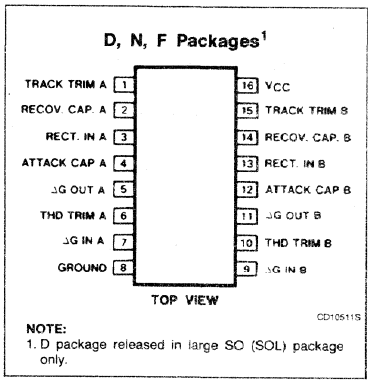
The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- **Independent control of attack and recovery time**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external op amp**
- **Wide dynamic range — greater than 110dB**
- **Temperature-compensated gain control**
- **Low distortion gain cell**
- **Low noise — 6μV typical**
- **Wide supply voltage range — 6V – 22V**
- **System level adjustable with external components**

PIN CONFIGURATION



NOTE:
1. D package released in large SO (SOL) package only.

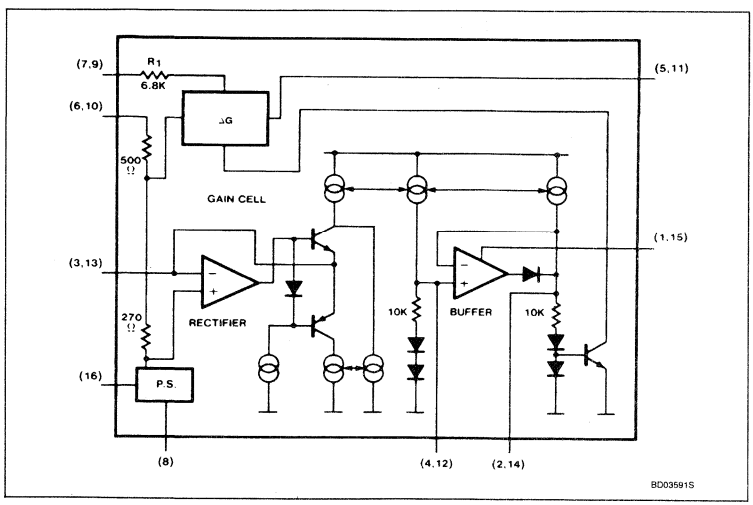
APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High-level limiter**
- **Low-level noise gate**
- **State variable filter**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE572D
16-Pin Plastic DIP	0 to +70°C	NE572N
16-Pin Plastic SO	−40°C to +85°C	SA572D
16-Pin Cerdip	−40°C to +85°C	SA572F
16-Pin Plastic DIP	−40°C to +85°C	SA572N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

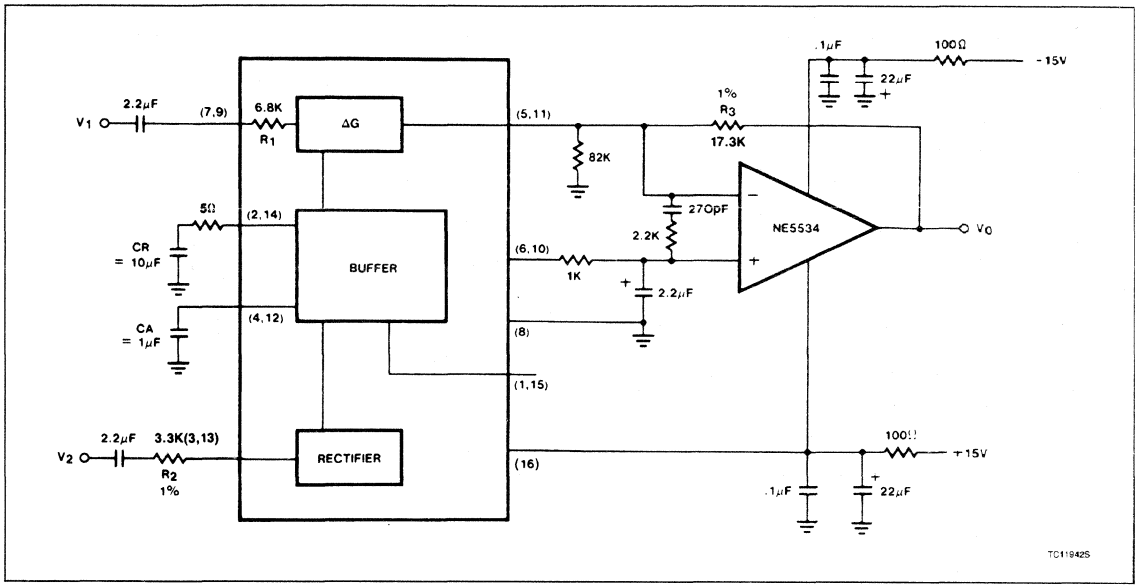
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	V_{DC}
T_A	Operating temperature range NE572 SA572	 0 to +70 -40 to +85	°C
P_D	Power dissipation	500	mW

DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) V_{CC} = 15V, T_A = 25°C; Expandor mode (see Test Circuit). Input signals at unity gain level (0dB) = 100mV_{RMS} at 1kHz; $V_1 = V_2$; R_2 = 3.3kΩ; R_3 = 17.3kΩ.

SYMBOL	PARAMETER	TEST CONDITIONS	NE572			SA572			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		22	6		22	V_{DC}
I_{CC}	Supply current	No signal			6			6.3	mA
V_R	Internal voltage reference		2.3	2.5	2.7	2.3	2.5	2.7	V_{DC}
THD	Total harmonic distortion (untrimmed)	1kHz C_A = 1.0μF		0.2	1.0		0.2	1.0	%
THD	Total harmonic distortion (trimmed)	1kHz C_R = 10μF		0.05			0.05		%
THD	Total harmonic distortion (trimmed)	100Hz		0.25			0.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20 - 20kHz)		6	25		6	25	μV
	DC level shift (untrimmed)	Input change from no signal to 100mV_{RMS}		±20	±50		±20	±50	mV
	Unity gain level		-1	0	+1	-1.5	0	+1.5	dB
	Large-signal distortion	$V_1 = V_2$ = 400mV		0.7	3.0		0.7	3	%
	Tracking error (measured relative to value at unity gain) = $[V_O - V_O$ (unity gain)]dB $- V_2$dB	Rectifier input V_2 = +6dB V_1 = 0dB V_2 = -30dB V_1 = 0dB		 ±0.2 ±0.5	 -1.5 +0.8		 ±0.2 ±0.5	 -2.5 +1.6	dB
	Channel crosstalk	200mV_{RMS} into channel A, measured output on channel B	60			60			dB
PSRR	Power supply rejection ratio	120Hz		70			70		dB

TEST CIRCUIT



AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10k resistor R_A defines the attack time t_A. The recovery time t_R of a tone burst is defined by a recovery capacitor C_R and an internal 10k resistor R_R. Typical attack time of 4ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1μF and 1.0μF attack capacitors, respectively. Recovery time of 200ms can be obtained with a 4.7μF external capacitor. With the recovery capacitor added in the level sensor, the gain control ripple for low frequency signals is much lower than that of a simple RC ripple filter. As a result, the residual third harmonic distortion of low frequency signal in a two quad transconductance amplifier is greatly improved. With the 1.0μF attack capacitor and 4.7μF recovery capacitor for a 100Hz signal, the third harmonic distortion is improved by more than 10dB over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0 – 70°C. The SA572 is intended for applications from −40°C to +85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of $Q_1 - Q_2$ and the V_{BE} of $Q_3 - Q_4$ equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\triangle V_{BEQ3-Q4} = \triangle_{BEQ1-Q2}$$

$$(V_{BE} = V_T \ln IC/IS)$$

$$V_T \ln\left(\frac{\frac{1}{2}I_G + \frac{1}{2}I_O}{I_S}\right) - V_T \ln\left(\frac{\frac{1}{2}I_G - \frac{1}{2}I_O}{I_S}\right)$$

$$= V_T \ln\left(\frac{I_1 + I_{IN}}{I_S}\right) - V_T \ln\left(\frac{I_2 - I_1 - I_{IN}}{I_S}\right) \quad (2)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$

$I_1 = 140\mu A$

$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \quad (3)$$

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within ±25μA into the THD trim pin.

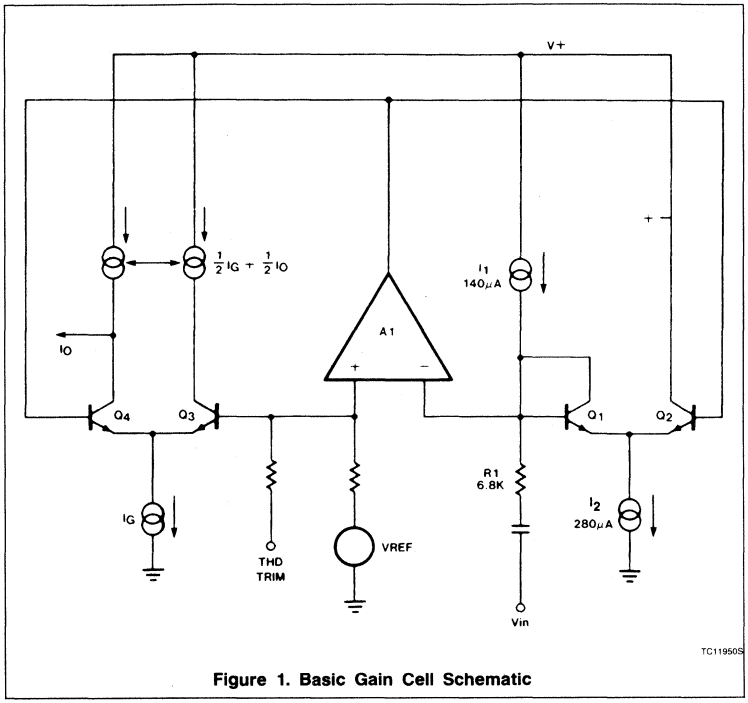


Figure 1. Basic Gain Cell Schematic

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only 6μV in the audio spectrum (10Hz – 20kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2. The input bias current is typically about 70nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \quad (4)$$

If V_{IN} is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN(AVG)}}{R_2}$$

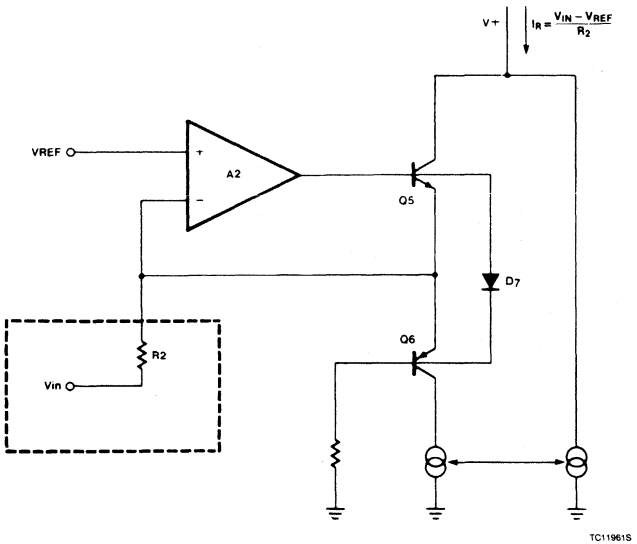


Figure 2. Simplified Rectifier Schematic

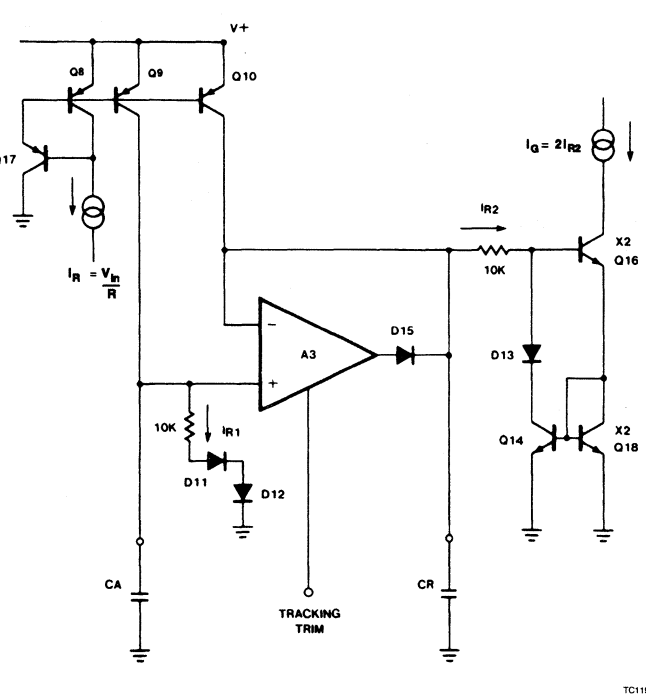


Figure 3. Buffer Amplifier Schematic

The internal bias scheme limits the maximum output current I_R to be around 300μA. Within a ±1dB error band the input range of the rectifier is about 52dB.

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common-mode bias for A_3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) = (Ga_{INT} - Ga_{FNL})\ e^{\frac{-t}{\tau_A}} + Ga_{FNL}$$

Ga_{INT} = Initial Gain

Ga_{FNL} = Final Gain

$\tau_A = R_A \cdot CA = 10k \cdot CA$

where τ_A is the attack time constant and R_A is a 10k internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR · R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{R\ INT} - G_{R\ FNL})\ e^{\frac{-t}{\tau_R}} + G_{R\ FNL}$$

$\tau R = R_R \cdot CR = 10k \cdot CR$

where τR is the recovery time constant and R_R is a 10k internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim pin into A_3 with a current source of ±3μA.

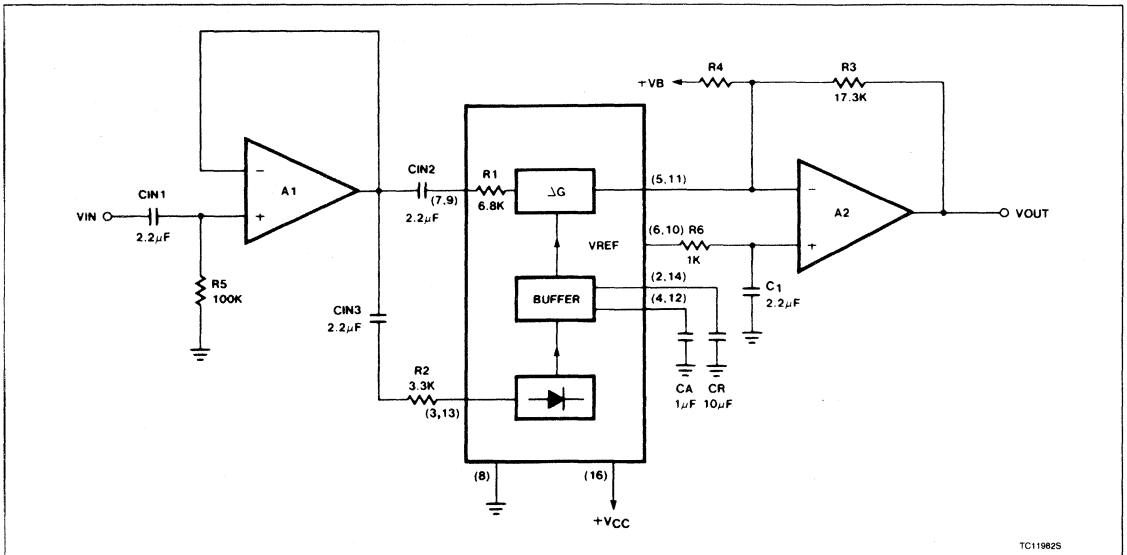


Figure 4. Basic Expandor Schematic

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \quad (5)$$

($I_1 = 140\mu A$)

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as $140\mu A$. This corresponds to a voltage level of $140\mu A \cdot 6.8k = 952mV$ peak. The input peak current into the rectifier is limited to $300\mu A$ by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B \frac{R_3}{R_4} \quad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}} \right)^{1/2} \quad (7)$$

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF} \left(1 + \frac{R_{DC1} + R_{DC2}}{R_4} \right) - V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4} \right) \quad (8)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

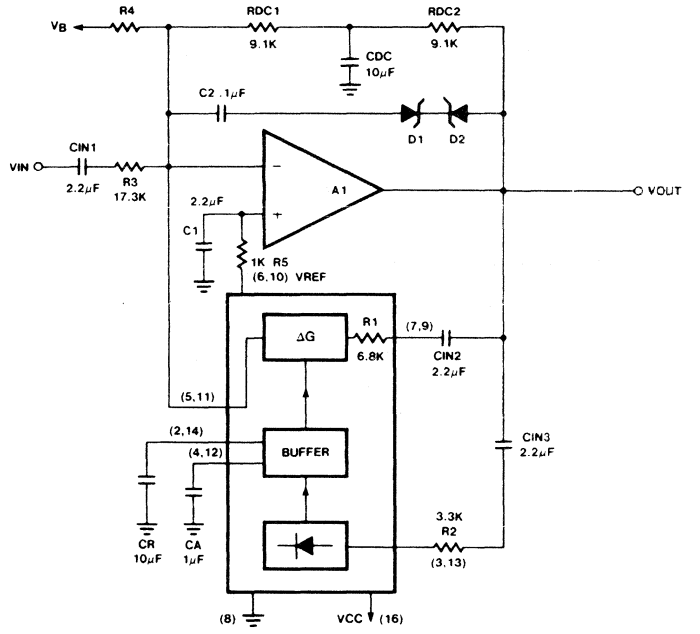


Figure 5. Basic Compressor Schematic

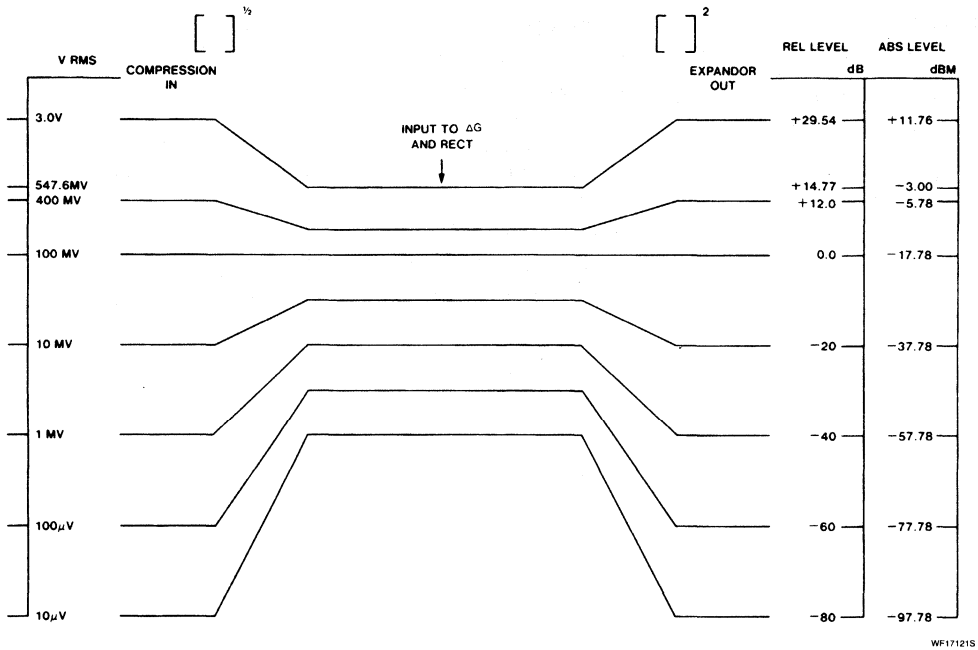


Figure 6. NE572 System Level

Document	853–1119
ECN No.	96727
Date of Issue	May 30, 1989
Status	Product Specification
RF Communications	

NE/SA575

Low voltage compandor

DESCRIPTION

The NE/SA575 is a precision dual gain control circuit designed for low voltage applications. The NE575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

FEATURES

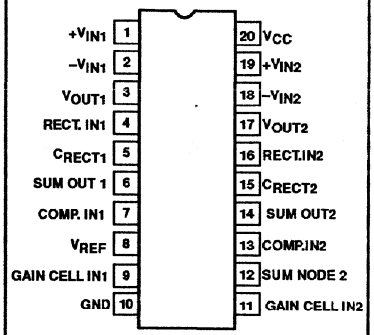
- Operating voltage range from 3V to 7V
- Reference voltage of $100mV_{RMS}$ = 0dB
- One dedicated summing op amp per channel and two extra uncommitted op amps
- 600Ω drive capability
- Single or split supply operation
- Wide input/output swing capability

APPLICATIONS

- Portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Portable broadcast mixers
- Wireless microphones
- Modems
- Electric organs
- Hearing aids

PIN CONFIGURATION

D[1] and N Packages



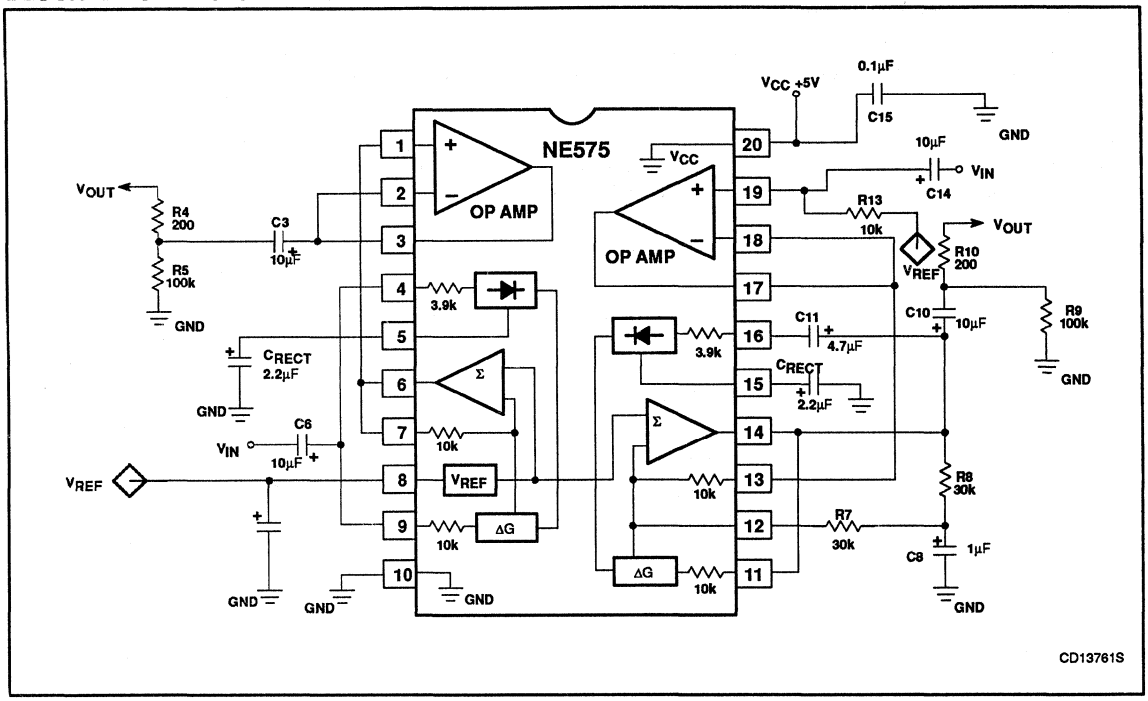
NOTE:
1. Available in large SOL package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE575N
20-Pin Plastic SOL	0 to +70°C	NE575D
20-Pin Plastic DIP	–40 to +85°C	SA575N
20-Pin Plastic SOL	–40 to +85°C	SA575D

Low voltage compandor NE/SA575

BLOCK DIAGRAM and TEST CIRCUIT



Low voltage compandor — NE/SA575

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE575	SA575	
V_{CC}	Single supply voltage	8	8	V
T_A	Operating ambient temperature range	–40 to +85	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP	68	68	°C/W
	SOL	112	112	°C/W

DC ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 25°C. Minimum and Maximum values are for the full operating temperature range: 0 to 70°C for NE575, –40 to +85°C for SA575. V_{CC} = 5V, unless otherwise stated. Both channels are tested in the Expandor mode (see Test Circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575			SA575			
			MIN	TYP	MAX	MIN	TYP	MAX	
For compandor, including summing amplifier									
V_{CC}	Supply voltage[1]		3	5	7	3	5	7	V
I_{CC}	Supply current	No signal	3	4.2	5.5	3	4.2	5.5	mA
V_{REF}	Reference voltage[2]	V_{CC} = 5V	2.4	2.5	2.6	2.4	2.5	2.6	V
R_L	Summing amp output load		10			10			kΩ
THD	Total harmonic distortion	1kHz, 0dB BW = 3.5kHz		0.12	1.0		0.12	1.5	%
E_{NO}	Output voltage noise	BW = 20kHz, R_S = 0Ω		6	20		6	30	μV
0dB	Unity gain level	1kHz	–1.0		1.0	–1.5		1.5	dB
V_{OS}	Output voltage offset	No signal	–100		100	–150		150	mV
	Output DC shift	No signal to 0dB	–50		50	–100		100	mV
	Tracking error relative to 0dB	Gain cell input = 0dB, 1kHz Rectifier input = 6dB, 1kHz	–0.5		0.5	–1.0		1.0	dB
		Gain cell input = 0dB, 1kHz Rectifier input = –30dB, 1kHz	–0.5		0.5	–1.0		1.0	dB
	Crosstalk	1kHz, 0dB, C_{REF} = 220μF		–80	–65		–80	–65	dB
For operational amplifier									
V_O	Output swing	R_L = 10kΩ	V_{CC}–0.4	V_{CC}–0.2		V_{CC}–0.4	V_{CC}–0.2		V
R_L	Output load	1kHz	600			600			Ω
CMR	Input common–mode range		0		V_{CC}	0		V_{CC}	V
CMRR	Common–mode rejection ratio		60	80		60	80		dB
I_B	Input bias current	V_{IN} = 0.5V to 4.5V	–0.5		0.5	–1		1	μA
V_{OS}	Input offset voltage			3			3		mV
A_{VOL}	Open–loop gain	R_L = 10kΩ		80			80		dB
SR	Slew rate	Unity gain		1			1		V/μs
GBW	Bandwidth	Unity gain		3			3		MHz
E_{NI}	Input voltage noise	BW = 20kHz		2.5			2.5		μV
PSRR	Power supply rejection ratio	1kHz, 250mV		60			60		dB

NOTES:
1. Operation down to V_{CC} = 2V is possible, but performance is significantly reduced. See curve in Figure 5.
2. Reference voltage, V_{REF}, is typically at 1/2V_{CC}.

Low voltage compandor NE/SA575

FUNCTIONAL DESCRIPTION

This section describes the basic subsystems and applications of the NE/SA575 Compandor. More theory of operation on compandors can be found in AN174 and AN176. The typical applications of the NE575 low voltage compandor in an Expandor (1:2), Compressor (2:1) and Automatic Level Control (ALC) function are explained. These three circuit configurations are shown in Figures 1, 2, 3 respectively.

The NE575 has two channels for a complete companding system. The left channel, A, can be configured as a 1:2 Expandor while the right channel, B, can be configured as either a 2:1 Compressor, a 1:2 Expandor or an ALC. Each channel consists of the basic companding building blocks of rectifier cell, variable gain cell, summing amplifier and V_{REF} cell. In addition, the NE575 has two additional high performance uncommitted op amps which can be utilized for application such as filtering, pre–emphasis/de–emphasis or buffering.

Figure 4 shows the complete schematic for the applications demo board. Channel A is configured as an expandor while channel B is configured so that it can be used either as a compressor or as an ALC circuit. The switch, S1, toggles the circuit between compressor and ALC mode. Jumpers J1 and J2 can be used to either include the additional op amps for signal conditioning or exclude them from the signal path. Bread boarding space is provided for R1, R2, C1, C2, R10, R11, C10 and C11 so that the response can be tailored for each individual need. The components as specified are suitable for the complete audio spectrum from 20Hz to 20kHz.

The most common configuration is as a unity gain non–inverting buffer where R1, C1, C2, R10, C10 and C11 are eliminated and R2 and R11 are shorted. Capacitors C3, C5, C8, and C12 are for DC blocking, and R4 and R8 provide termination (for the capacitors). In systems where the inputs and outputs are AC coupled, these capacitors and resistors can be eliminated. Capacitors C4 and C9 are for setting the attack and release time constant.

C6 is for decoupling and stabilizing the voltage reference circuit. The value of C6 should be such that it will offer a very low impedance to the lowest frequencies of interest. Too small a capacitor will allow supply ripple to modulate the audio path. The better filtered the power supply, the smaller this capacitor can be. R5 and R12 provide DC reference voltage to the amplifiers of channel B. R6 and R7 provide a DC feedback path for the summing amp of channel B, while C7 is a short–circuit to ground for signals. C14 and C15 are for power supply decoupling. C14 can also be eliminated if the power supply is well regulated with very low noise and ripple. Figure 8 shows the PC board layout of the applications demo board.

DEMONSTRATED PERFORMANCE

The applications demo board was built and tested for a frequency range of 20Hz to 20kHz with the component values as shown in Figure 4 and V_{CC} = 5V. In the expandor mode, the typical input dynamic range was from –34dB to +12dB where 0dB is equal to $100mV_{RMS}$. The typical unity gain level measured at 0dB @ 1kHz input was ±0.5dB and the typical tracking error was ±0.1dB for input range of –30 to +10dB.

In the compressor mode, the typical input dynamic range was from –42dB to ±18dB with a tracking error +0.1dB and the typical unity gain level was ±0.5dB.

In the ALC mode, the typical input dynamic range was from –42dB to +8dB with typical output deviation of ±0.2dB about the nominal output of 0dB. For input greater than +9dB in ALC configuration, the summing amplifier sometimes exhibits high frequency oscillations. There are several solutions to this problem. The first is to lower the values of R7 and R8 to 20kΩ each. the second is to add a current limiting resistor in series with C13 at Pin 13. the third is to add a compensating capacitor of about 22 to 30pF between the input and output of summing amplifier (Pins 12 and 14). With any one of the above recommendations, the typical ALC mode input range increased to +18dB yielding a dynamic range of over 60dB.

EXPANDOR

The typical expandor configuration is shown in Figure 1. The variable gain cell and the rectifier cell are in the signal input path. The V_{REF} is always 1/2 V_{CC} to provide the maximum headroom without clipping. The 0dB ref is $100mV_{RMS}$. The input is AC coupled through C5, and the output is AC coupled through C3. If in a system the inputs and outputs are AC coupled, then C3, C5, R3 and R4 can be eliminated, thus requiring only one external component, C4. The variable gain cell and rectifier cell are DC coupled so any offset voltage between Pins 4 and 9 will cause small offset error current in the rectifier cell. This will affect the accuracy of the gain cell. This can be improved by using an extra capacitor from the input to Pin 4 and eliminating the DC connection between Pins 4 and 9.

The expandor gain expression and the attach and release time constant is given by Equation 1 and Equation 2, respectively.

Equation 1.

$$\text{Expandor gain} = \frac{4V_{IN}(avg)}{3.9k \times 100\mu A}$$

where $V_{IN}(avg) = 0.975V_{IN(RMS)}$

Equation 2.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

COMPRESSOR

The typical compressor configuration is shown in Figure 2. In this mode, the rectifier cell and variable gain cell are in the feedback path. R6 and R7 provide the DC feedback to the summing amplifier. The input is AC coupled through C12 and output is AC coupled through C8. In a system with inputs and outputs AC coupled, C8, C12, R8, and R9 could be eliminated and only R5, R6, R7, C7, and C13 would be required. If the external components R5, R6, R7 and C7 are eliminated, then the output of the summing amplifier will motor–boat in absence of signals or at extremely low signals. This is because there is no DC feedback path from the output to input. In the presence of an AC signal this phenomenon is not observed and the circuit will appear to function properly.

The compressor gain expression and the attack and release time constant is given by Equation 3 and Equation 4, respectively.

Equation 3.

$$\text{Compressor gain} = \left[\frac{3.9k \times 100\mu A}{4V_{IN(avg)}}\right]^{1/2}$$

where $V_{IN}(avg) = 0.975V_{IN(RMS)}$

Equation 4.

$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$

AUTOMATIC LEVEL CONTROL

The typical Automatic Level Control circuit configuration is shown in Figure 3. It can be seen that it is quite similar to the compressor schematic except that the input to the rectifier cell is from the input path and not from the feedback path. The input is AC coupled through C12 and C13 and the output is AC coupled through C8. Once again, as in the previous cases, if the system input and output signals are already AC coupled, then C12, C13, C8, R8 and R9 could be eliminated. Concerning the compressor, removing R5, R6, R7 and C7 will cause motor–boating in absence of signals. C_{COMP} is necessary to stabilize the summing amplifier at higher input levels. This circuit provides an input dynamic range greater than 60dB with the output within ±0.5dB typical. The necessary design expressions are given by Equation 5 and Equation 6, respectively.

Equation 5.

$$\text{ALC gain} = \frac{3.9k \times 100\mu A}{4V_{IN(avg)}}$$

Equation 6.

$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C9$

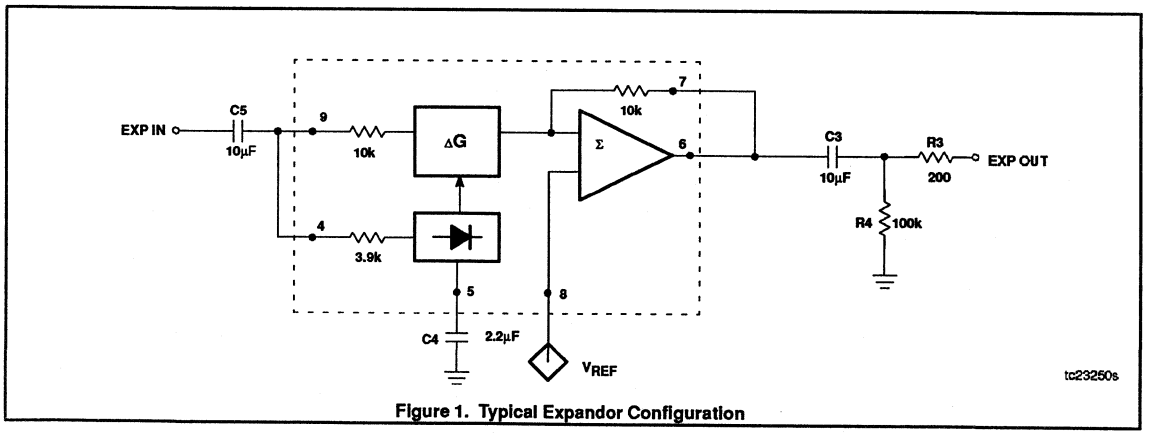


Figure 1. Typical Expandor Configuration

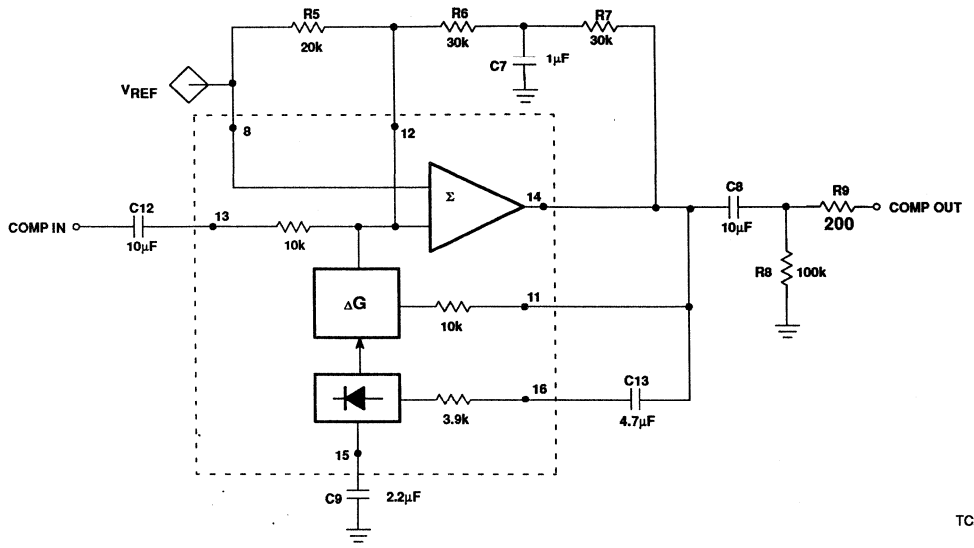


Figure 2. Typical Compressor Configuration

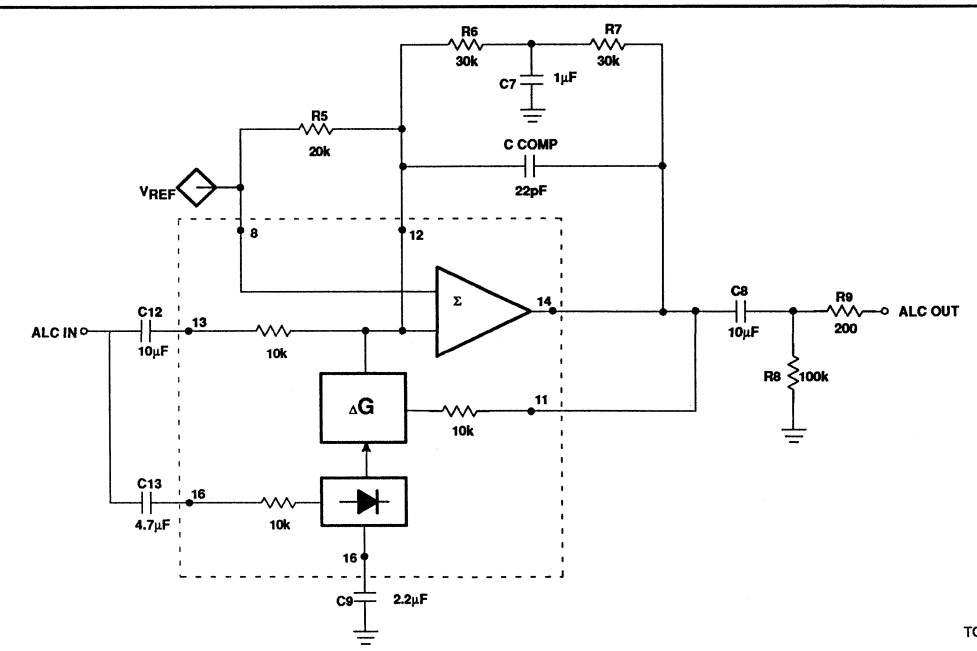


Figure 3. Typical ALC Configuration

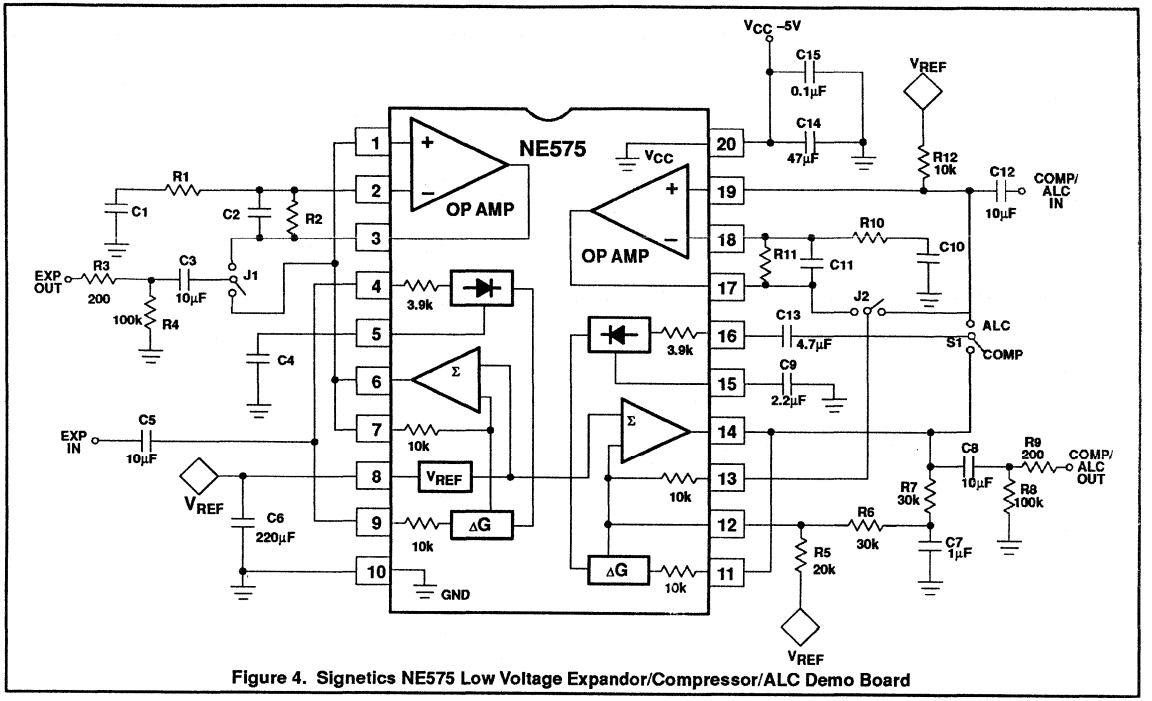


Figure 4. Signetics NE575 Low Voltage Expandor/Compressor/ALC Demo Board

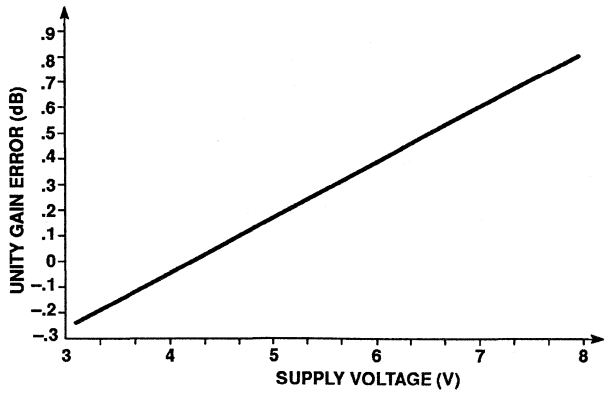


Figure 5. Unity Gain Error vs Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

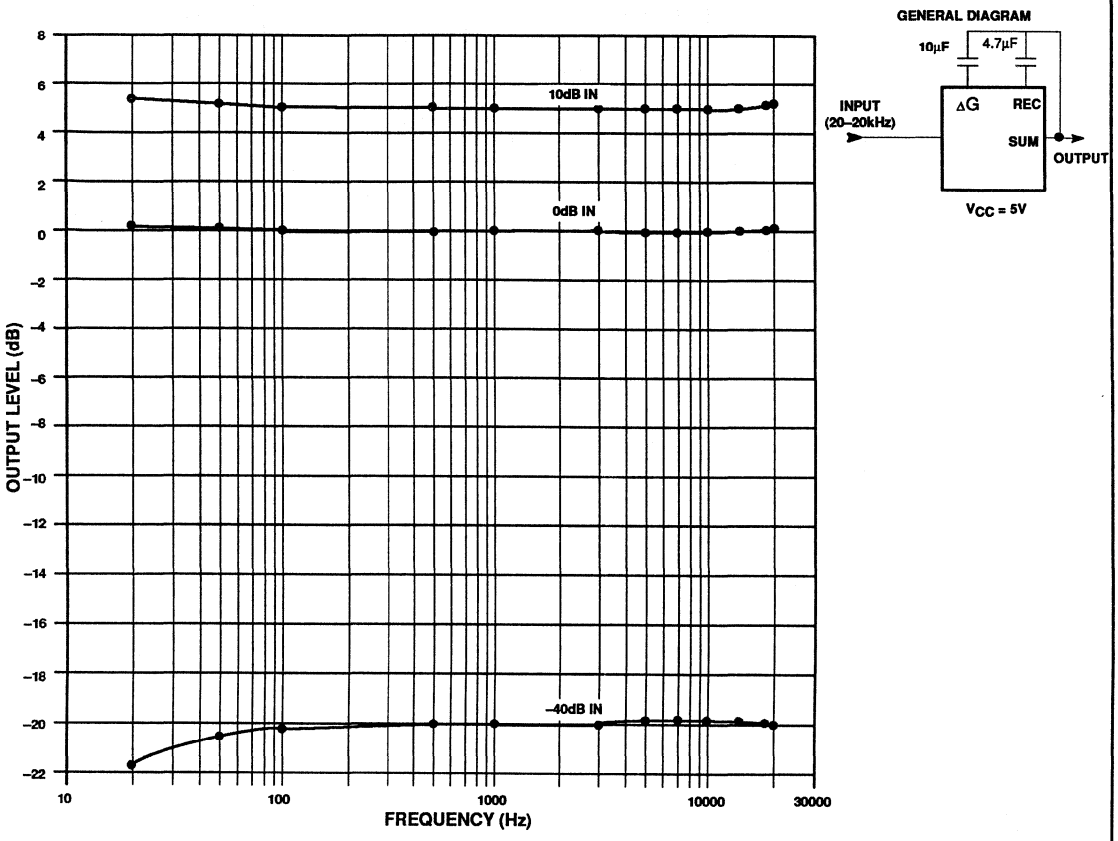


Figure 6. Compressor Output Frequency Response

Low voltage compandor NE/SA575

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

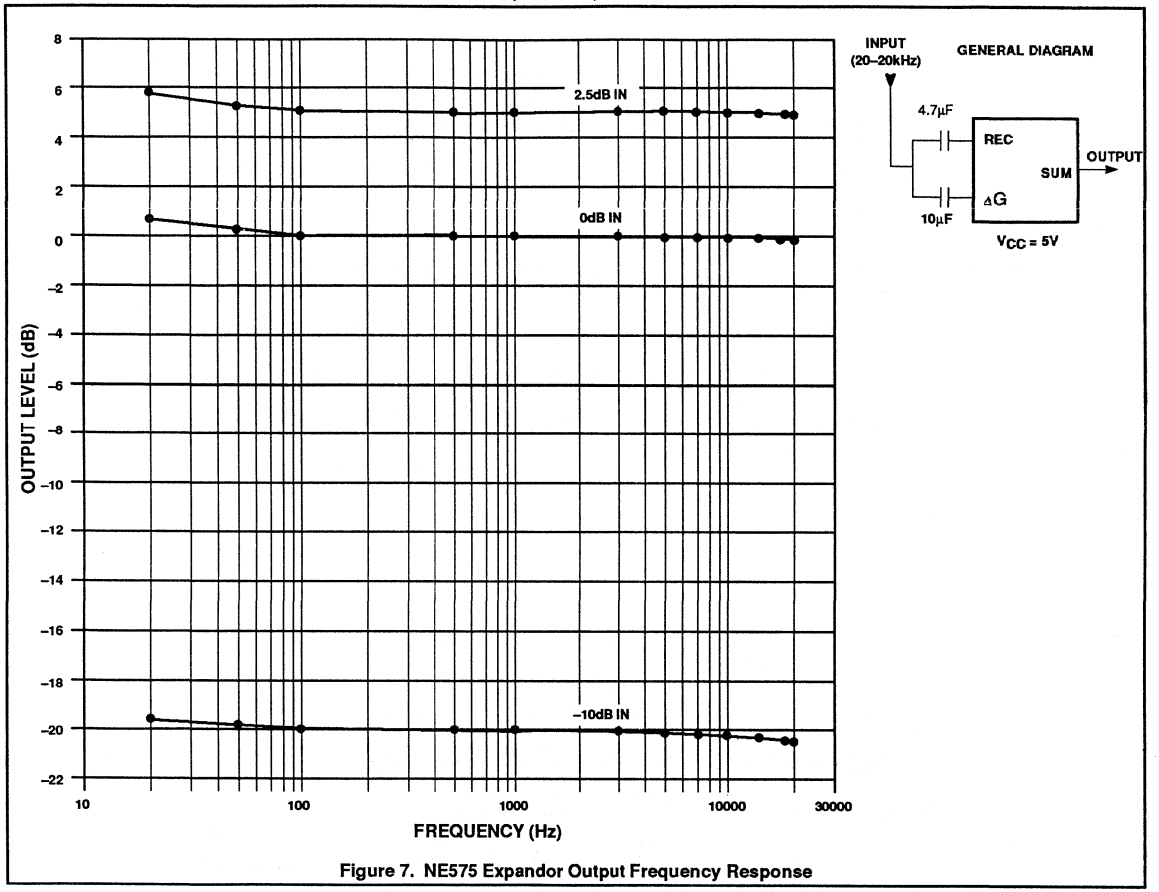
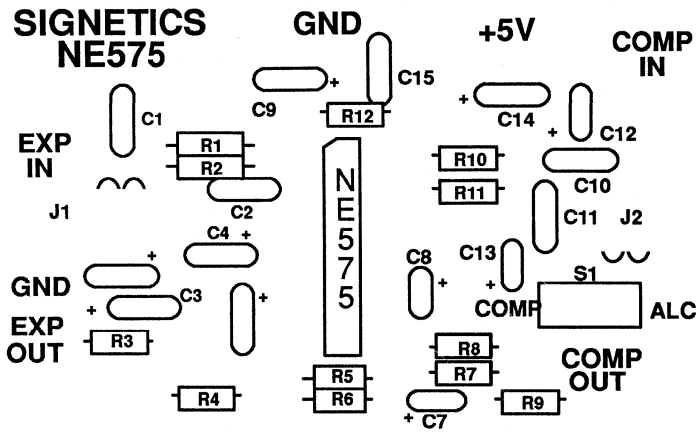
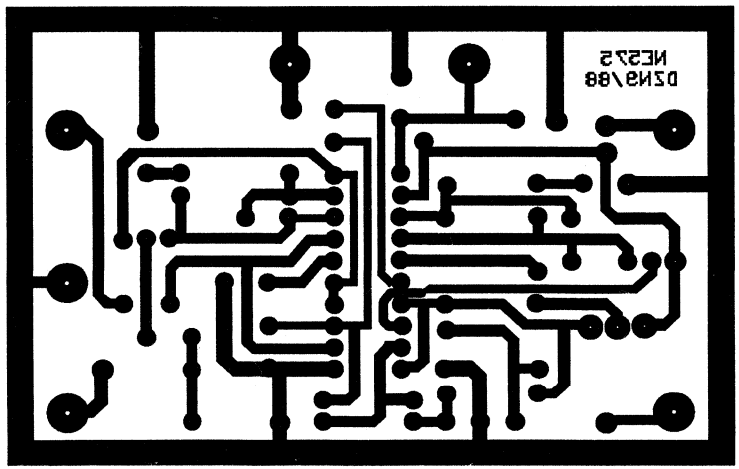


Figure 7. NE575 Expandor Output Frequency Response



8a. Application Board Component Placement



8B. Application Board Layout

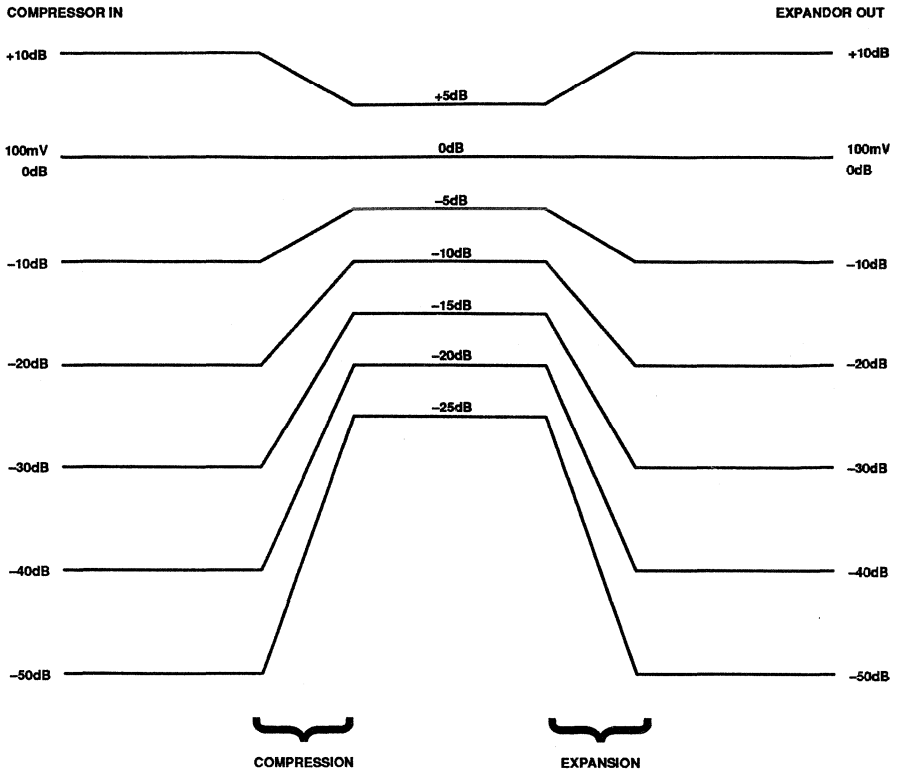


Figure 9. The Companding Function

Document	
ECN No.	
Date of Issue	July 23, 1990
Status	Preliminary Specification
RF Communications	

NE/SA575 (SSOP)

Low voltage compandor in shrink small outline package

DESCRIPTION

The NE/SA575 is a precision dual gain control circuit designed for low voltage applications. The NE575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

FEATURES

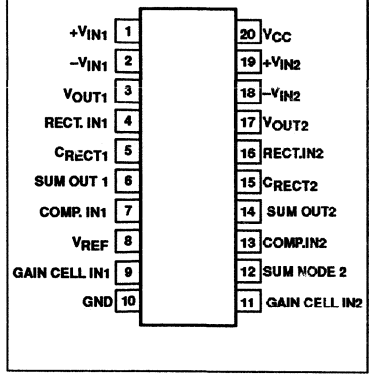
- Operating voltage range from 3V to 7V
- Reference voltage of $100mV_{RMS}$ = 0dB
- One dedicated summing op amp per channel and two extra uncommitted rail-to-rail op amps
- 600Ω drive capability
- Single or split supply operation
- Wide input/output swing capability
- DTMF summing

APPLICATIONS

- Portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Portable broadcast mixers
- Wireless microphones
- Modems
- Electric organs
- Hearing aids

PIN CONFIGURATION

SSOP Package

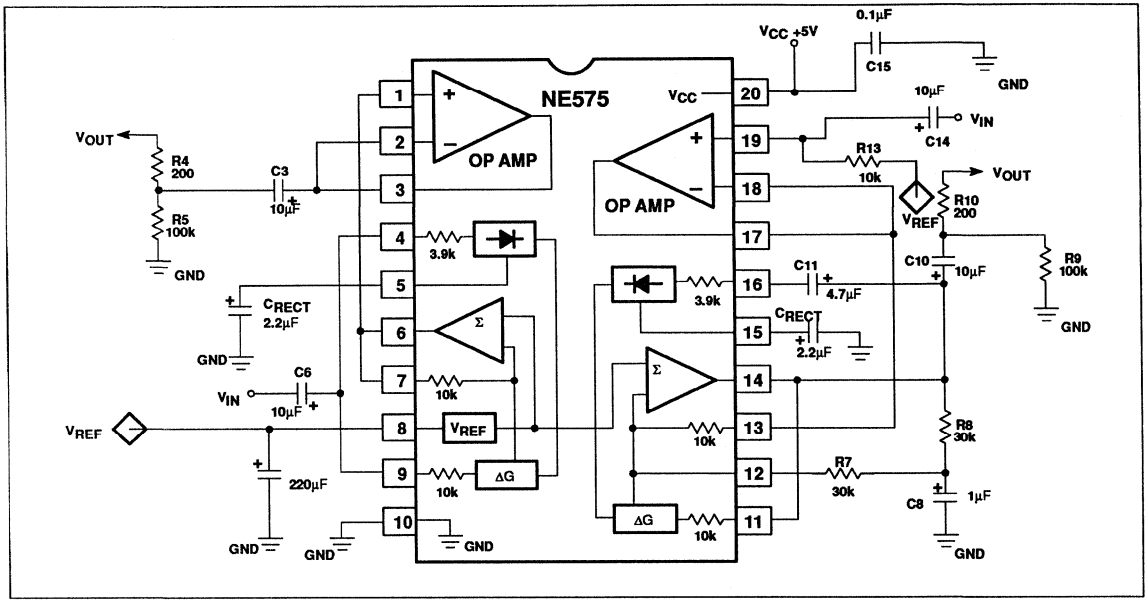


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SSOP	0 to +70°C	NE575DK
20-Pin Plastic SSOP	–40 to +85°C	SA575DK

Low voltage compandor in shrink small outline package NE/SA575 (SSOP)

BLOCK DIAGRAM and TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE575	SA575	
V_{CC}	Single supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance SSOP	117	117	°C/W

AC/DC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = 5V, unless otherwise stated. Both channels are tested in the Expandor mode (see Test Circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575			SA575			
			MIN	TYP	MAX	MIN	TYP	MAX	
For compandor, including summing amplifier									
V_{CC}	Supply voltage[1]		3	5	7	3	5	7	V
I_{CC}	Supply current	No signal	3	4.2	5.5	3	4.2	5.5	mA
V_{REF}	Reference voltage[2]	V_{CC} = 5V	2.4	2.5	2.6	2.4	2.5	2.6	V
R_L	Summing amp output load		10			10			kΩ
THD	Total harmonic distortion	1kHz, 0dB BW = 3.5kHz		0.12	1.0		0.12	1.5	%
E_{NO}	Output voltage noise	BW = 20kHz, R_S = 0Ω		6	20		6	30	µV
0dB	Unity gain level	1kHz	–1.0		1.0	–1.5		1.5	dB
V_{OS}	Output voltage offset	No signal	–100		100	–150		150	mV
	Output DC shift	No signal to 0dB	–50		50	–100		100	mV

Low voltage compandor in shrink small outline package NE/SA575 (SSOP)

AC/DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575			SA575			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Tracking error relative to 0dB	Gain cell input = 0dB, 1kHz Rectifier input = 6dB, 1kHz	–0.5		0.5	–1.0		1.0	dB
		Gain cell input = 0dB, 1kHz Rectifier input = –30dB, 1kHz	–0.5		0.5	–1.0		1.0	dB
	Crosstalk	1kHz, 0dB, C_{REF} = 220µF		–80	–65		–80	–65	dB
For operational amplifier									
V_O	Output swing	R_L = 10kΩ	V_{CC}–0.4	V_{CC}–0.2		V_{CC}–0.4	V_{CC}–0.2		V
R_L	Output load	1kHz	600			600			Ω
CMR	Input common-mode range		0		V_{CC}	0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	80		60	80		dB
I_B	Input bias current	V_{IN} = 0.5V to 4.5V	–0.5		0.5	–1		1	µA
V_{OS}	Input offset voltage			3			3		mV
A_{VOL}	Open-loop gain	R_L = 10kΩ		80			80		dB
SR	Slew rate	Unity gain		1			1		V/µs
GBW	Bandwidth	Unity gain		3			3		MHz
E_{NI}	Input voltage noise	BW = 20kHz		2.5			2.5		µV
PSRR	Power supply rejection ratio	1kHz, 250mV		60			60		dB

NOTES:
9. Operation down to V_{CC} = 2V is possible, but performance is significantly reduced. See curve in Figure 5.
10. Reference voltage, V_{REF}, is typically at 1/2V_{CC}.

FUNCTIONAL DESCRIPTION

This section describes the basic subsystems and applications of the NE/SA575 Compandor. More theory of operation on compandors can be found in AN174 and AN176. The typical applications of the NE575 low voltage compandor in an Expandor (1:2), Compressor (2:1) and Automatic Level Control (ALC) function are explained. These three circuit configurations are shown in Figures 1, 2, 3 respectively.

The NE575 has two channels for a complete companding system. The left channel, A, can be configured as a 1:2 Expandor while the right channel, B, can be configured as either a 2:1 Compressor, a 1:2 Expandor or an ALC. Each channel consists of the basic companding building blocks of rectifier cell, variable gain cell, summing amplifier and V_{REF} cell. In addition, the NE575 has two additional high performance uncommitted op amps which can be utilized for application such as filtering, pre-emphasis/de-emphasis or buffering.

Figure 4 shows the complete schematic for the applications demo board. Channel A is configured as an expandor while channel B is configured so that it can be used either as a compressor or as an ALC circuit. The switch, S1, toggles the circuit between compressor and ALC mode. Jumpers J1 and J2 can be used to either include the additional op amps for signal conditioning or exclude them from the signal path. Bread boarding space is provided for R1, R2, C1, C2, R10, R11, C10 and C11 so that the response can be tailored for each individual need. The components as specified are suitable for the complete audio spectrum from 20Hz to 20kHz.

The most common configuration is as a unity gain non-inverting buffer where R1, C1, C2, R10, C10 and C11 are eliminated and R2 and R11 are shorted. Capacitors C3, C5, C8, and C12 are for DC blocking, and R4 and R8 provide termination (for the capacitors). In systems where the inputs and outputs are AC coupled, these capacitors and resistors can be eliminated. Capacitors C4 and C9 are for setting the attack and release time constant.

C6 is for decoupling and stabilizing the voltage reference circuit. The value of C6 should be such that it will offer a very low impedance to the lowest frequencies of interest. Too small a capacitor will allow supply ripple to modulate the audio path. The better filtered the power supply, the smaller this capacitor can be. R5 and R12 provide DC reference voltage to the amplifiers of channel B. R6 and R7 provide a DC feedback path for the summing amp of channel B, while C7 is a short-circuit to ground for signals. C14 and C15 are for power supply decoupling. C14 can also be eliminated if the power supply is well regulated with very low noise and ripple. Figure 8 shows the PC board layout of the applications demo board.

DEMONSTRATED PERFORMANCE

The applications demo board was built and tested for a frequency range of 20Hz to 20kHz with the component values as shown in Figure 4 and V_{CC} = 5V. In the expandor mode, the typical input dynamic range was from –34dB to +12dB where 0dB is equal to 100mV_{RMS}. The typical unity gain level measured at 0dB @ 1kHz input was ±0.5dB and the typical tracking error was ±0.1dB for input range of –30 to +10dB.

In the compressor mode, the typical input dynamic range was from –42dB to ±18dB with a tracking error +0.1dB and the typical unity gain level was ±0.5dB.

In the ALC mode, the typical input dynamic range was from –42dB to +8dB with typical output deviation of ±0.2dB about the nominal output of 0dB. For input greater than +9dB in ALC configuration, the summing amplifier sometimes exhibits high frequency

Low voltage compandor in shrink small outline package NE/SA575 (SSOP)

oscillations. There are several solutions to this problem. The first is to lower the values of R7 and R8 to 20kΩ each. The second is to add a current limiting resistor in series with C13 at Pin 13. The third is to add a compensating capacitor of about 22 to 30pF between the input and output of summing amplifier (Pins 12 and 14). With any one of the above recommendations, the typical ALC mode input range increased to +18dB yielding a dynamic range of over 60dB.

EXPANDOR

The typical expandor configuration is shown in Figure 1. The variable gain cell and the rectifier cell are in the signal input path. The V_{REF} is always 1/2 V_{CC} to provide the maximum headroom without clipping. The 0dB ref is 100mV_{RMS}. The input is AC coupled through C5, and the output is AC coupled through C3. If in a system the inputs and outputs are AC coupled, then C3, C5, R3 and R4 can be eliminated, thus requiring only one external component, C4. The variable gain cell and rectifier cell are DC coupled so any offset voltage between Pins 4 and 9 will cause small offset error current in the rectifier cell. This will affect the accuracy of the gain cell. This can be improved by using an extra capacitor from the input to Pin 4 and eliminating the DC connection between Pins 4 and 9.

The expandor gain expression and the attack and release time constant is given by Equation 1 and Equation 2, respectively.

Equation 1.

$$\text{Expandor gain} = \frac{4V_{IN}(avg)}{3.9k \times 100\mu A}$$

where $V_{IN}(avg) = 0.975V_{IN(RMS)}$

Equation 2.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

COMPRESSOR

The typical compressor configuration is shown in Figure 2. In this mode, the rectifier cell and variable gain cell are in the feedback path. R6 and R7 provide the DC feedback to the summing amplifier. The input is AC coupled through C12 and output is AC coupled through C8. In a system with inputs and outputs AC coupled, C8, C12, R8, and R9 could be eliminated and only R5, R6, R7, C7, and C13 would be required. If the external components R5, R6, R7 and C7 are eliminated, then the output of the summing amplifier will motor-boat in absence of signals or at extremely low signals. This is because there is no DC feedback path from the output to input. In the presence of an AC signal this phenomenon is not observed and the circuit will appear to function properly.

The compressor gain expression and the attack and release time constant is given by Equation 3 and Equation 4, respectively.

Equation 3.

$$\text{Compressor gain} = \left[\frac{3.9k \times 100\mu A}{4V_{IN}(avg)}\right]^{1/2}$$

where $V_{IN}(avg) = 0.975V_{IN(RMS)}$

Equation 4.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

AUTOMATIC LEVEL CONTROL

The typical Automatic Level Control circuit configuration is shown in Figure 3. It can be seen that it is quite similar to the compressor schematic except that the input to the rectifier cell is from the input path and not from the feedback path. The input is AC coupled through C12 and C13 and the output is AC coupled through C8. Once again, as in the previous cases, if the system input and output signals are already AC coupled, then C12, C13, C8, R8 and R9 could be eliminated. Concerning the compressor, removing R5, R6, R7 and C7 will cause motor-boating in absence of signals. C_{COMP} is necessary to stabilize the summing amplifier at higher input levels. This circuit provides an input dynamic range greater than 60dB with the output within ±0.5dB typical. The necessary design expressions are given by Equation 5 and Equation 6, respectively.

Equation 5.

$$\text{ALC gain} = \frac{3.9k \times 100\mu A}{4V_{IN}(avg)}$$

Equation 6.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C9$$

Figure 5 shows that the unity gain error remains small over a wide range of supply voltages. The unity gain error is important because it effects the tracking error. So, to achieve the best unity gain error, provide a power supply voltage of 4 to 5V to the NE575.

Figures 6 and 7 show the output level over a range of frequencies and inputs for the compressor and expandor, respectively. These graphs reveal that the compandor has a constant and flat output. This is important because the signal will not be altered.

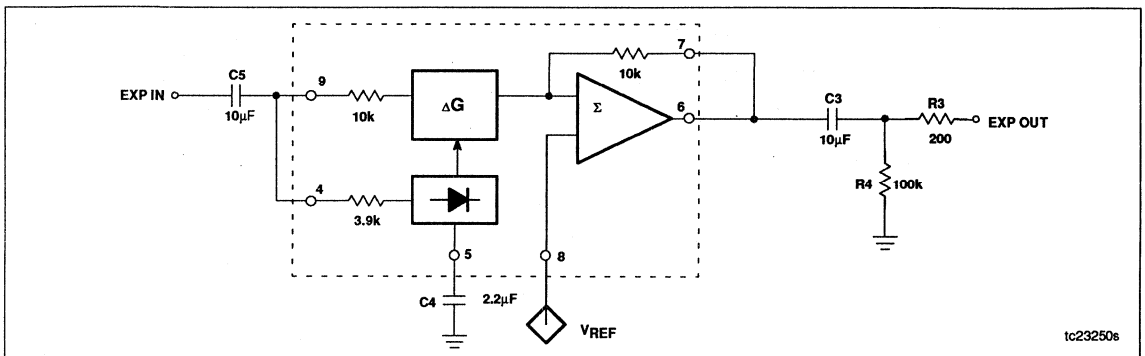


Figure 1. Typical Expandor Configuration

Low voltage compandor in shrink small outline package NE/SA575 (SSOP)

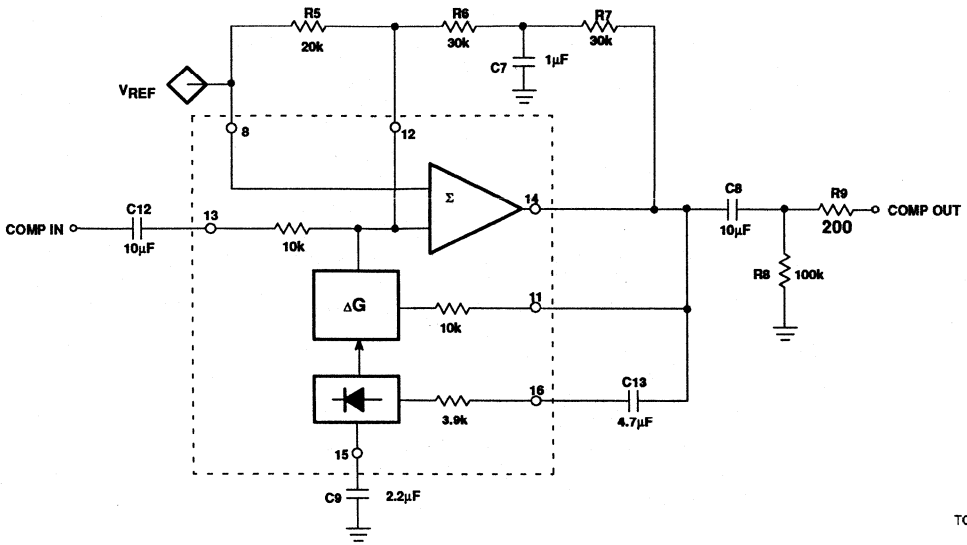


Figure 2. Typical Compressor Configuration

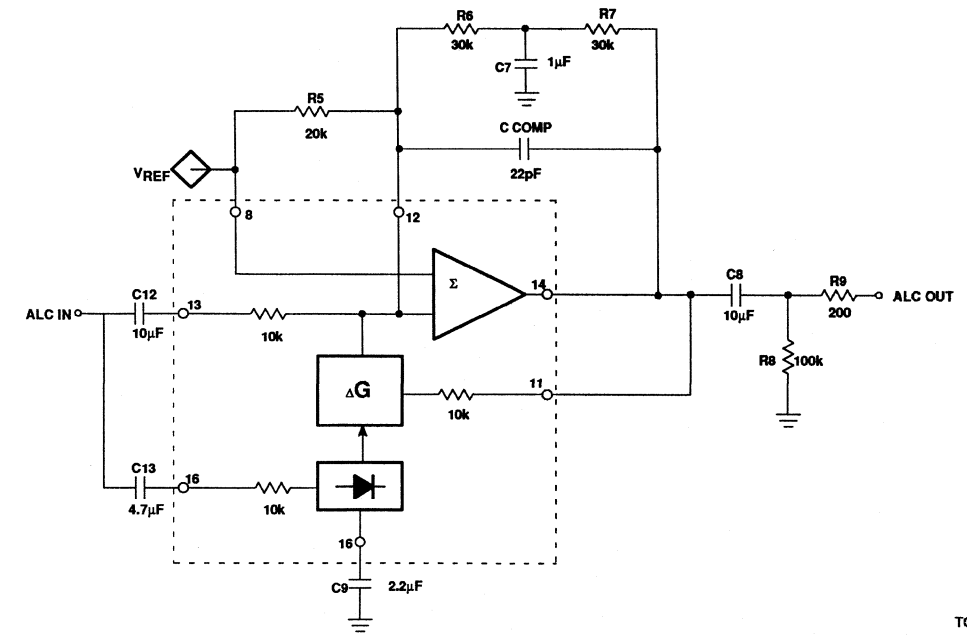


Figure 3. Typical ALC Configuration

Low voltage compandor in shrink small outline package NE/SA575 (SSOP)

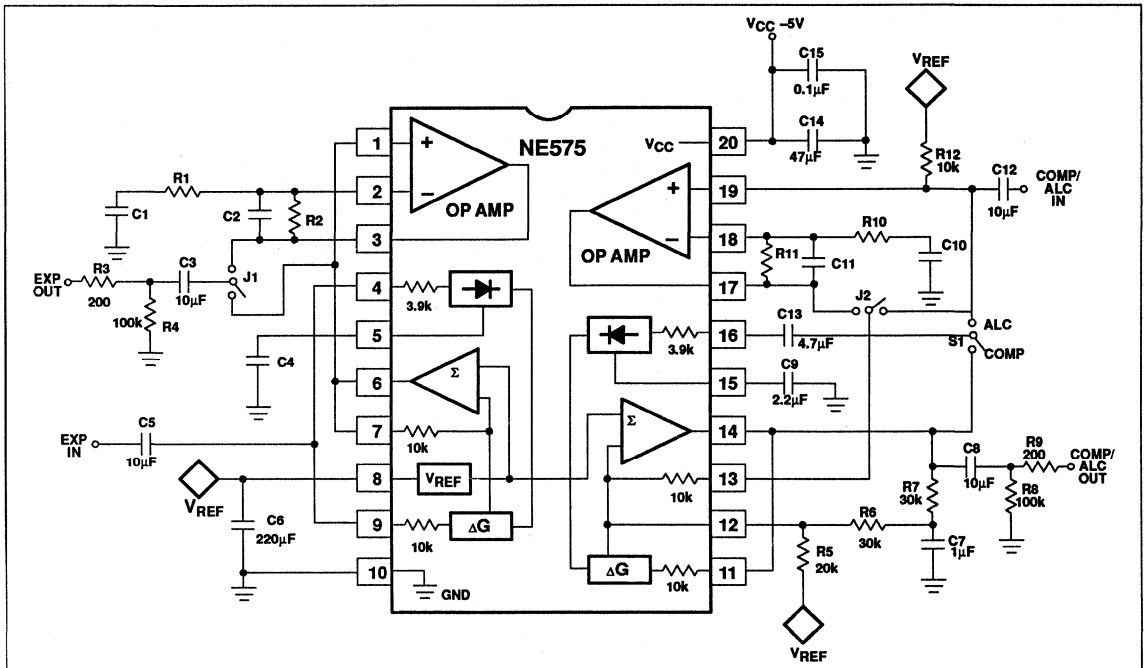


Figure 4. Signetics NE575 Low Voltage Expandor/Compressor/ALC Demo Board

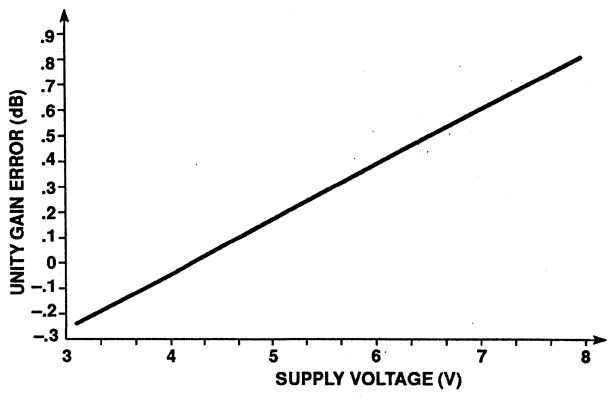


Figure 5. Unity Gain Error vs Supply Voltage

Low voltage compandor in shrink small outline package NE/SA575 (SSOP)

TYPICAL PERFORMANCE CHARACTERISTICS

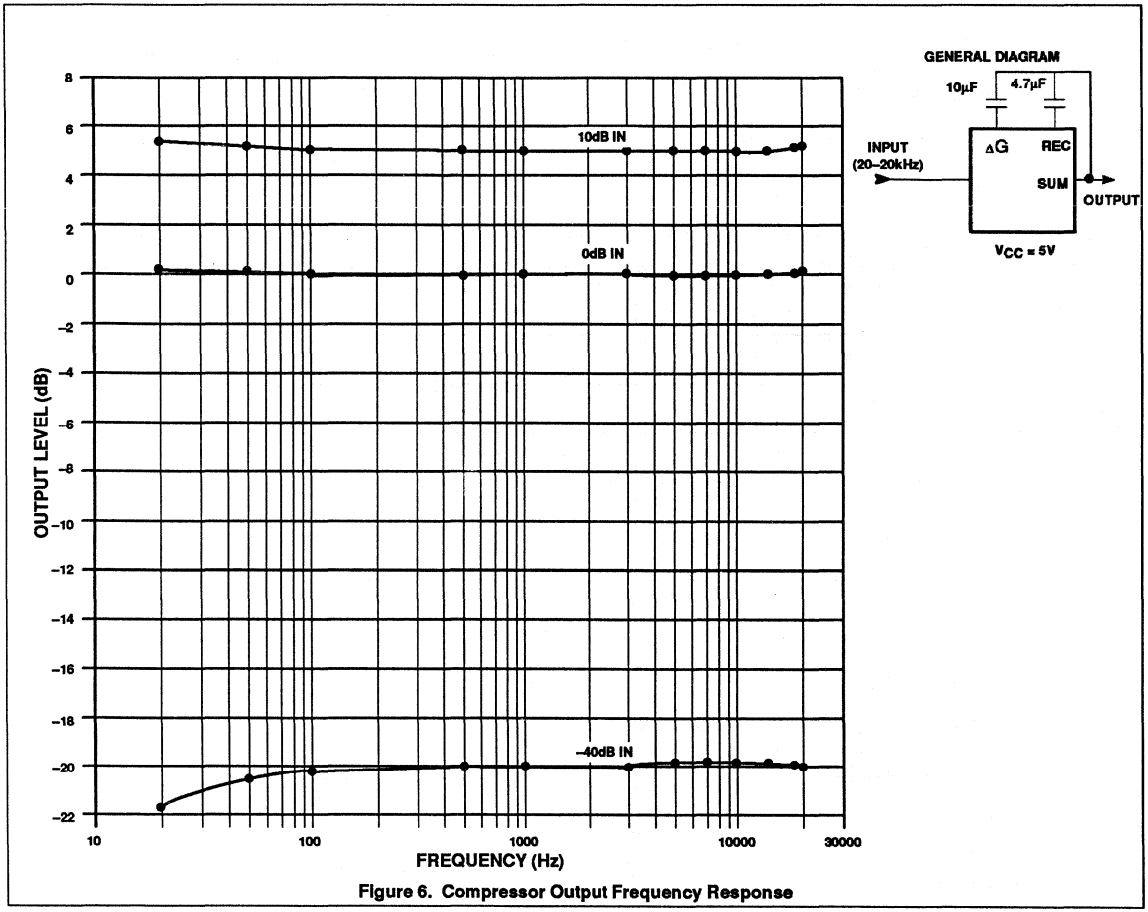


Figure 6. Compressor Output Frequency Response

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

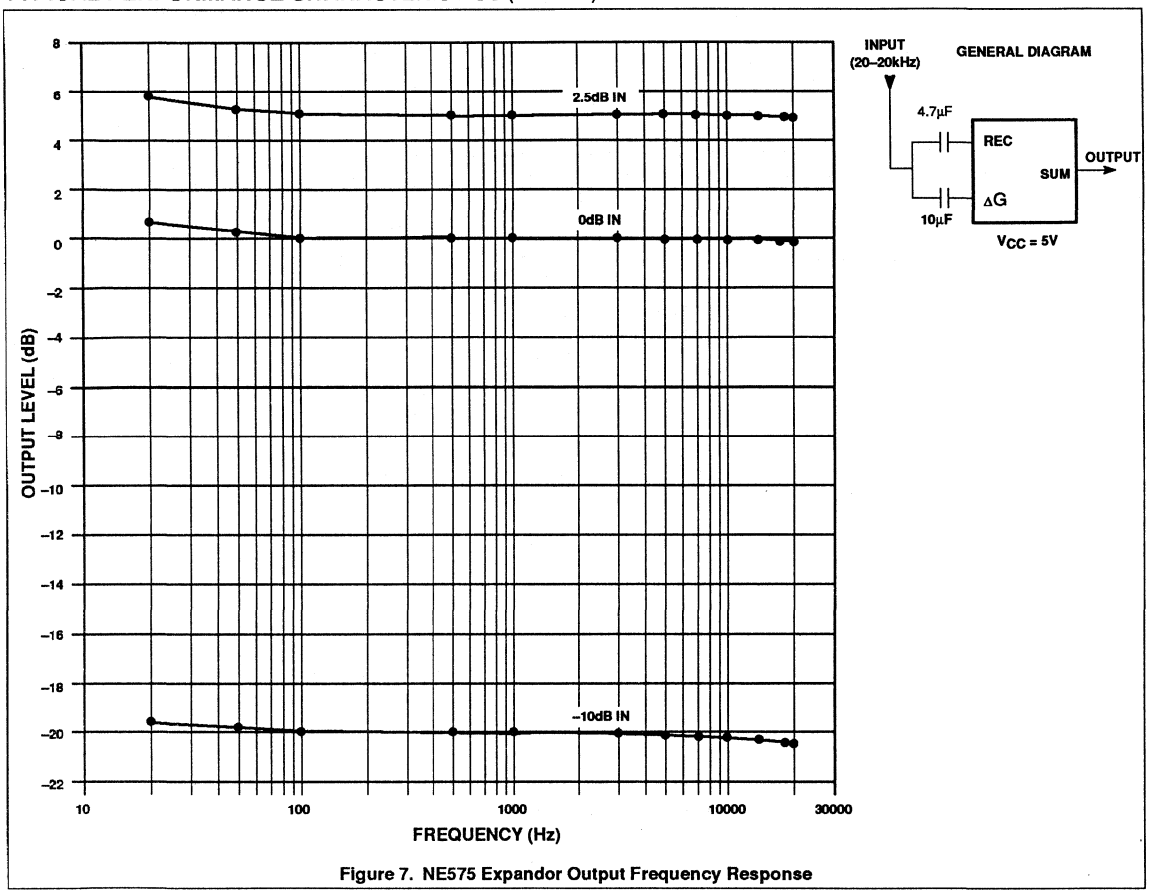


Figure 7. NE575 Expandor Output Frequency Response

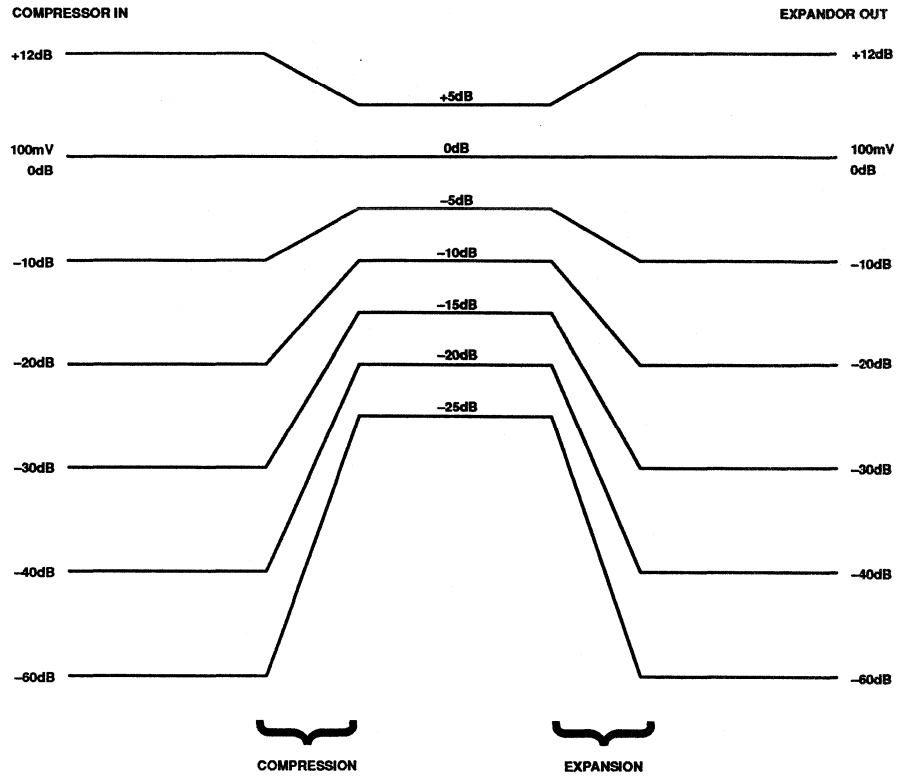


Figure 9. The Companding Function

Document	
ECN No.	
Date of Issue	September 11, 1990
Status	Preliminary Specification
RF Communications	

NE/SA577

Unity gain level programmable low power compandor

DESCRIPTION

The NE/SA577 is a unity gain level programmable compandor designed for low power applications. The NE577 is internally configured as an expandor and a compressor to minimize external component count.

The NE577 is available in a 14-pin plastic DIP and SO packages.

FEATURES

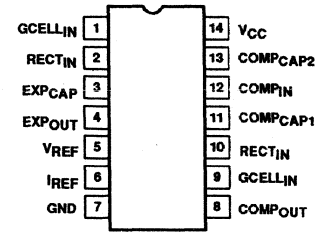
- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable ($10mV_{RMS}$ to $1.0V_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- SA577 meets cellular radio specifications
- ESD hardened

APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

PIN CONFIGURATION

D and N Packages

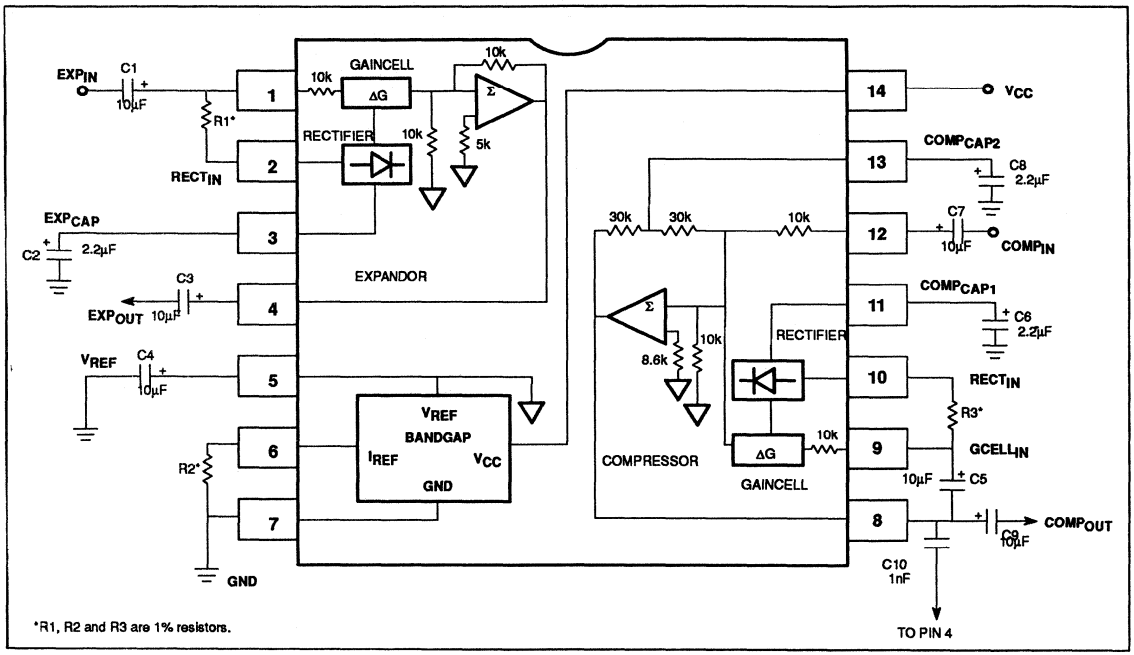


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE577N
14-Pin Plastic SO	0 to +70°C	NE577D
14-Pin Plastic DIP	–40 to +85°C	SA577N
14-Pin Plastic SO	–40 to +85°C	SA577D

Unity gain level programmable low power compandor NE/SA577

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



Unity gain level programmable low power compandor NE/SA577

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE577	SA577	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA577			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	2	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V	1.7	1.8	1.9	V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.1	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω			25	μV
0dB	Unity gain level	0dB at 1kHz	–1.5		1.5	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		dBV
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		dBV
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		dBV
V_{OS}	Output voltage offset	No signal	–150		150	mV
	Expandor output DC shift	No signal to 0dB	–100		100	mV
	Tracking error relative to 0dB output		–1.0		1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10μF		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		V

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see application note AN1762.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = 10mV_{RMS} and 0dBV = 1.0V_{RMS}. For details see application note AN1762.

Document	
ECN No.	
Date of Issue	September 11, 1990
Status	Preliminary Specification
Application Specific Product	

NE/SA578

Unity gain level programmable low power compandor

DESCRIPTION

The NE/SA578 is a unity gain level programmable compandor designed for low power applications. The NE578 is internally configured as an expandor and a compressor to minimize external component count.

The summing amplifiers of the NE578 have 600Ω drive capability and the inverting input of the compressor amplifier is accessible through Pin 9 for summing multiple external signals. Power Down/Mute function is active low and requires an open collector output logic configuration at Pin 8. If Power Down/Mute is not needed, Pin 8 should be left open. When the part is muted, supply current drops to 170μA at 3.6V. The NE578 is available in a 16-pin plastic DIP and SO packages.

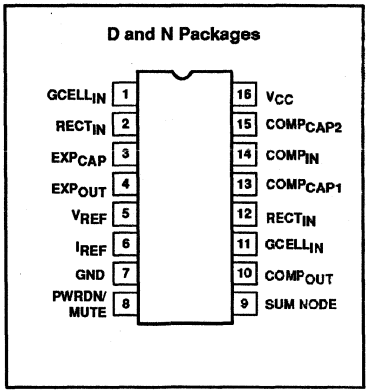
FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable ($10mV_{RMS}$ to $1.0V_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability
- Low external component count
- SA578 meets cellular radio specifications
- ESD hardened
- Power Down mode (I_{CC} = 170μA @ 3.6V)
- Mute function
- Multiple external summing capability
- 600Ω drive capability

APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

PIN CONFIGURATION

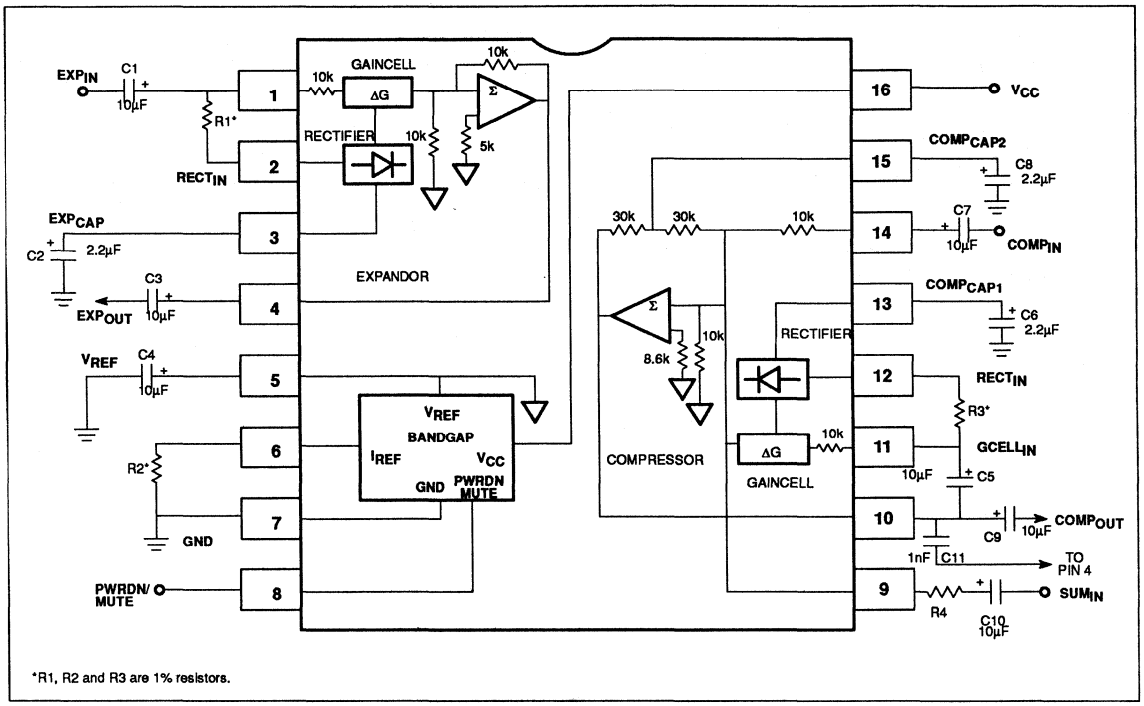


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE578N
16-Pin Plastic SO	0 to +70°C	NE578D
16-Pin Plastic DIP	–40 to +85°C	SA578N
16-Pin Plastic SO	–40 to +85°C	SA578D

Unity gain level programmable low power compandor NE/SA578

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



*R1, R2 and R3 are 1% resistors.

Unity gain level programmable low power compandor NE/SA578

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE578	SA578	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA578			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current operating power down	No signal, R_2 = 100kΩ		1.4 170	2	mA µA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V	1.7	1.8	1.9	V
R_L	Summing amp minimum output load			600		Ω
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.1	1.0	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω			20	µV
0dB	Unity gain level	0dB at 1kHz	–1.0		1.0	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		dBV
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		dBV
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		dBV
V_{OS}	Output voltage offset	No signal	–150		150	mV
	Expandor output DC shift	No signal to 0dB	–100		100	mV
	Tracking error relative to 0dB output		–1.0		1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		V
	Power Down/Mute low level		0		0.4	V
	Power Down/Mute input current	Pin 8 grounded		–65		µA

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see application note AN1762.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = 10mV_{RMS} and 0dBV = 1.0V_{RMS}. For details see application note AN1762.

NE/SA602
Double-Balanced Mixer and Oscillator

Product Specification

DESCRIPTION

The SA/NE602 is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602 make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external L.O. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the SA/NE602 a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

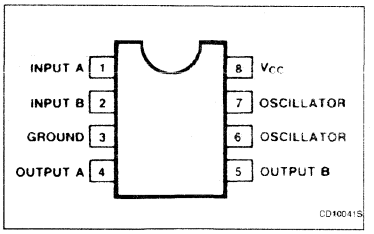
FEATURES

- **Low current consumption: 2.4mA typical**
- **Excellent noise figure: < 5.0dB typical at 45MHz**
- **High operating frequency**
- **Excellent gain, intercept and sensitivity**
- **Low external parts count; suitable for crystal/ceramic filters**
- **SA602 meets cellular radio specifications**

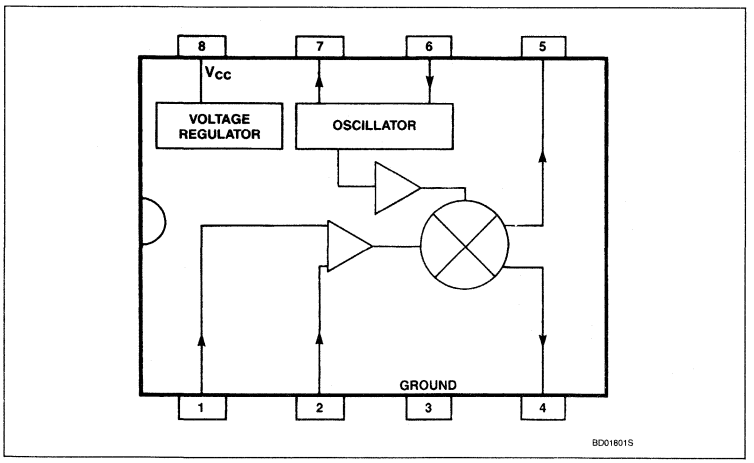
APPLICATIONS

- **Cellular radio mixer/oscillator**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **HF/VHF frequency conversion**
- **Instrumentation frequency conversion**
- **Broadband LANs**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE602N
8-Pin Plastic SO	0 to +70°C	NE602D
8-Pin Cerdip	0 to +70°C	NE602FE
8-Pin Plastic DIP	−40°C to +85°C	SA602N
8-Pin Plastic SO	−40°C to +85°C	SA602D
8-Pin Cerdip	−40°C to +85°C	SA602FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature range NE602 SA602	0 to +70 −40 to +85	°C °C

AC/DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 6V, Figure 1

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0	6.0	dB
	Third-order intercept point	RF_{IN} = −45dBm: f_1 = 45.0 f_2 = 45.06		−15	−17	dBm
	Conversion gain at 45MHz		14	18		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

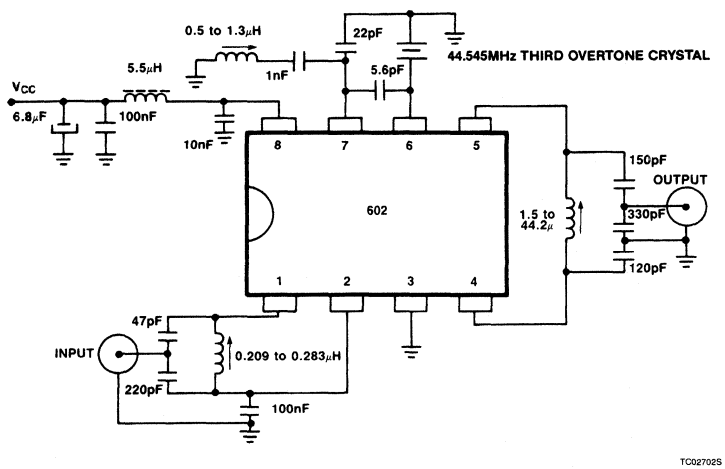


Figure 1. Test Configuration

DESCRIPTION OF OPERATION

The NE/SA602 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA602 is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio 2nd IF and demodulator, the SA602 is capable of receiving −119dBm signals with a 12dB S/N ratio. Third-order intercept is typically −15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE602 should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE/SA602 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedence is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be at least $200mV_{p-p}$.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor. This improves the AC operating characteristic of the transistor and should help the oscillator to start. 22kΩ will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

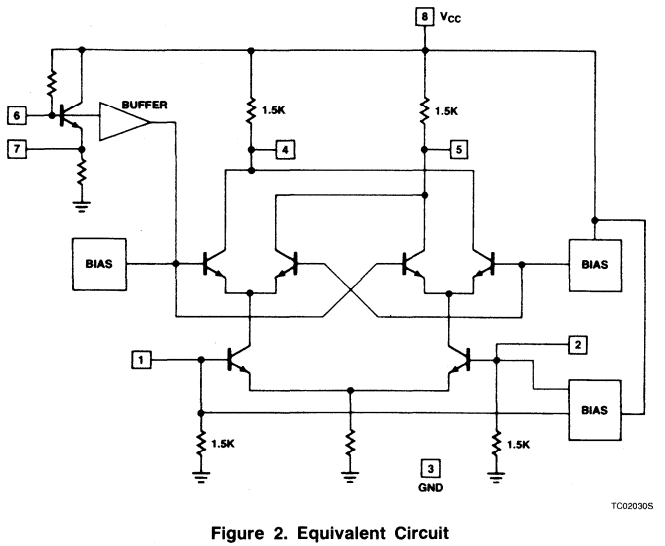
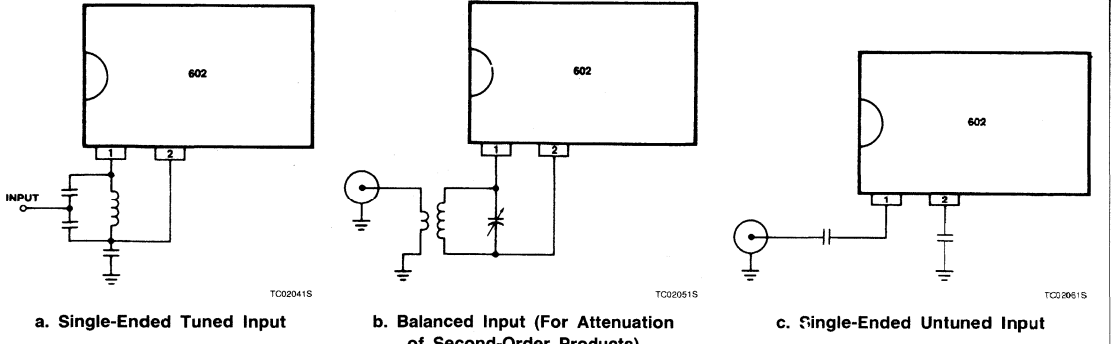


Figure 2. Equivalent Circuit

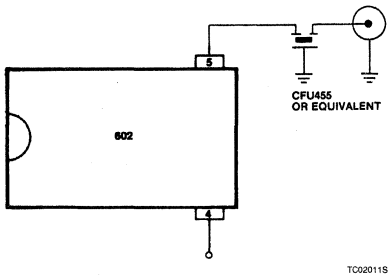


a. Single-Ended Tuned Input

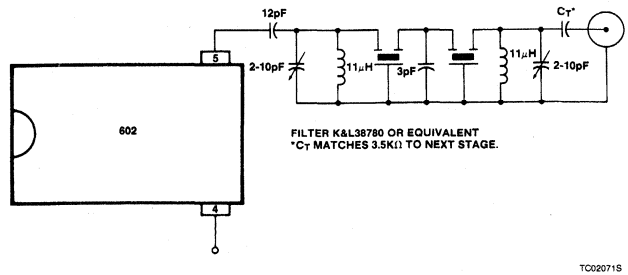
b. Balanced Input (For Attenuation of Second-Order Products)

c. Single-Ended Untuned Input

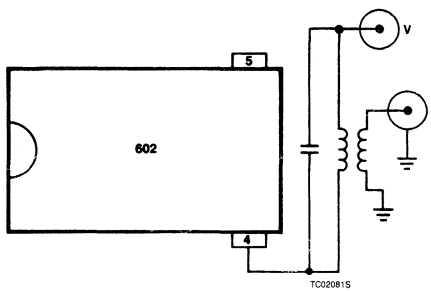
Figure 3. Input Configuration



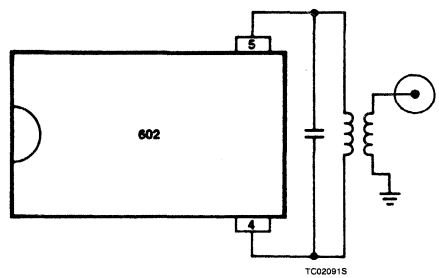
a. Single-Ended Ceramic Filter



b. Single-Ended Crystal Filter

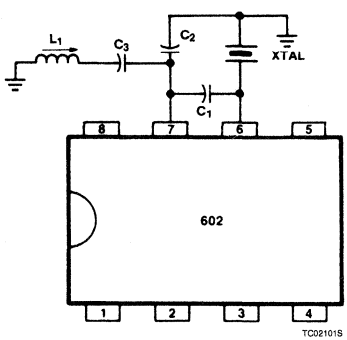


c. Single-Ended IFT

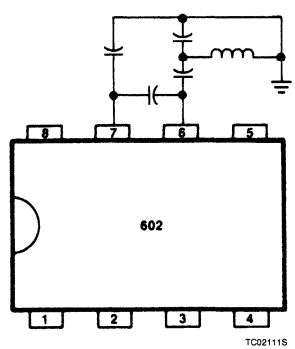


d. Balanced Output

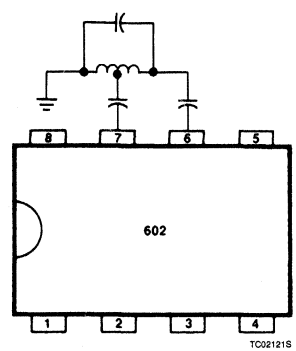
Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)



b. Colpitts L/C Tank Oscillator



c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

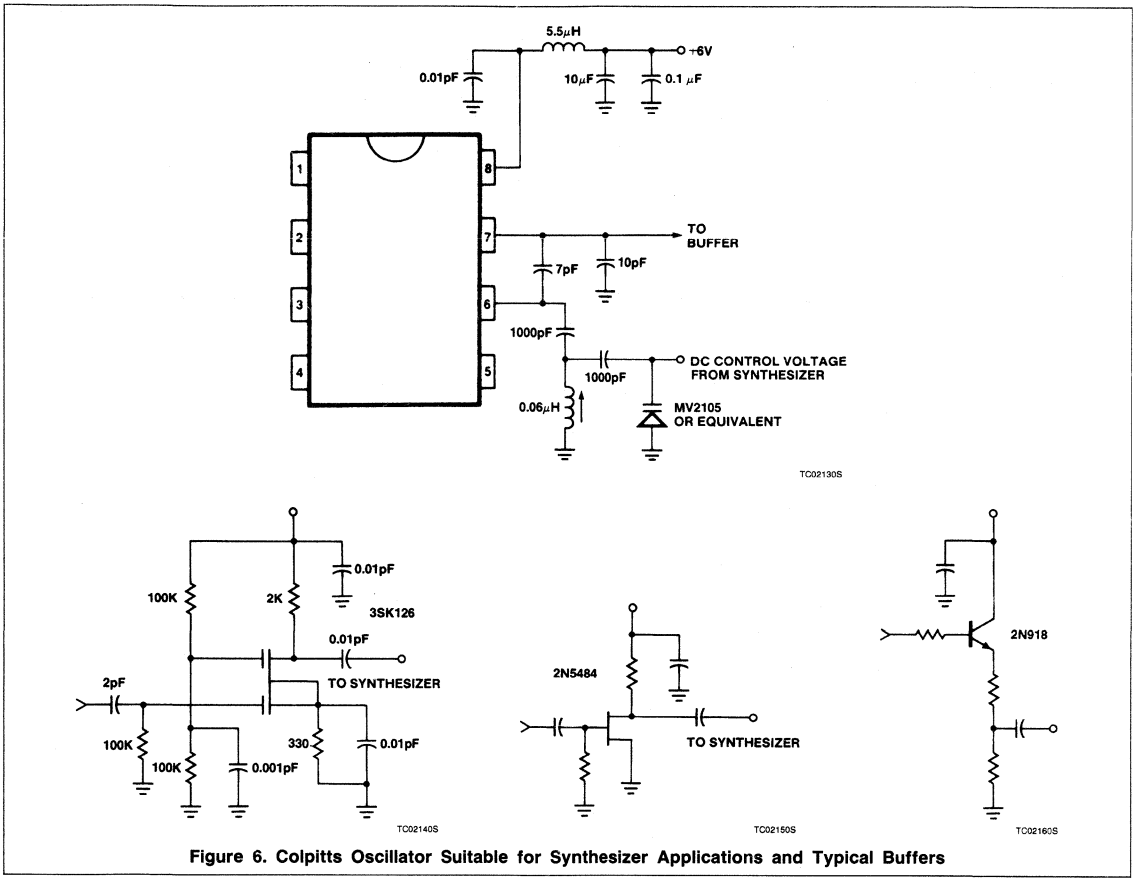


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

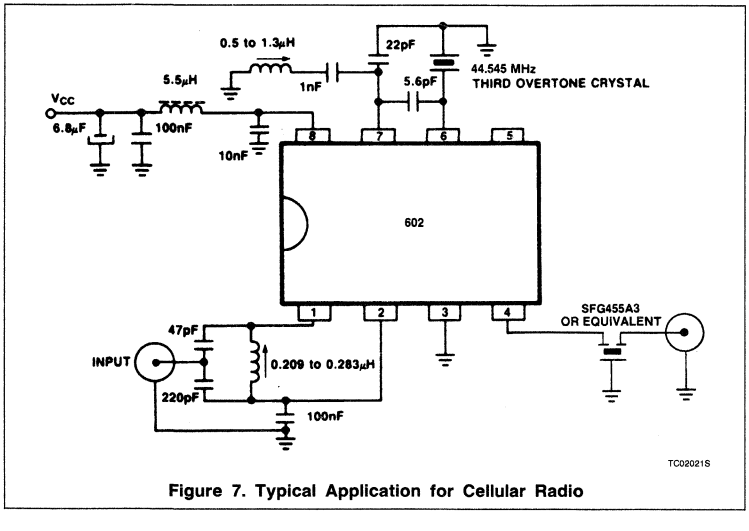


Figure 7. Typical Application for Cellular Radio

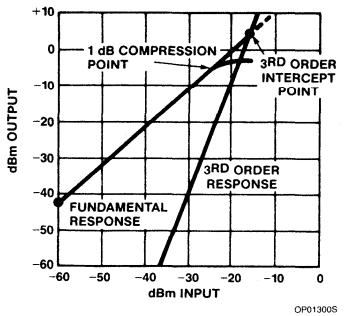


Figure 8. NE/SA602 Third-Order Intermod and 1dB Compression Point Performance

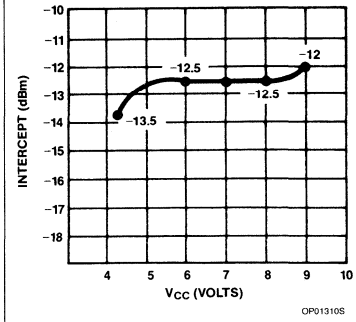


Figure 9. Input Third-Order Intercept Point vs V_{CC}

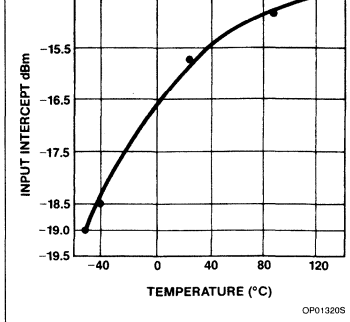


Figure 10. Third-Order Intercept Point vs Temperature

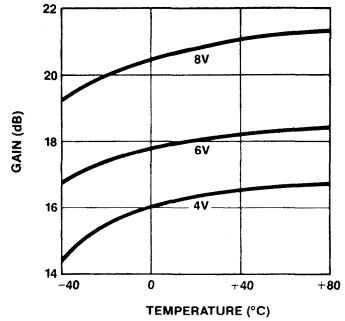


Figure 11

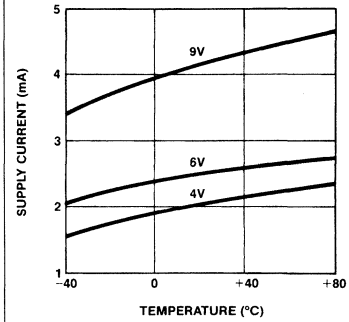


Figure 12

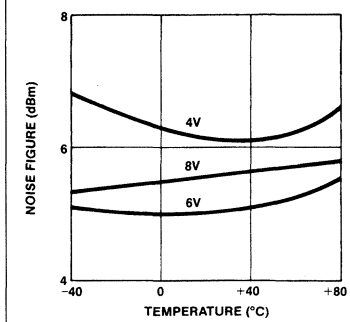


Figure 13

Philips Components

Document	853–1424
ECN No.	99374
Date of Issue	April 17, 1990
Status	Product Specification
RF Communications	

NE/SA602A

Double-balanced mixer and oscillator

DESCRIPTION

The NE/SA602A is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602A make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external LO. For higher frequencies the LO input may be externally driven. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the NE/SA602A a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

FEATURES

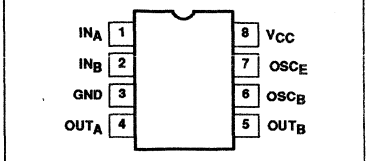
- Low current consumption: 2.4mA typical
- Excellent noise figure: <4.7dB typical at 45MHz
- High operating frequency
- Excellent gain, intercept and sensitivity
- Low external parts count; suitable for crystal/ceramic filters
- SA602A meets cellular radio specifications

APPLICATIONS

- Cellular radio mixer/oscillator
- Portable radio
- VHF transceivers
- RF data links
- HF/VHF frequency conversion
- Instrumentation frequency conversion
- Broadband LANs

PIN CONFIGURATION

F, D and N Packages

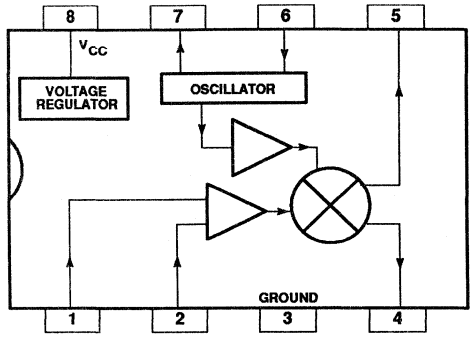


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE602AN
8-Pin Plastic SO (Surface-mount)	0 to +70°C	NE602AD
8-Pin Cerdip	0 to +70°C	NE602AFE
8-Pin Plastic DIP	–40 to +85°C	SA602AN
8-Pin Plastic SO (Surface-mount)	–40 to +85°C	SA602AD
8-Pin Cerdip	–40 to +85°C	SA602AFE

Double–balanced mixer and oscillator NE/SA602A

BLOCK DIAGRAM



Double–balanced mixer and oscillator NE/SA602A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Maximum operating voltage		9	V
T_{STG}	Storage temperature range		–65 to +150	°C
T_A	Operating ambient temperature range	NE602A	0 to +70	°C
		SA602A	–40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		N package	75	°C/W

AC/DC ELECTRICAL CHARACTERISTICS V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA602A			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figure at 45MHz			5.0	5.5	dB
	Third–order intercept point	RF_{IN} = –45dBm: f_1 = 45.0MHz, f_2 = 45.06MHz		–13	–15	dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The NE/SA602A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA602A is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio second IF and demodulator, the SA602A is capable of receiving –119dBm signals with a 12dB S/N ratio. Third–order intercept is typically –13dBm (that is approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small–signal or signal–to–noise issues are not critical, the input to the NE602A should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE/SA602A is designed to be flexible. The input, RF mixer output and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required LO is beyond oscillation limits, or the system calls for an external LO, the external signal can be injected at Pin 6 through a DC blocking capacitor. External LO should be at least 200mV_{P-P}.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 6 shows a Colpitts varactor tuned tank oscillator suitable for synthesizer–controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual–gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non–critical applications. The resistive divider in the emitter–follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor.

This improves the AC operating characteristic of the transistor and should help the oscillator to start. A 22kΩ resistor will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

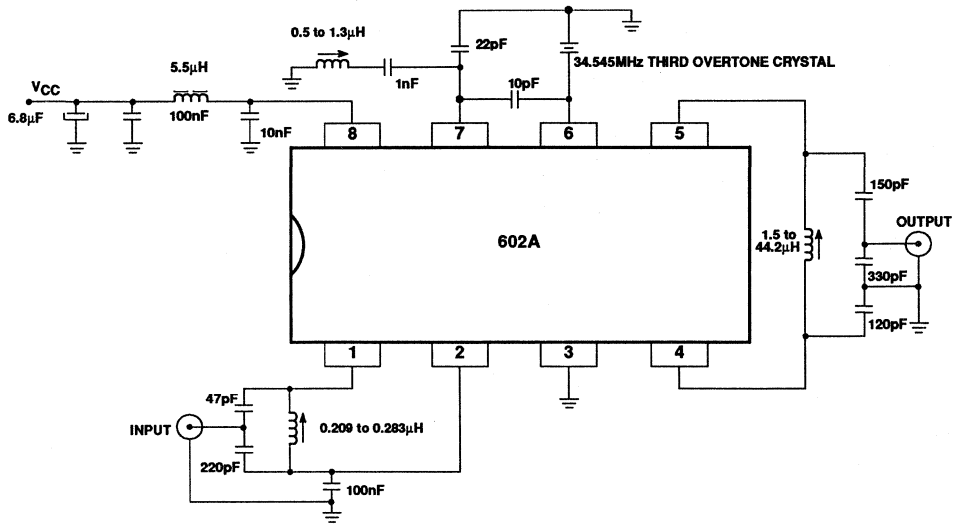


Figure 1. Test Configuration

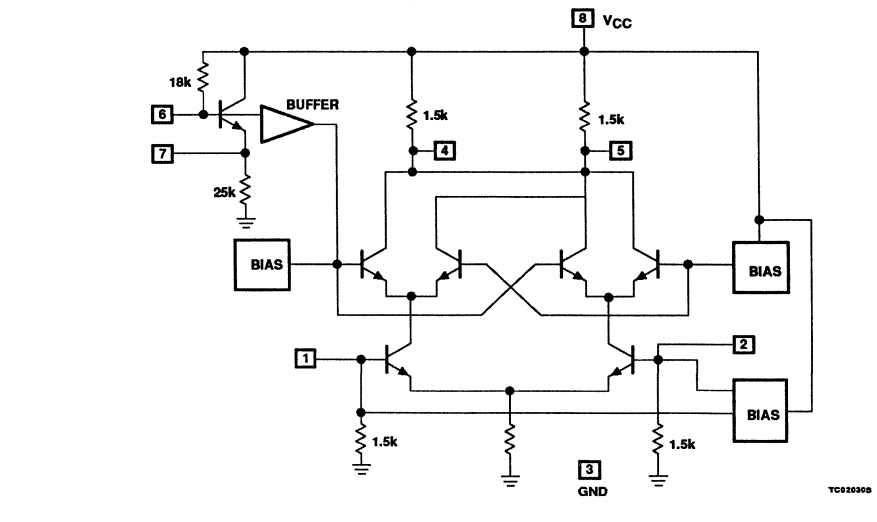
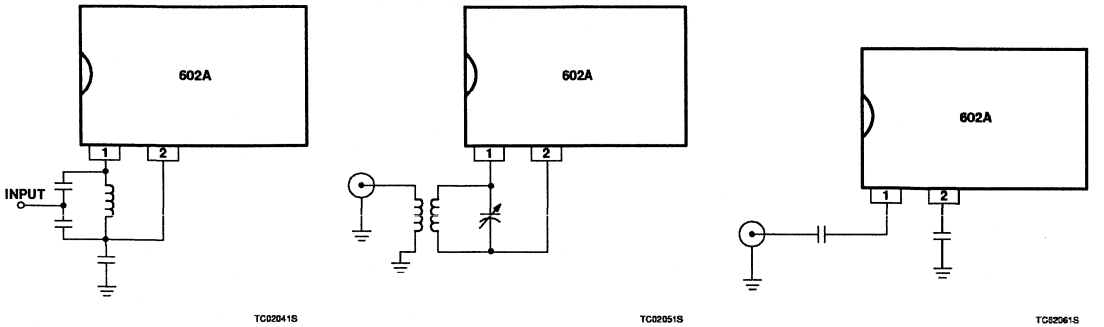


Figure 2. Equivalent Circuit

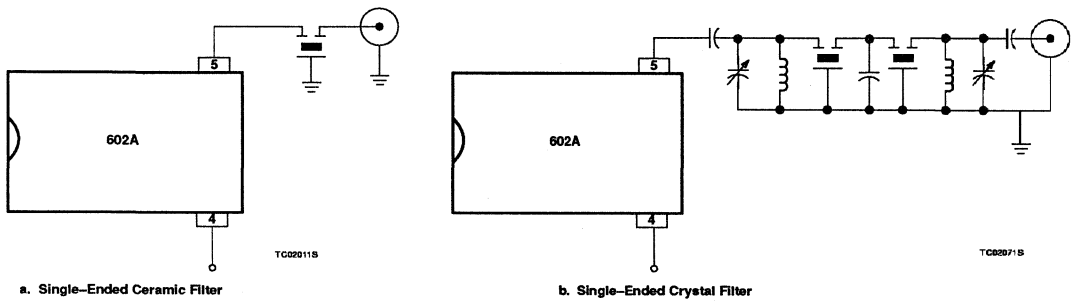


a. Single–Ended Tuned Input

b. Balanced Input (For Attenuation of Second–Order Products)

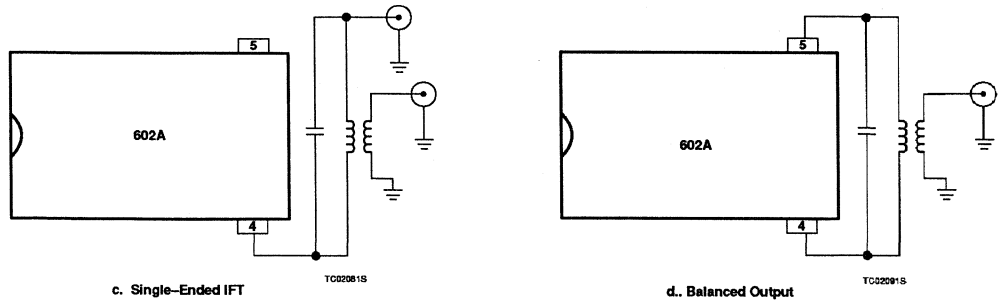
c. Single–Ended Untuned Input

Figure 3. Input Configuration



a. Single–Ended Ceramic Filter

b. Single–Ended Crystal Filter

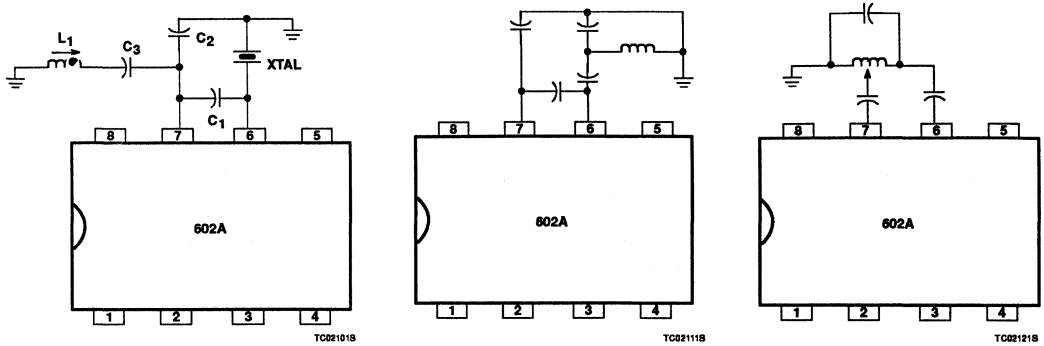


c. Single–Ended IFT

d.. Balanced Output

Figure 4. Output Configuration

Double–balanced mixer and oscillator NE/SA602A



a. Colpitts Crystal Oscillator (Overtone Mode)

b. Colpitts L/C Tank Oscillator

c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

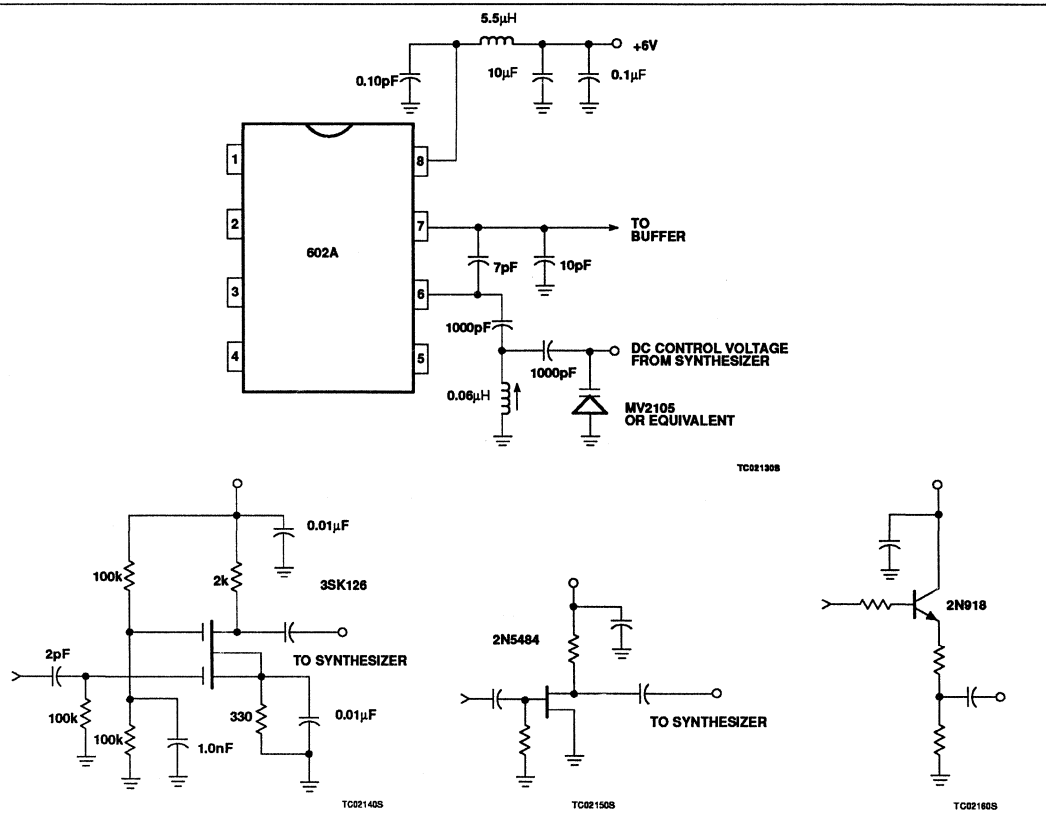


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

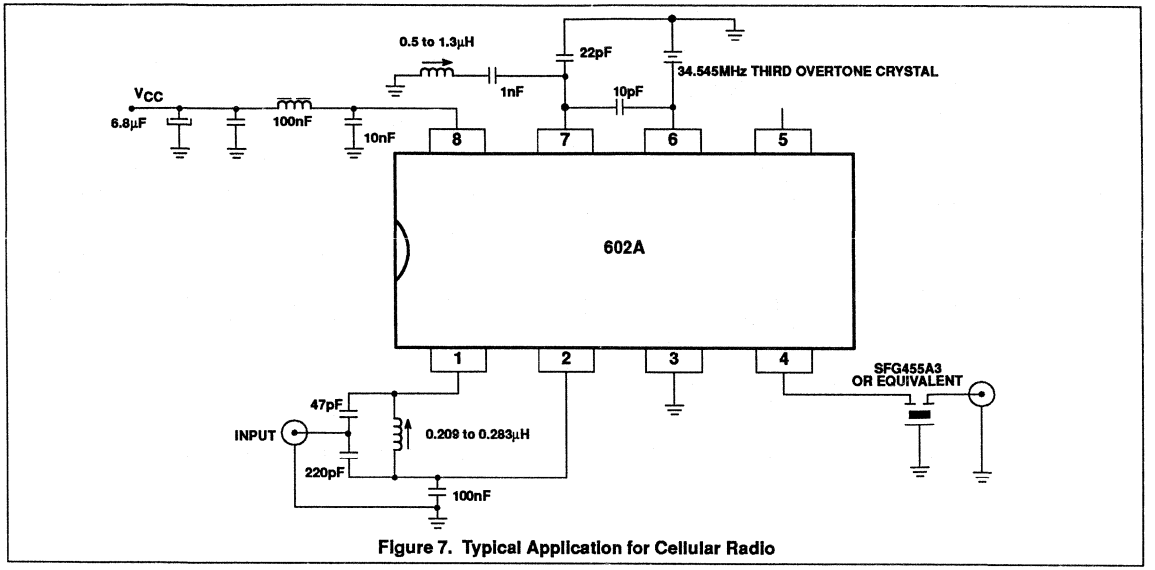


Figure 7. Typical Application for Cellular Radio

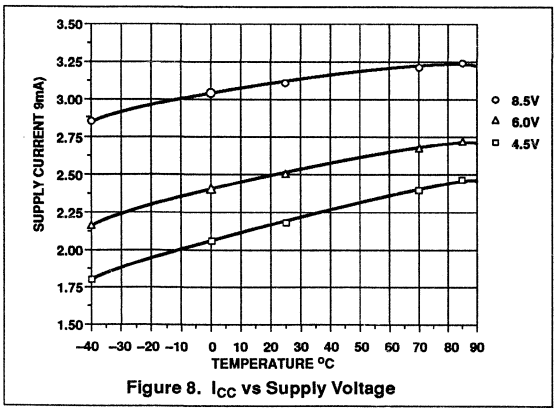


Figure 8. I_{CC} vs Supply Voltage

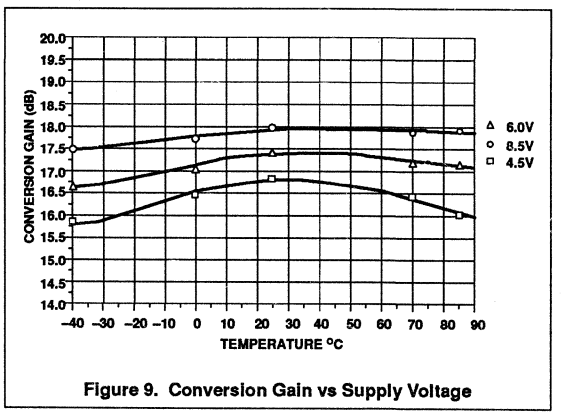


Figure 9. Conversion Gain vs Supply Voltage

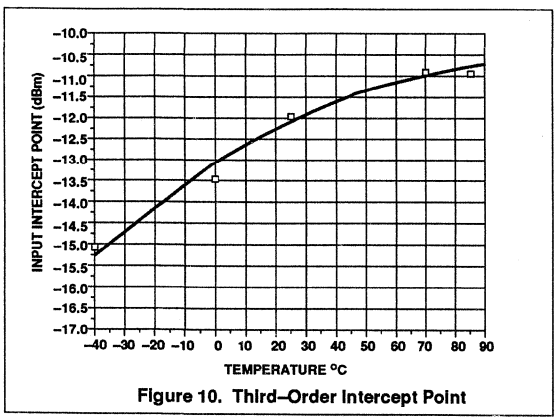


Figure 10. Third–Order Intercept Point

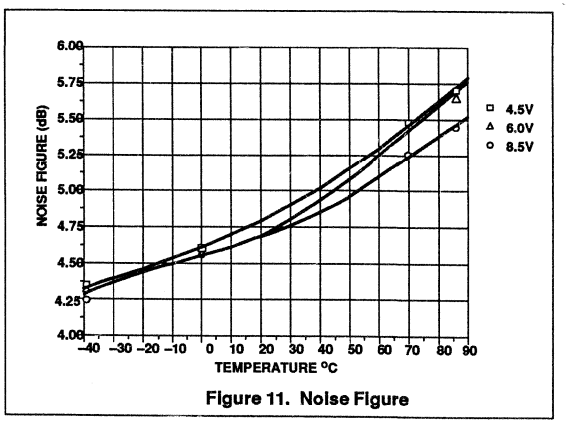


Figure 11. Noise Figure

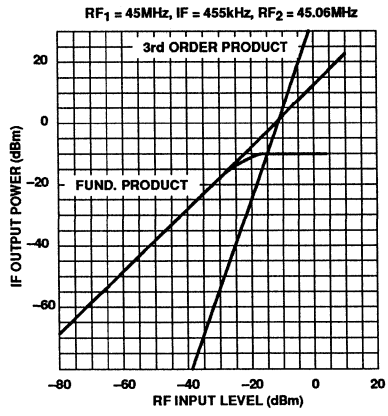


Figure 12. Third–Order Intercept and Compression

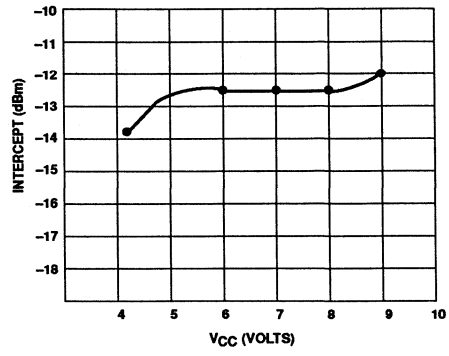


Figure 13. Input Third–Order Intermod Point vs V_{CC}

Document	853–1431
ECN No.	99620
Date of Issue	May 1, 1990
Status	Product Specification
Application Specific Product	

NE/SA604A

High Performance Low Power FM IF System

DESCRIPTION

The NE/SA604A is an improved monolithic low–power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA604A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA604A is available in a 16–lead dual–in–line plastic and 16–lead SO (surface–mounted miniature) package.

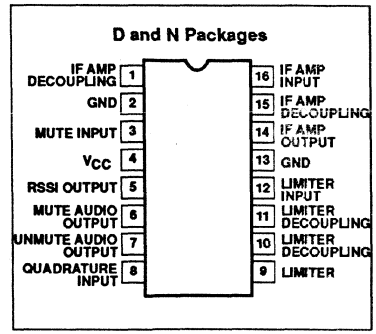
FEATURES

- **Low power consumption: 3.3mA typical**
- **Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Two audio outputs – muted and unmuted**
- **Low external component count; suitable for crystal/ceramic filters**
- **Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz**
- **SA604A meets cellular radio specifications**

APPLICATIONS

- **Cellular radio FM IF**
- **High performance communications receivers**
- **Intermediate frequency amplification and detection up to 25MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **FSK and ASK data receivers**

PIN CONFIGURATION



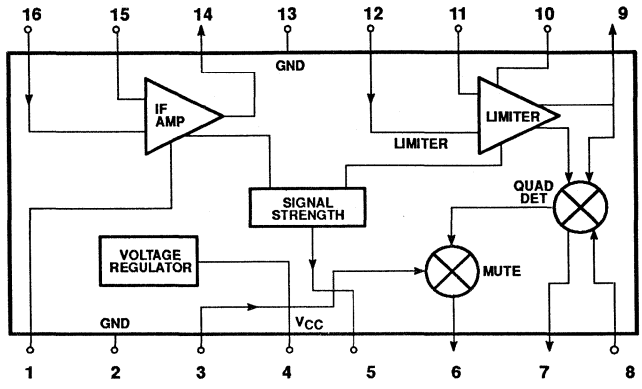
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16–Pin Plastic DIP	0 to +70°C	NE604AN
16–Pin Plastic SOL (Surface–mount)	0 to +70°C	NE604AD
16–Pin Plastic DIP	–40 to +85°C	SA604AN
16–Pin Plastic SOL (Surface–mount)	–40 to +85°C	SA604AD

High Performance Low Power FM IF System

NE/SA604A

BLOCK DIAGRAM



High Performance Low Power FM IF System — NE/SA604A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range NE604A SA604A	0 to +70 –40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

DC ELECTRICAL CHARACTERISTICS V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE604A			SA604A			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at T_A = 25°C; V_{CC} = ±6V, unless otherwise stated. IF frequency = 455kHz; IF level = –47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C–message weighted filter and de–emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE604A			SA604A			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input limiting –3dB	Test at Pin 16		–92			–92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		30	34		dB
	Recovered audio level	15nF de–emphasis	110	175	250	80	175	260	mV_{RMS}
	Recovered audio level	150pF de–emphasis		530			530		mV_{RMS}
THD	Total harmonic distortion		–35	–42		–34	–42		dB
S/N	Signal–to–noise ratio	No modulation for noise		73			73		dB
	RSSI output[1]	RF level = –118dBm	0	160	550	0	160	650	mV
		RF level = –68dBm	2.0	2.65	3.0	1.9	2.65	3.1	V
		RF level = –18dBm	4.1	4.85	5.5	4.0	4.85	5.6	V
	RSSI range	R_4 = 100k (Pin 5)		90			90		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±1.5			±1.5		dB
	IF input impedance		1.4	1.6		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		1.4	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ

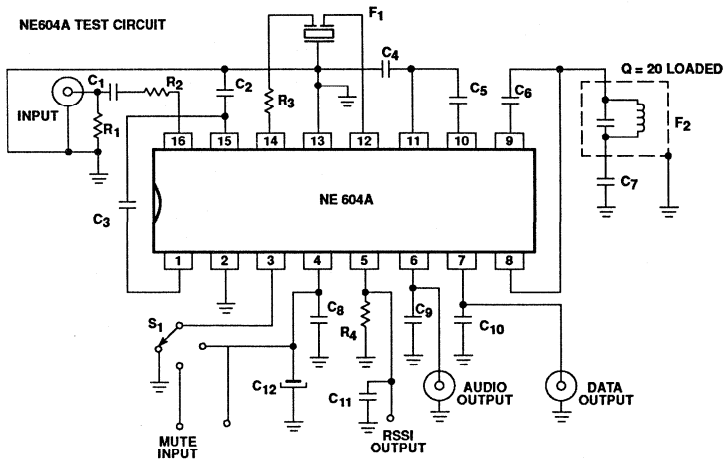
NOTE:

1. NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

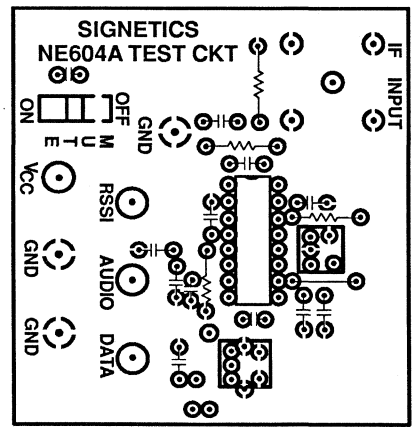
NE604 (50)	NE604A (1.5k)/NE605 (1.5k
–97dBm	–118dBm
–47dBm	–68dBm
+3dBm	–18dBm

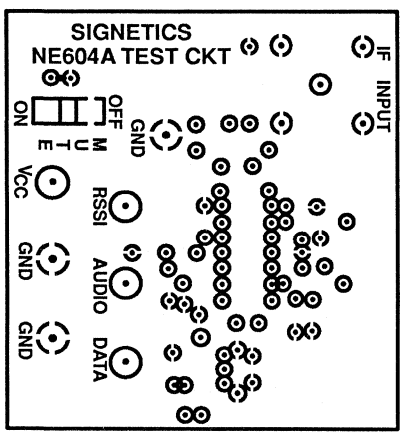
The NE605 and NE604A are both derived from the same basic die. The NE605 performance plots are directly applicable to the NE604A.

High Performance Low Power FM IF System — NE/SA604A



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000–Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz IF Filter
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film





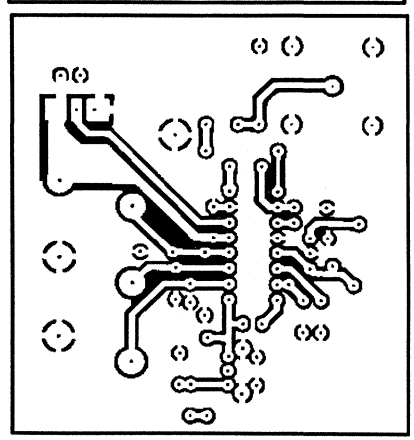


Figure 1. NE/SA604A Test Circuit

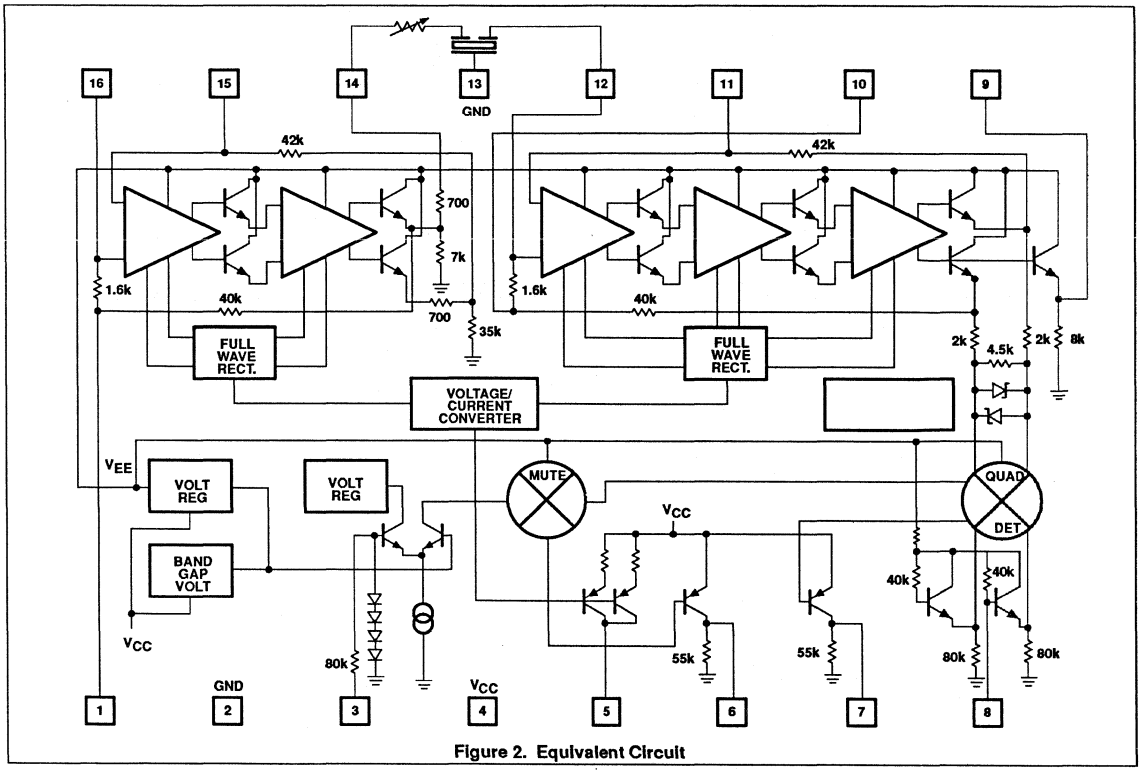


Figure 2. Equivalent Circuit

High Performance Low Power FM IF System — NE/SA604A

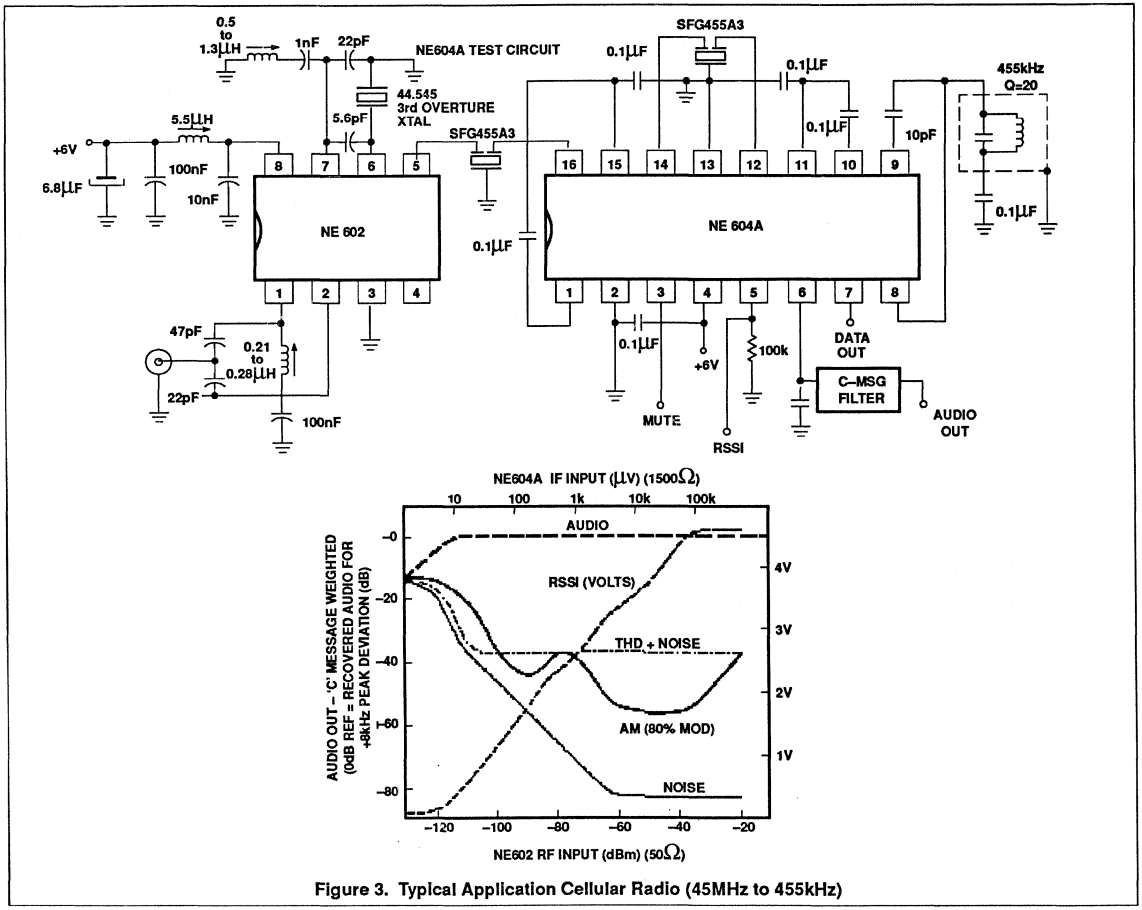


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA604A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA604A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA604A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub–systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log–limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

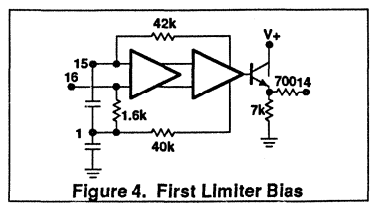


Figure 4. First Limiter Bias

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields)

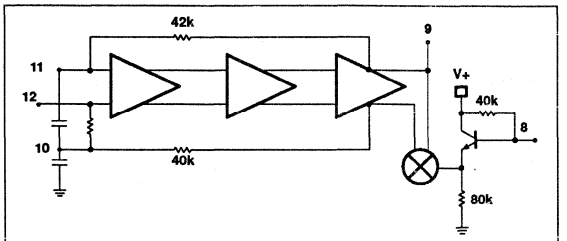


Figure 5. Second Limiter and Quadrature Detector

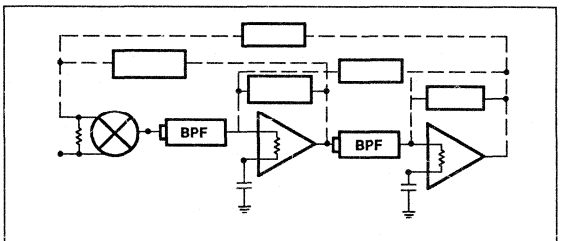


Figure 6. Feedback Paths

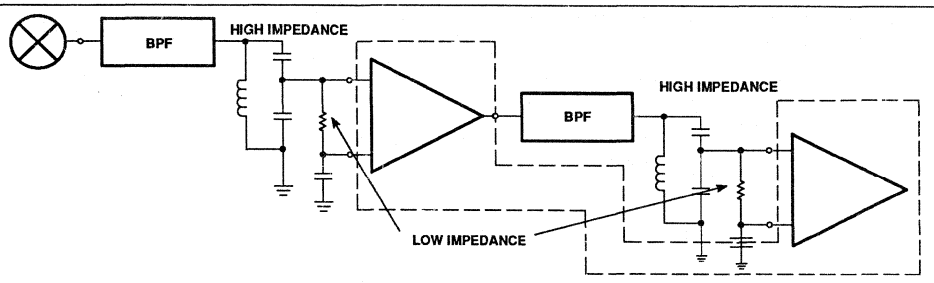


Figure 7. Terminating High Impedance Filters with Transformation to Low Impedance

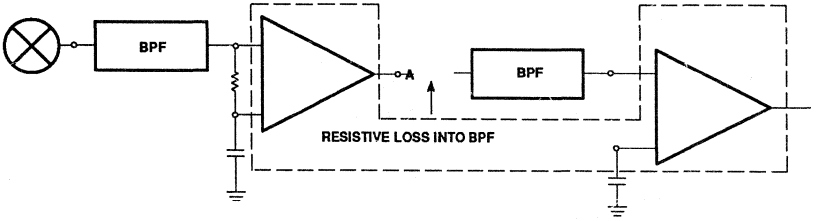


Figure 7. Low Impedance Termination and Gain Reduction
Figure 7. Practical Termination

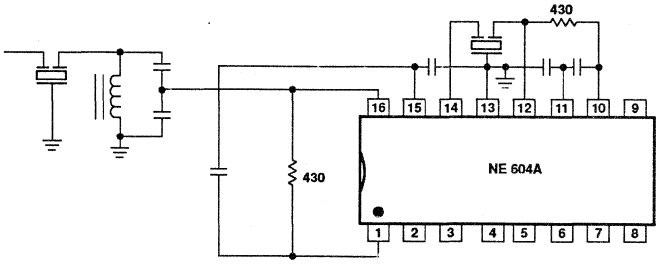


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 7. Reduced gain will result in reduced limiting sensitivity.

High Performance Low Power FM IF System — NE/SA604A

A feature of the NE604A IF amplifiers, which is not specified, is low phase shift. The NE604A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

Stability Considerations

The high gain and bandwidth of the NE604A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1μF monolithic right at the V_{CC} pin, and a 6.8μF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1μF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430W external resistors are applied in parallel to the internal 1.6kW load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non–existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE604A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single–ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non–linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first–order effects only.

Frequency Discriminator Design Equations for NE604A

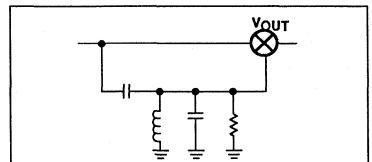


Figure 9.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 10 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$ with respect to the V_{IN}.

$$\text{If } V_{IN} = A \sin \omega t \Rightarrow V_O = A \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (3)$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \sin \omega t \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (4)$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (5)$$

$$= \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1 \frac{\omega_1}{\omega} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 10) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) $\Rightarrow$ Choose a Q = 20

The internal R of the 604A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174\text{pF}$ and $L = 0.7\text{mH}$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10\text{pF}$ and $C_P = 164\text{pF}$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1\text{pF}$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current–to–voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current–to–voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no–signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE604A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in–band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current–to–voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE604A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

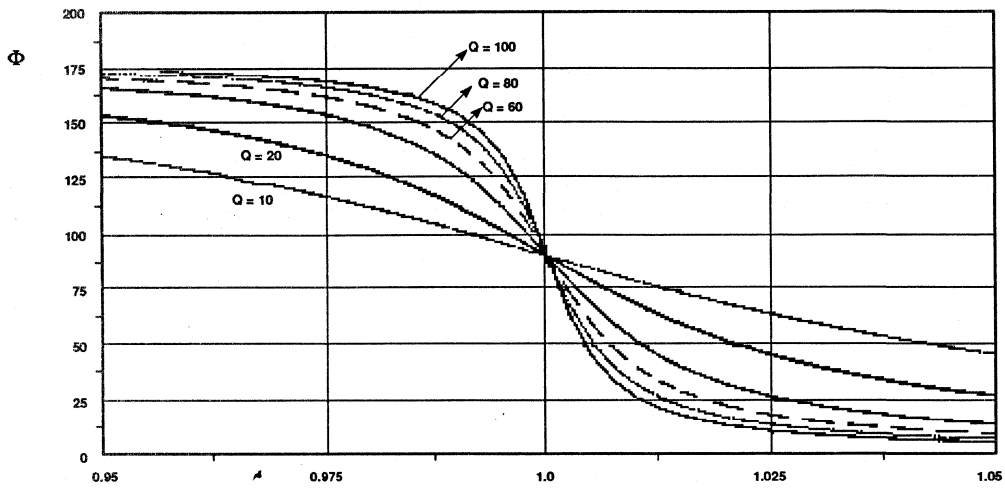


Figure 10. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

Document	853–1401
ECN No.	97959
Date of Issue	October 25, 1989
Status	Product Specification
RF Communications	

NE/SA605

High performance low power mixer FM IF system

DESCRIPTION

The NE/SA605 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA605 combines the functions of Signetics' NE602 and NE604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The NE/SA605 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package).

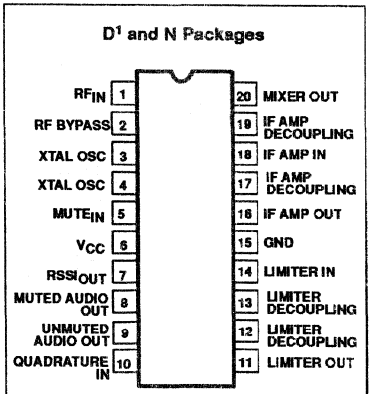
The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA605. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA605 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

D[1] and N Packages



NOTE:
1. Large SO (SOL) package only.

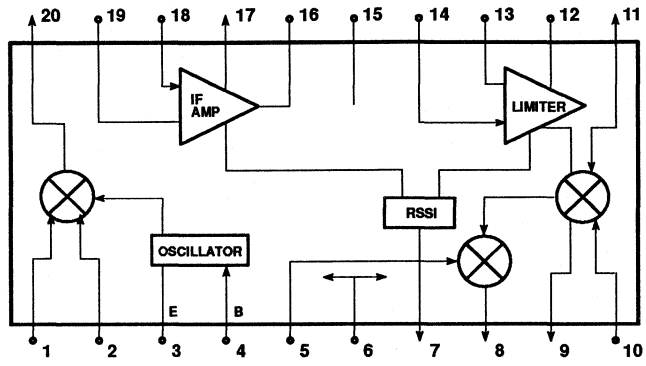
APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE605N
20-Pin Plastic SOL (Surface-mount)	0 to +70°C	NE605D
20-Pin Plastic DIP	-40 to +85°C	SA605N
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA605D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		–65 to +150	°C
T_A	Operating ambient temperature range	NE605	0 to +70	°C
		SA605	–40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		N package	75	°C/W

DC ELECTRICAL CHARACTERISTICS V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.7	6.5	4.55	5.7	6.55	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

Typical reading at T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step–up; IF frequency = 455kHz; R17 = 5.1k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C–message weighted filter and de–emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third–order input intercept point	f1 = 45.0; f2 = 45.06MHz		–10			–10		dBm
	Conversion power gain	Matched 14.5dBV step–up	10.5	13	14.5	10	13	15	dB
		50Ω source		–1.7			–1.7		dB
	RF input resistance	Single–ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting –3dB, R_{17} = 5.1k	Test at Pin 18		–113			–113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de–emphasis	110	150	250	80	150	260	mV_{RMS}

High performance low power mixer FM IF system NE/SA605

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Unmuted audio level, R_{I1} = 100k	150pF de-emphasis		480			480		mV
	SINAD sensitivity	RF level –118dB		16			16		dB
THD	Total harmonic distortion		–35	–42		–34	–42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = –118dBm	0	160	550	0	160	650	mV
		IF level = –68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = –18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	RSSI range	R_9 = 100kΩ Pin 16		90			90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		1.40	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ
RF/IF section (int LO)									
	Unmuted audio level	4.5V = V_{CC}, RF level = –27dBm		450			450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = –27dBm		4.3			4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA605 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of –10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

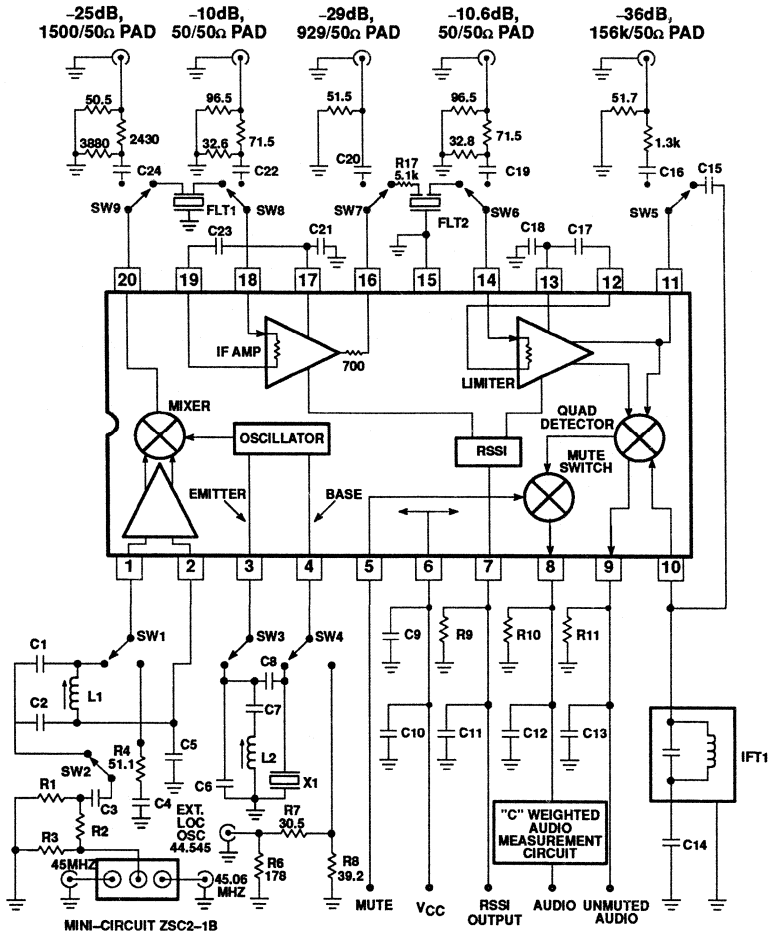
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

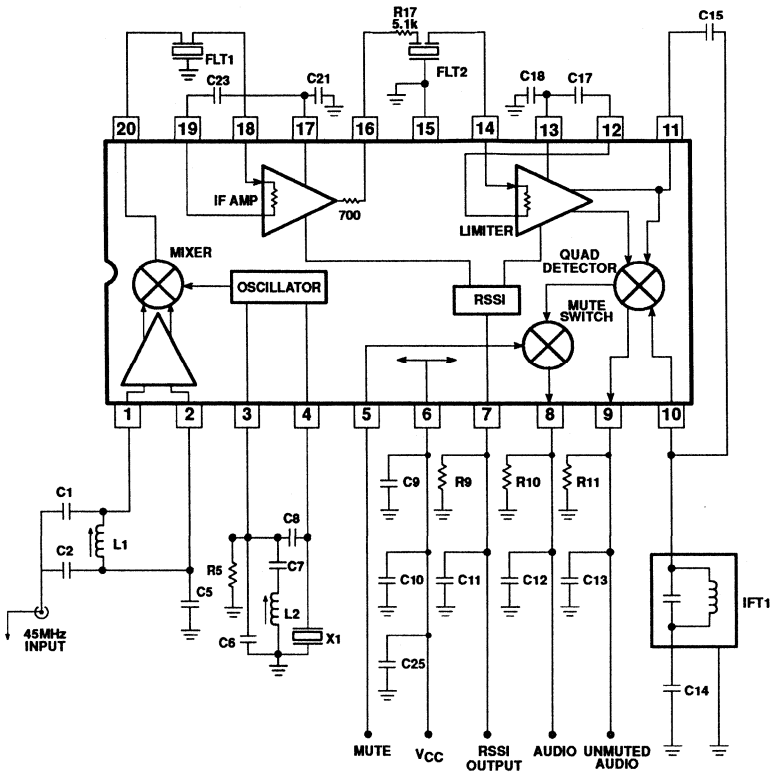
NOTE: dB(v) = 20log V_{OUT}/V_{IN}



Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	3.3μH nominal Toko 292CNS–T1046Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

Figure 1. NE/SA605 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	3.3μH nominal Toko 292CNS–T1046Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

Figure 2. NE/SA605 45MHz Application Circuit

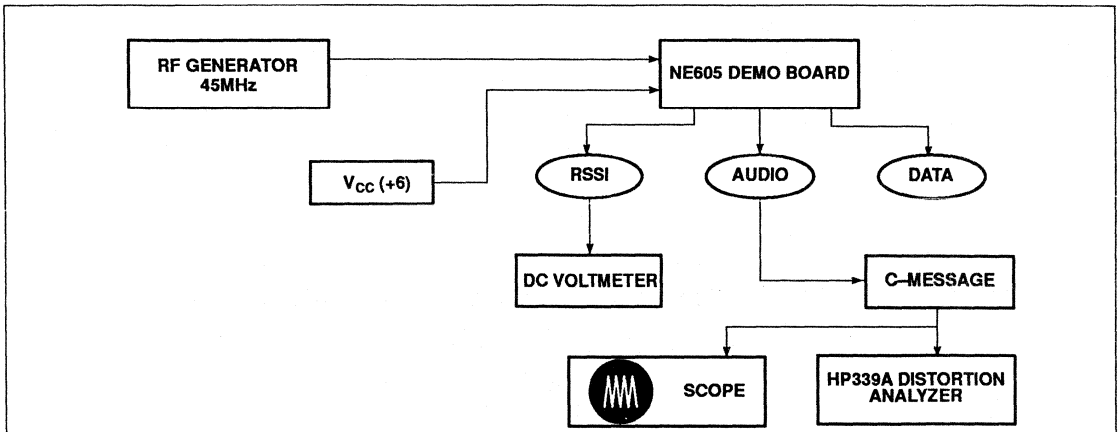


Figure 3. NE/SA605 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or –120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10–15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2–3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

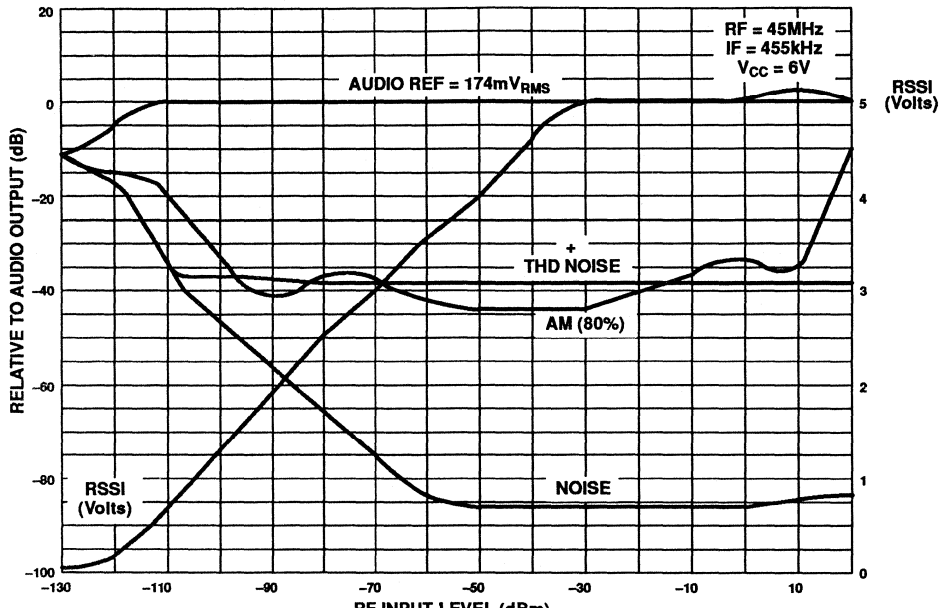


Figure 4. NE605 Application Board at 25°C

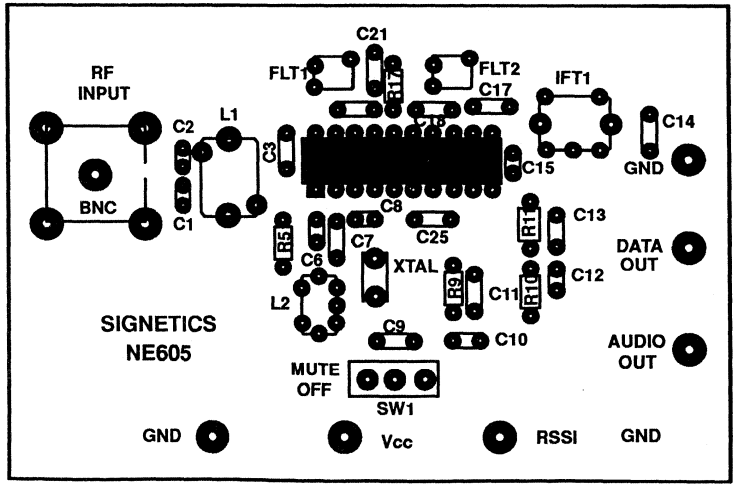
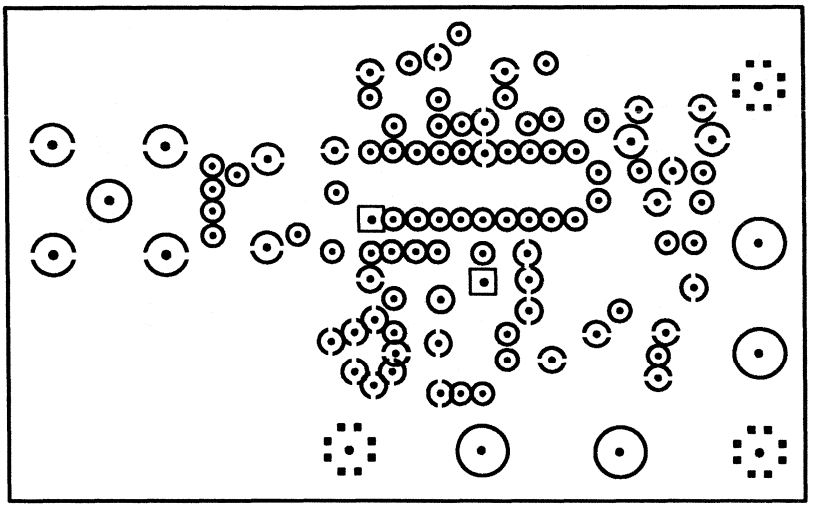
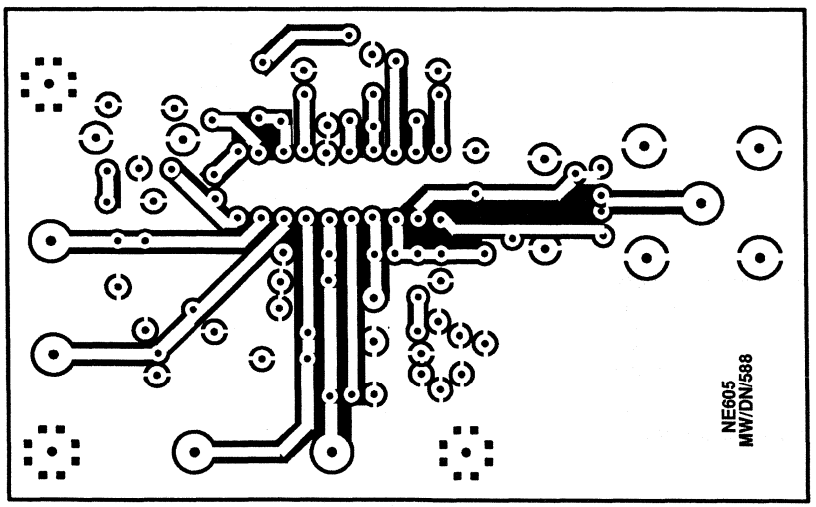


Figure 5. Component Placement for NE605 Application Circuit



TOP VIEW



BOTTOM VIEW

Figure 6. Layout for NE/SA605 Application Board

NE612
Double-Balanced Mixer and Oscillator

Product Specification

DESCRIPTION

The NE612 is a low-power VHF monolithic double-balanced mixer with onboard oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 49MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 49MHz is typically below 6dB and makes the device well suited for high performance cordless telephone. The low power consumption makes the NE612 excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE612 is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface mounted miniature package).

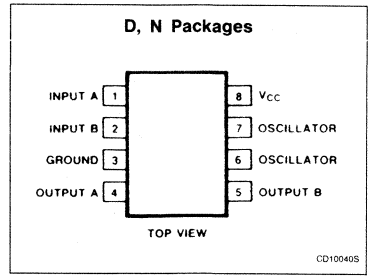
FEATURES

- **Low current consumption**
- **Low cost**
- **Operation to 500MHz**
- **Low radiated energy**
- **Low external parts count; suitable for crystal/ceramic filter**
- **Excellent sensitivity, gain, and noise figure**

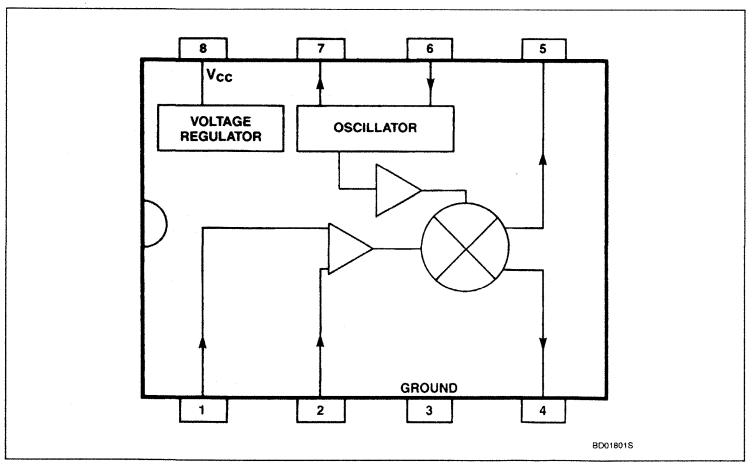
APPLICATIONS

- **Cordless telephone**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **Sonabuoys**
- **Communications receivers**
- **Broadband LANs**
- **HF and VHF frequency conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE612N
8-Pin Plastic SO	0 to +70°C	NE612D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

AC/DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 6V, Figure 1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	3.0	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 49MHz			5.0		dB
	Third-order intercept point at 49MHz	RF_{IN} = −45dBm		−15		dBm
	Conversion gain at 49MHz		14	18		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3		pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

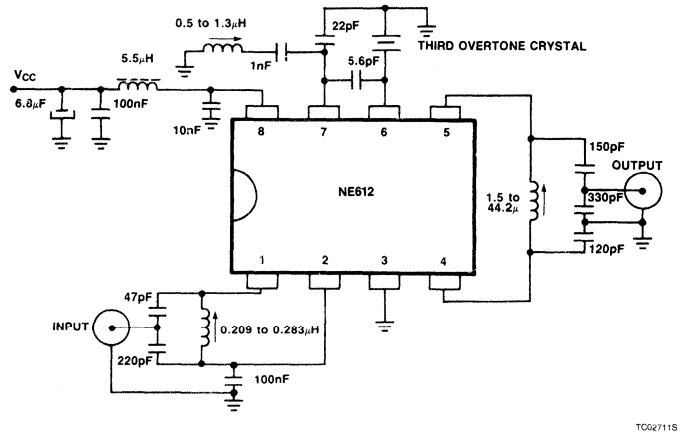


Figure 1. Test Configuration

DESCRIPTION OF OPERATION

The NE612 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE612 is designed for optimum low power performance. When used with the NE614 as a 49MHz cordless telephone system, the NE612 is capable of receiving −119dBm signals with a 12dB S/N ratio. Third-order intercept is typically −15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE612 should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE612 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k ‖ 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be 200mV$_{P-P}$ minimum to 300mV$_{P-P}$ maximum.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cordless telephones. In this circuit a third overtone parallel-mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

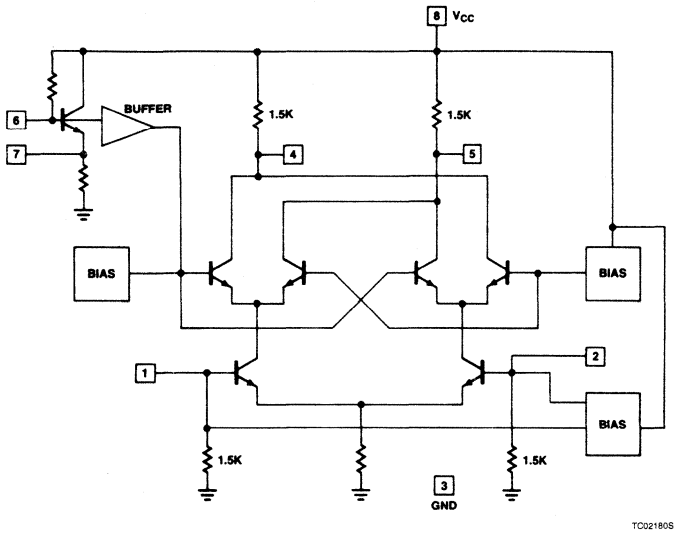
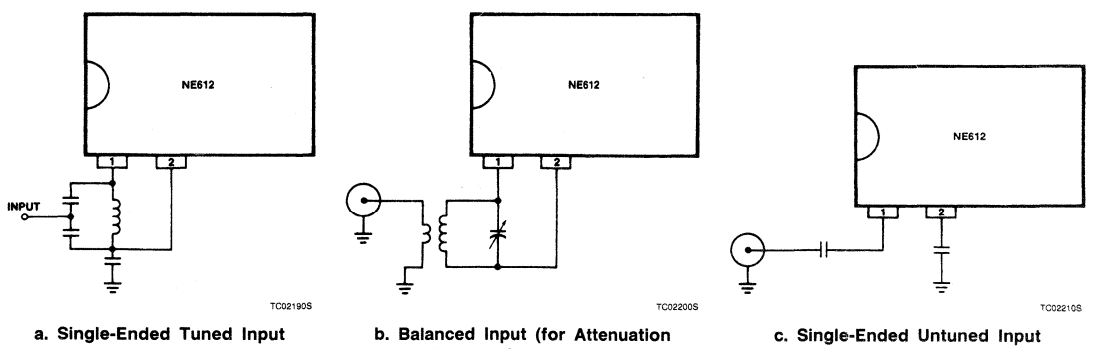


Figure 2. Equivalent Circuit

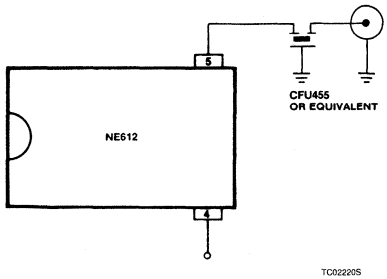


a. Single-Ended Tuned Input

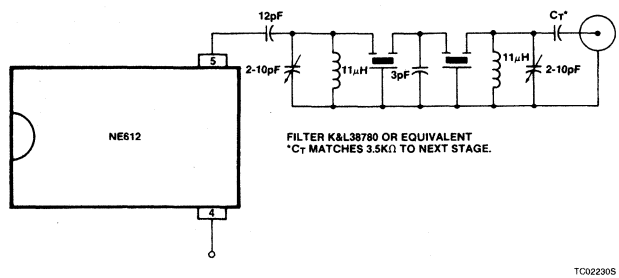
b. Balanced Input (for Attenuation of Second Order Products)

c. Single-Ended Untuned Input

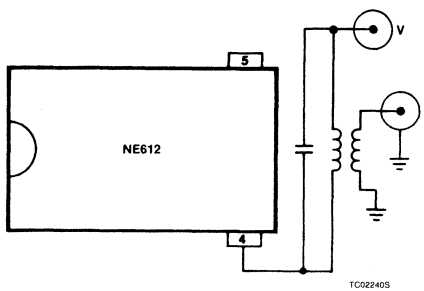
Figure 3. Input Configuration



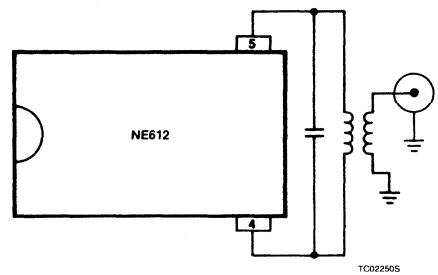
a. Single-Ended Ceramic Filter



b. Single-Ended Crystal Filter

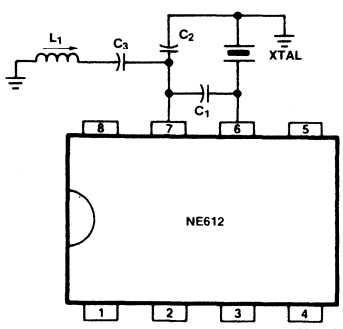


c. Single-Ended IFT

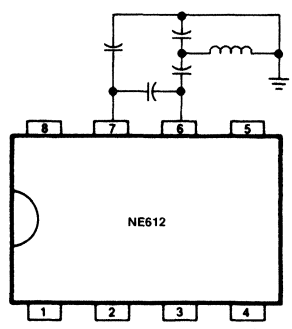


d. Balanced Output

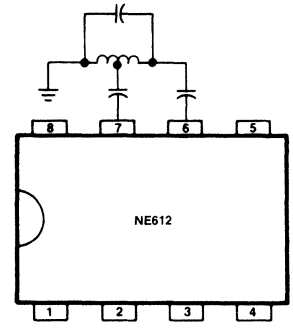
Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)

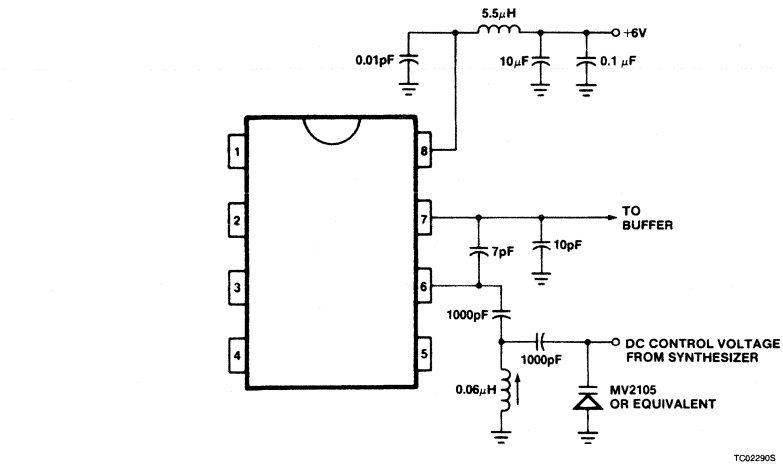


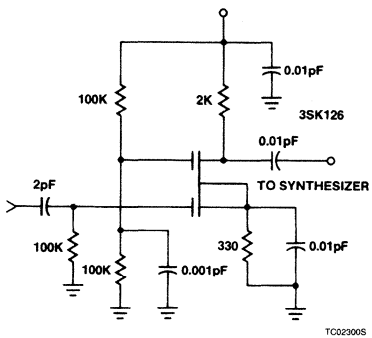
b. Colpitts L/C Tank Oscillator

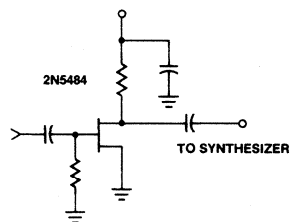


c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits







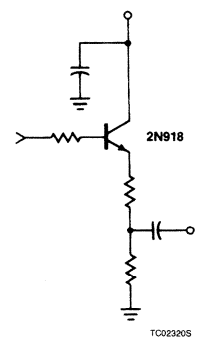


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

TEST CONFIGURATION

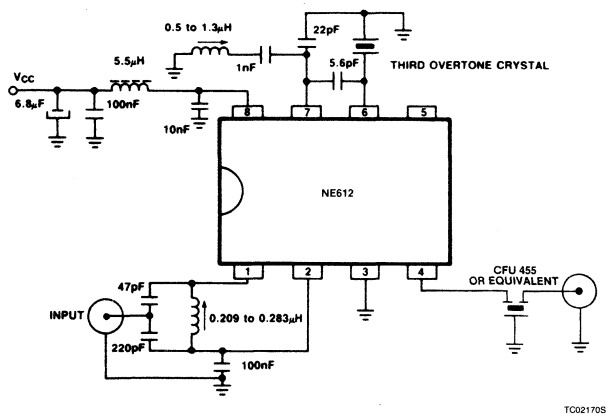


Figure 7. Typical Application for 46/49MHz Cordless Telephone

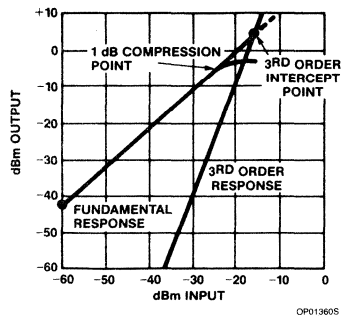


Figure 8. NE612 Third-Order Intermod and 1dB Compression Point Performance

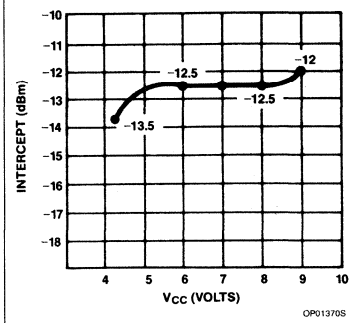


Figure 9. Input Third-Order Intercept Point vs V_{CC}

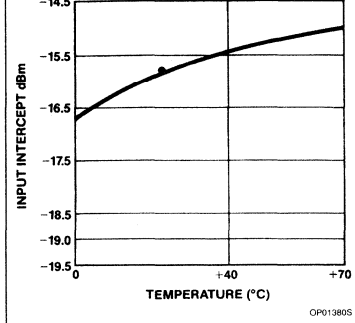


Figure 10. Third-Order Intercept Point vs Temperature

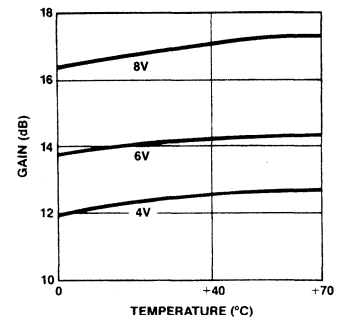


Figure 11

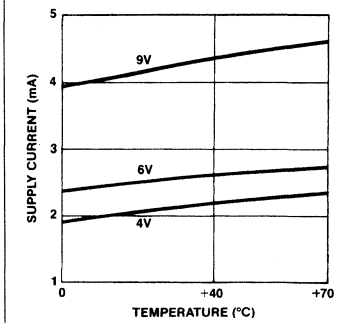


Figure 12

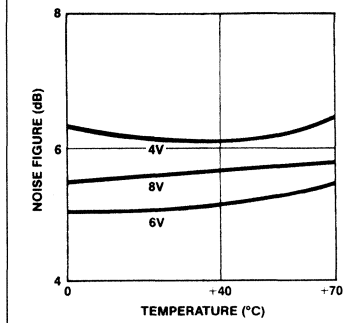


Figure 13

NE614
Low Power FM IF System

Product Specification

Linear Products

DESCRIPTION

The NE614 is a monolithic low power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The NE614 is available in a 16-lead dual in-line plastic package and 16-lead SO (surface-mounted miniature package).

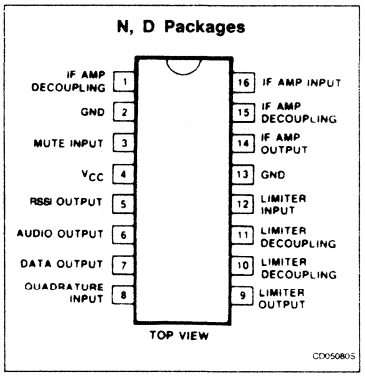
FEATURES

- **Low power consumption**
- **Logarithmic signal strength indicator**
- **Separate data output**
- **Audio output with muting**
- **Low external count; suitable for crystal/ceramic filters**
- **Excellent sensitivity**

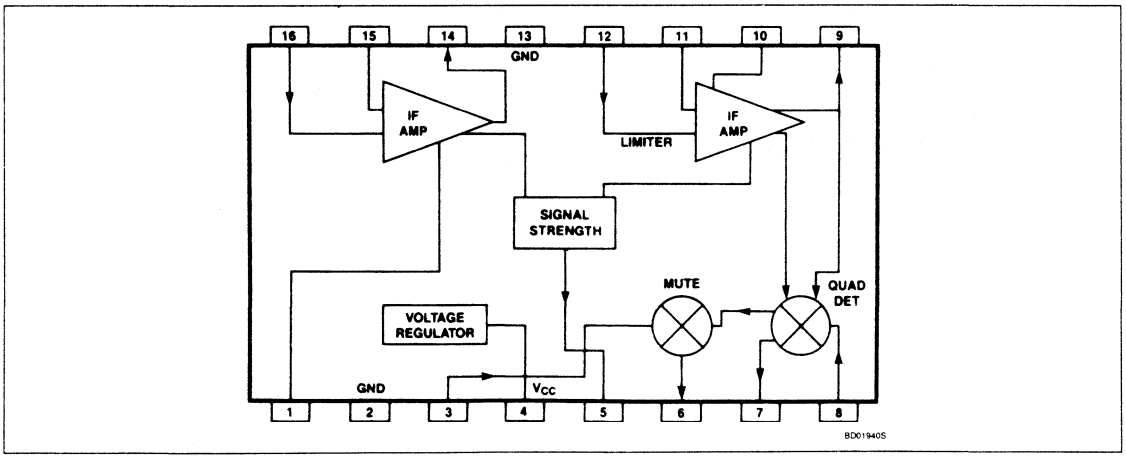
APPLICATIONS

- **Cellular Radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 15MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **Cordless telephone**
- **Remote control**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE614N
16-Pin Plastic SO	0 to +70°C	NE614D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range NE614	0 to +70	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise specified.

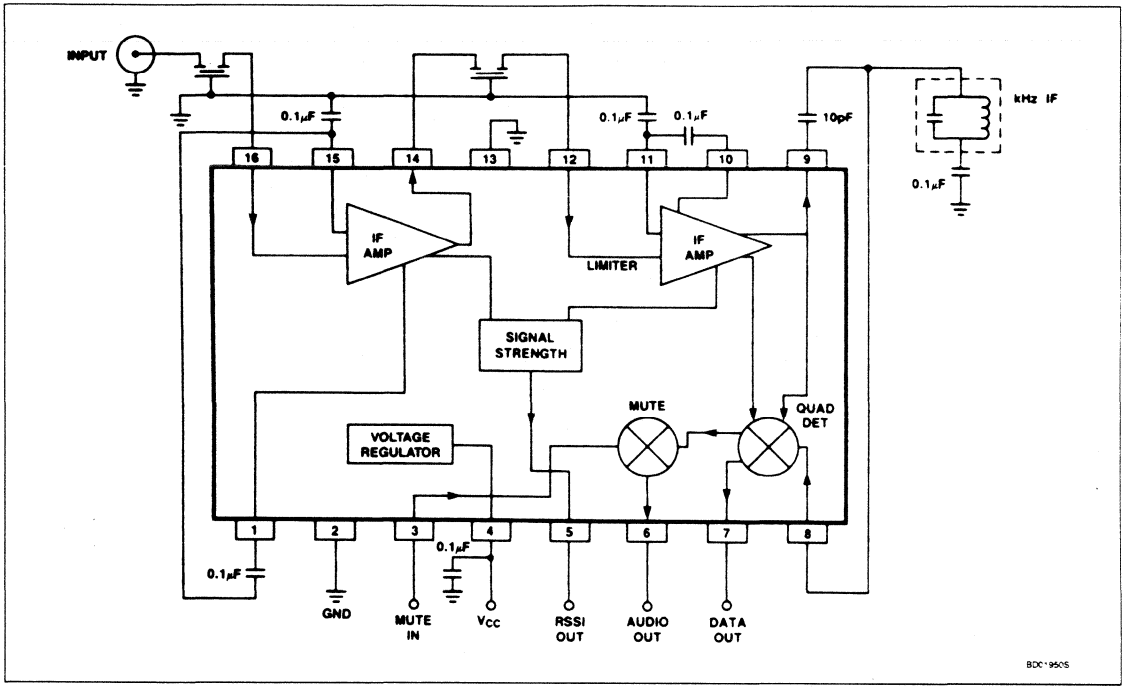
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain				3.0	mA
	Mute switch input threshold (on) (off)		 1.7		 1.0	 V V

AC ELECTRICAL CHARACTERISTICS

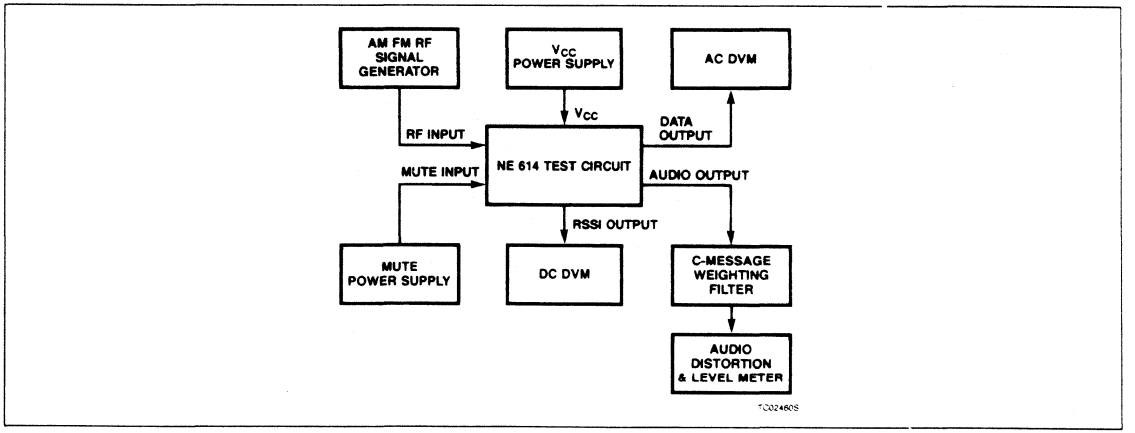
T_A = 25°C; V_{CC} = +6V, unless otherwise specified. RF frequency = 455kHz; RF level = −47dBm; FM modulation = 1kHz with +8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor.

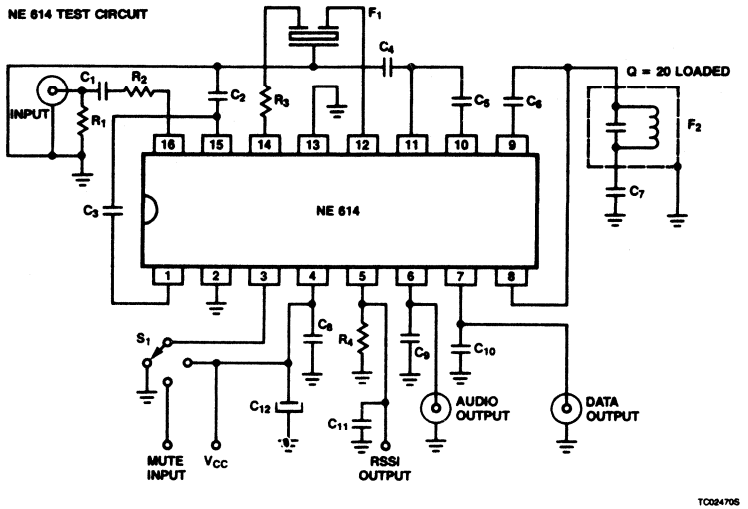
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input limiting − 3dB	Test at pin 16		−90	−80	dBm
	AM rejection	80% AM 1kHz	30			dB
	Recovered audio level	After C filter and de-emphasis capacitor	80	100		mV_{RMS}
	Recovered data level		250	350		mV_{RMS}
	SINAD sensitivity	RF level − 97dBm	8	12		dB
THD	Total harmonic distortion		−35			dB
S/N	Signal-to-noise ratio	No modulation		75		dB
	IF input impedance		1.5			kΩ
	IF output impedance		1.0			kΩ
	Limiter input impedance		1.5			kΩ
	Quadrature detector data output impedance		50			kΩ
	Muted audio output impedance			50		kΩ

TYPICAL APPLICATION



TEST SETUP





NOTES:
C1 10nF +80 – 20% 63V K10000-Z5V Ceramic
C2 100nF ± 10% 50V Polyester
C3 100nF ± 10% 50V Polyester
C4 100nF ± 10% 50V Polyester
C5 100nF ± 10% 50V Polyester
C6 10pF ± 2% 100V NPO Ceramic
C7 100nF ± 10% 50V Polyester
C8 100nF ± 10% 50V Polyester
C9 15nF ± 10% 50V Polyester
C10 150pF ± 2% 100V N1500 Ceramic
C11 1nF ± 10% 100V K2000-Y5P Ceramic
C12 6.8μF ± 20% 25V Tantalum
F1 455kHz Ceramic Filter Murata SFG455A3
F2 455kHz IF Filter A2549
R1 51Ω ± 1% 1/4W Metal Film
R2 1500Ω ± 1% 1/4W Metal Film
R3 1500Ω ± 5% 1/8W Carbon Composition
R4 100kΩ ± 1% 1/4W Metal Film

Figure 1. NE614 Test Circuit and Parts List

DESCRIPTION OF OPERATION

The NE614 is comprised of five subsystems for IF signal processing. These subsystems, two IF limiting amplifiers, quadrature detector, audio mute, and logarithmic signal strength, can be configured to satisfy many high-performance or low power systems objectives. Internal temperature compensated bias regulation completes the circuitry.

Figure 2 shows the equivalent circuits of the NE614.

Limiting Amplifiers

The NE614 has two independent limiting IF amplifiers. The first has a typical gain of 30dB. The second typically has 60dB gain. Both have 1.5k nominal input impedance and 15MHz bandwidth. The output impedance of the first limiter is approximately 1kΩ. These impedances permit direct interface with popular ceramic filters such as the SFU455. On the surface, the 1k output of the first limiter would not seem correct. However, approximately 6dB insertion loss is required between limiter stages to optimize the linearity of the signal strength indicator. The impedance mismatch has little effect on passband. Use of an interstage filter reduces wide-band noise. A DC blocking capacitor or L/C filter can also be used.

As the signal frequency increases, the 90dB total gain can become a source of instability. Figure 3 shows the limiters as a closed-loop system with stray capacitance and the equivalent AC input impedance setting the loop gain.

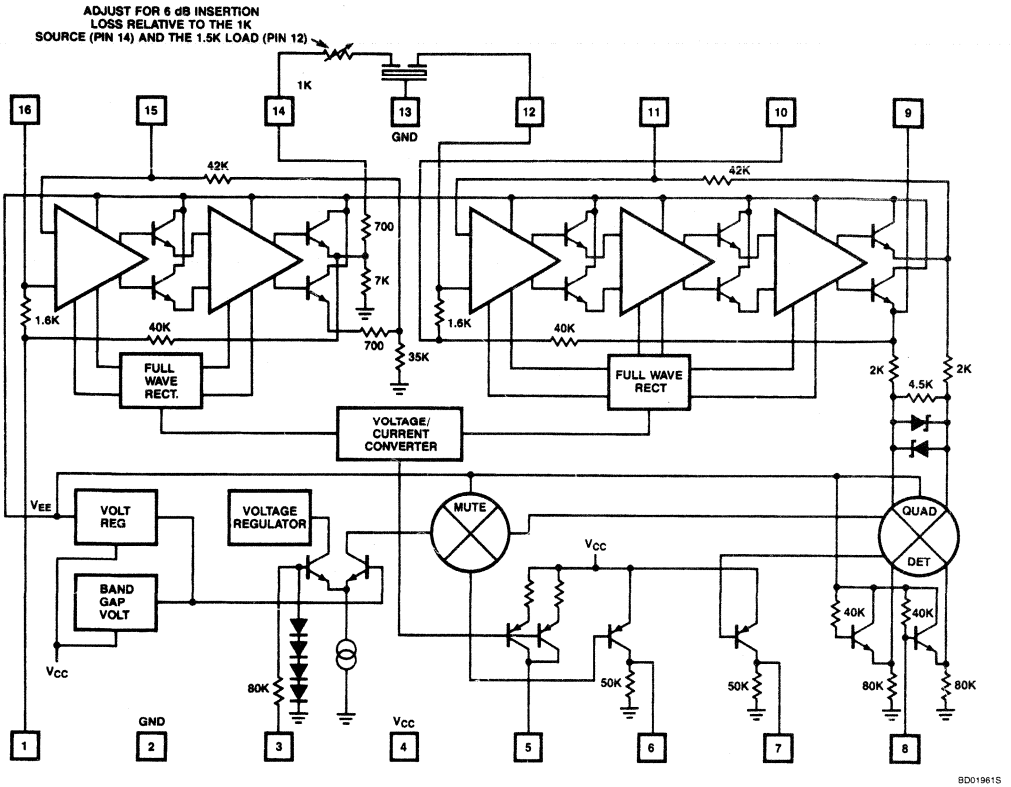


Figure 2. Equivalent Circuit

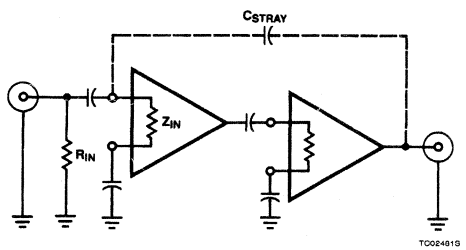
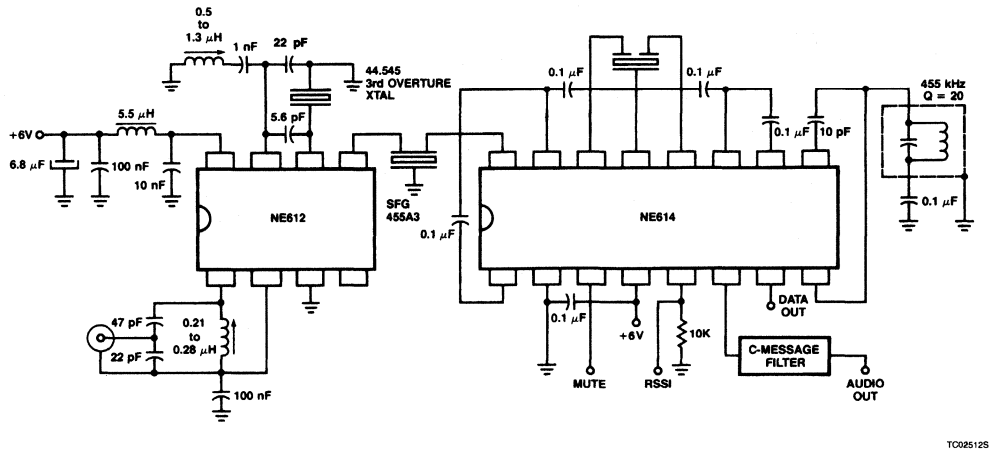


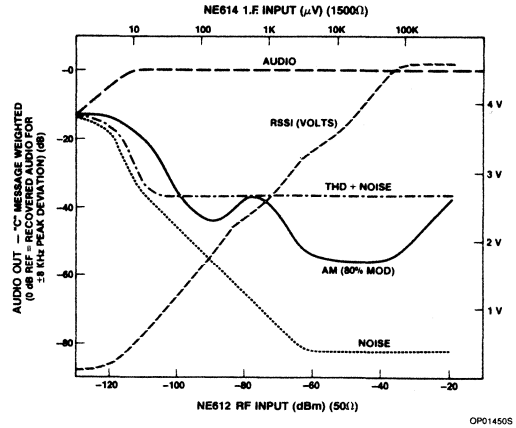
Figure 3. Considerations for Stability

The equivalent AC attenuation factor from the output to the input must be greater than 90dB or oscillation can occur. The input impedance of the device is nominally 1.5k. The stray layout capacitance is a frequency-dependent impedance so that as the frequency of operation or the value of stray capacitance increases, the output-to-input attenuation factor decreases. Keep stray capacitance low by using good RF layout technique. Sockets should be avoided above 455kHz.

Good RF layout is the proper way to avoid instability. However, if system constraints require, stability can be achieved by only using one of the limiting amplifiers, or by adding a resistance, R_{IN}, which will increase the attenuation factor.



a. NE614 Application Circuit



b. Typical Application Circuit Performance

Figure 4

Adding an input resistor is an easy way to reduce the attenuation factor, but may make correct termination of interstage filters difficult or impossible. At 455kHz instability should not be a problem if reasonable RF layout is used. Figure 4a indicates a 455kHz circuit configuration which should serve as a reasonable starting point for many applications. This circuit is configured for 46/49MHz cordless telephone.

Quadrature Detector

The detector of the NE614 is a four quadrant multiplier of the Gilbert cell type. It can be used for frequency or amplitude demodulation. Figure 4b indicates a typical quadrature FM configuration. Fully limited in-phase signal is applied to the multiplier internally. 90° phase phase shift is accomplished with the L/C tuned circuit connected directly to Pin 8 and and capacitively to Pin 9. Because of the DC bias of the NE614, the phase shift network must be returned to ground through a low impedance capacitor. Recovered signal is continuously available at Pin 7 or on a switched basis at Pin 6.

Table 1. System Parameters as Applied to Figure 4a

$\Delta\omega$	=	2π*8kHz
ω_0	=	2π*455kHz
CP	=	180pF
RPU	=	233K
RPL	=	40K
LP	=	644μH
Q	≈	20

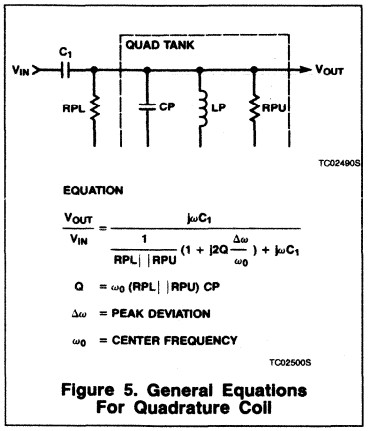


Figure 5. General Equations For Quadrature Coil

The quadrature coil or crystal/ceramic discriminator affects three system parameters: Bandwidth, linearity, and detected signal amplitude. Figure 6 shows three quadrature curves.

Curve A has the most narrow bandwidth and high peak-to-peak output versus frequency deviation corresponding to a high Q network. Curve C is very low Q with good linearity and shows how very large deviations can be processed. Curve B shows how the quadrature network can cause non-linearity in the detected output. A typical loaded Q for the 455kHz quadrature coil of Figure 4 is 20. Using the test circuit of Figure 4 with an input of −47dBm, the recovered audio is typically 90mV$_{RMS}$ with −35dB distortion.

While the NE614 was designed principally for FM applications, the detector can be used for synchronous amplitude demodulation if the carrier is limited through the internal circuitry and AGC'd external to the device. The AGC'd signal is applied to Pin 8 instead of a quadrature signal. The signal strength indicator can control AGC. A low-pass filter on the output completes the demodulator. Figure 7 shows the equivalent circuit.

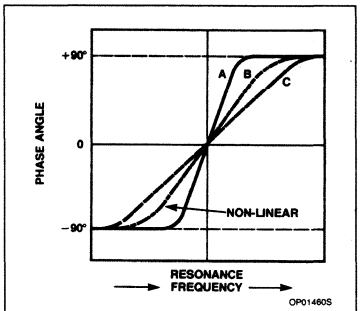


Figure 6. Quadrature

Audio Mute

An electronic switch permits muting or squelch of one of the demodulated outputs. The data (unmuted output) and audio (muted output) both have 50kΩ output impedance and their detected signals are 180 degrees out of phase with each other. The mute input (Pin 3) has a very high impedance and is compatible with three and five volt CMOS and TTL levels. Little or no DC level shift occurs after muting when the quadrature detector is adjusted to the IF center frequency. Muting will attenuate the audio signal by more than 60dB and no voltage spikes will be generated by muting.

Signal Strength Indicator

The logarithmic signal strength indicator is a current source output with maximum source current of 50μA. The signal strength indicator's transfer function is approximately 10μA per 20dB and is independent of IF frequency. The interstage filter must have a 6dB insertion loss to optimize slope linearity.

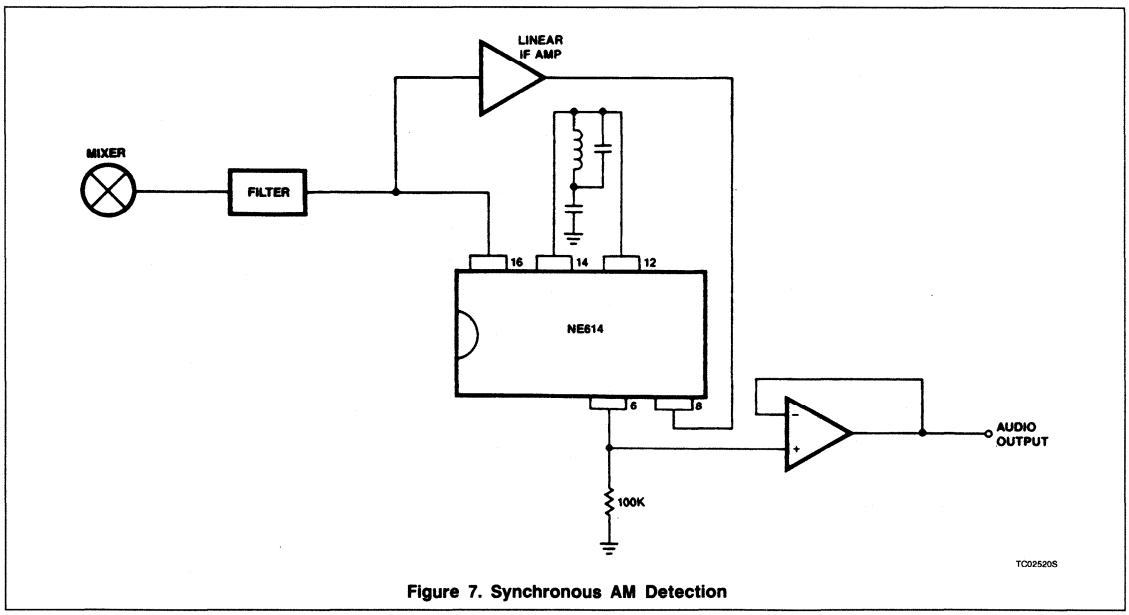


Figure 7. Synchronous AM Detection

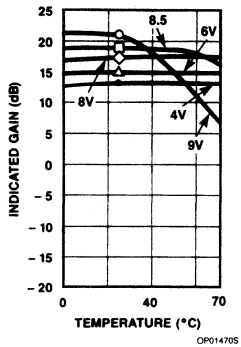


Figure 8. NE614 Indicated Gain vs Temperature and Voltage

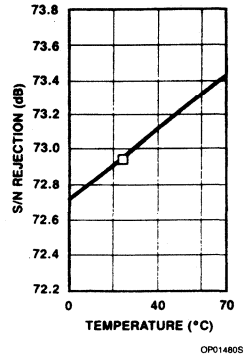


Figure 9. NE614 Signal-To-Noise Ratio vs Temperature

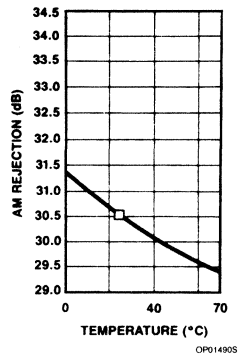


Figure 10. NE614 AM Rejection vs Temperature

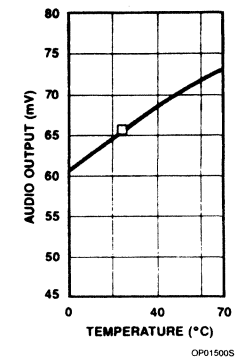


Figure 11. NE614 Audio Output vs Temperature

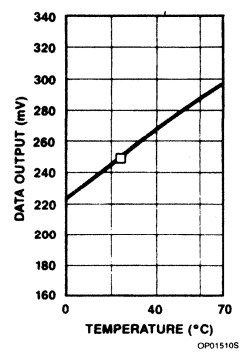


Figure 12. NE614 Data Output vs Temperature

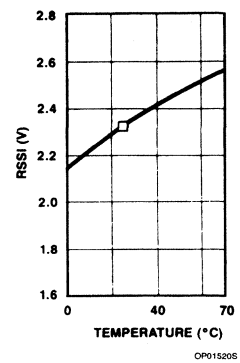


Figure 13. RSSI vs Temperature

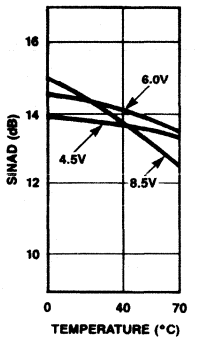


Figure 14. NE614 SINAD vs Temperature and V_{CC}

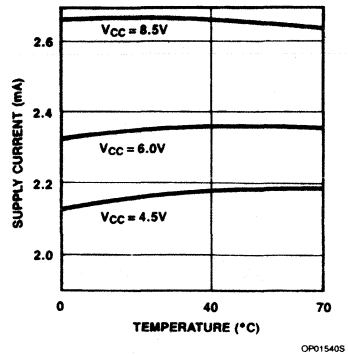


Figure 15. NE614 Supply Current vs Temperature

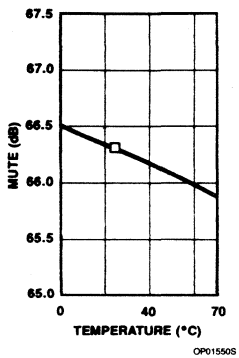


Figure 16. NE614 Muting vs Temperature

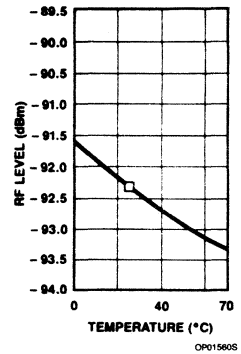


Figure 17. NE614 Limiting RF Level vs Temperature

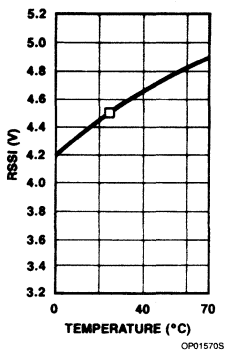


Figure 18. NE614 Large Signal Uncompensated RSSI Voltage vs Temperature

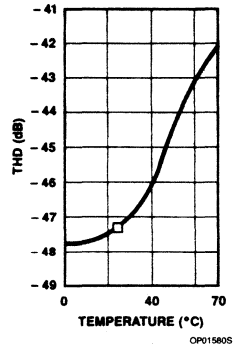


Figure 19. NE614 Total Harmonic Distortion vs Temperature

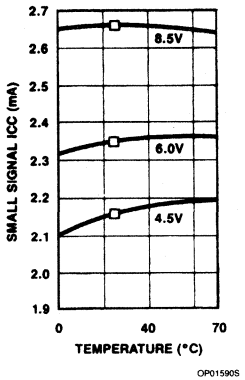


Figure 20. NE614 Supply Current vs Temperature and Voltage

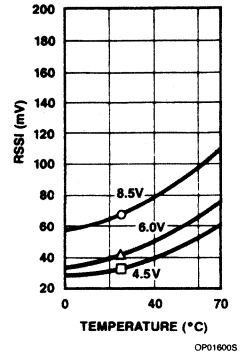


Figure 21. Small-Signal RSSI vs Temperature and Voltage

Document	853–0594
ECN No.	94867
Date of Issue	October 21, 1988
Status	Product Specification
Application Specific Product	

NE/SA614A

Low power FM IF system

DESCRIPTION

The NE/SA614A is an improved monolithic low–power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA614A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA614A is available in a 16–lead dual–in–line plastic and 16–lead SO (surface–mounted miniature) package.

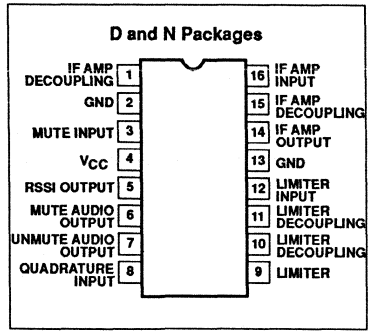
FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs – muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA614A meets cellular radio specifications

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

PIN CONFIGURATION

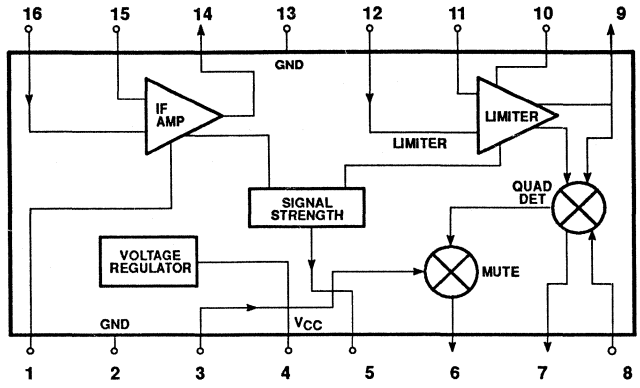


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16–Pin Plastic DIP	0 to +70°C	NE614AN
16–Pin Plastic SOL (Surface–mount)	0 to +70°C	NE614AD
16–Pin Plastic DIP	–40 to +85°C	SA614AN
16–Pin Plastic SOL (Surface–mount)	–40 to +85°C	SA614AD

Low power FM IF system | NE/SA614A

BLOCK DIAGRAM



Low power FM IF system — NE/SA614A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range NE614A SA614A	0 to +70 –40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

DC ELECTRICAL CHARACTERISTICS V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE614A			SA614A			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at T_A = 25°C; V_{CC} = ±6V, unless otherwise stated. IF frequency = 455kHz; IF level = –47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C–message weighted filter and de–emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA614A			
			MIN	TYP	MAX	
	Input limiting –3dB	Test at Pin 16		–92		dBm/50Ω
	AM rejection	80% AM 1kHz	25	33		dB
	Recovered audio level	15nF de–emphasis	60	175	260	mV_{RMS}
	Recovered audio level	150pF de–emphasis		530		mV_{RMS}
THD	Total harmonic distortion			–30	–42	dB
S/N	Signal–to–noise ratio	No modulation for noise		68		dB
	RSSI output[1]	RF level = –118dBm	0	160	800	mV
		RF level = –68dBm	1.7	2.50	3.3	V
		RF level = –18dBm	3.6	4.80	5.8	V
	RSSI range	R_4 = 100k (Pin 5)		80		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±2.0		dB
	IF input impedance		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ

NOTE:

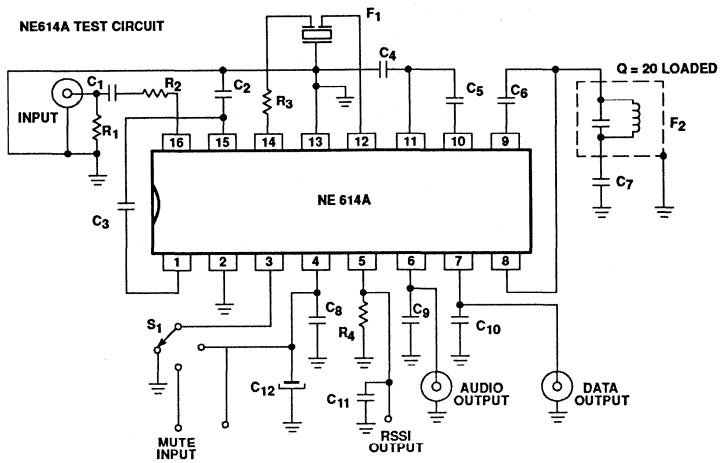
1. NE614A data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

NE614A (50)	NE614A (1.5k)/NE615 (1.5k
–97dBm	–118dBm
–47dBm	–68dBm
+3dBm	–18dBm

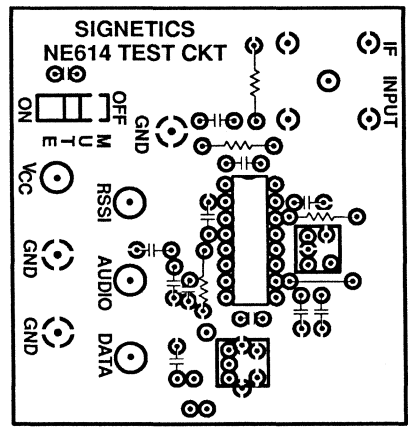
The NE615 and NE614A are both derived from the same basic die. The NE615 performance plots are directly applicable to the NE614A.

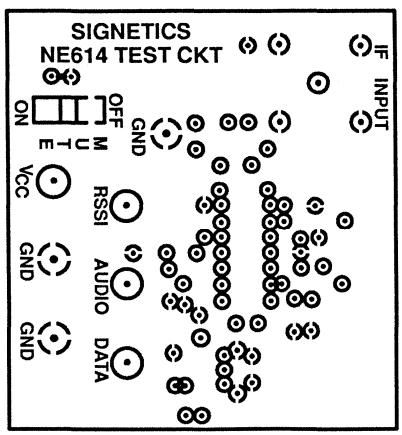
Low power FM IF system

NE/SA614A



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000–Y5P Ceramic
C12	6.8μF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz IF Filter
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film





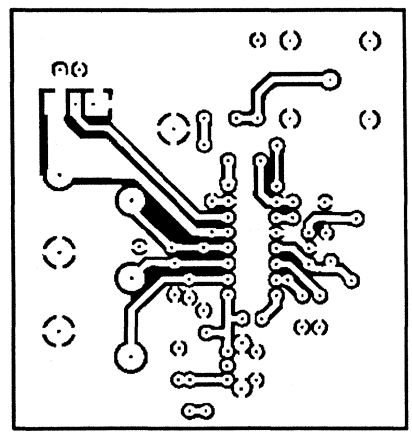


Figure 1. NE/SA614A Test Circuit

Low power FM IF system

NE/SA614A

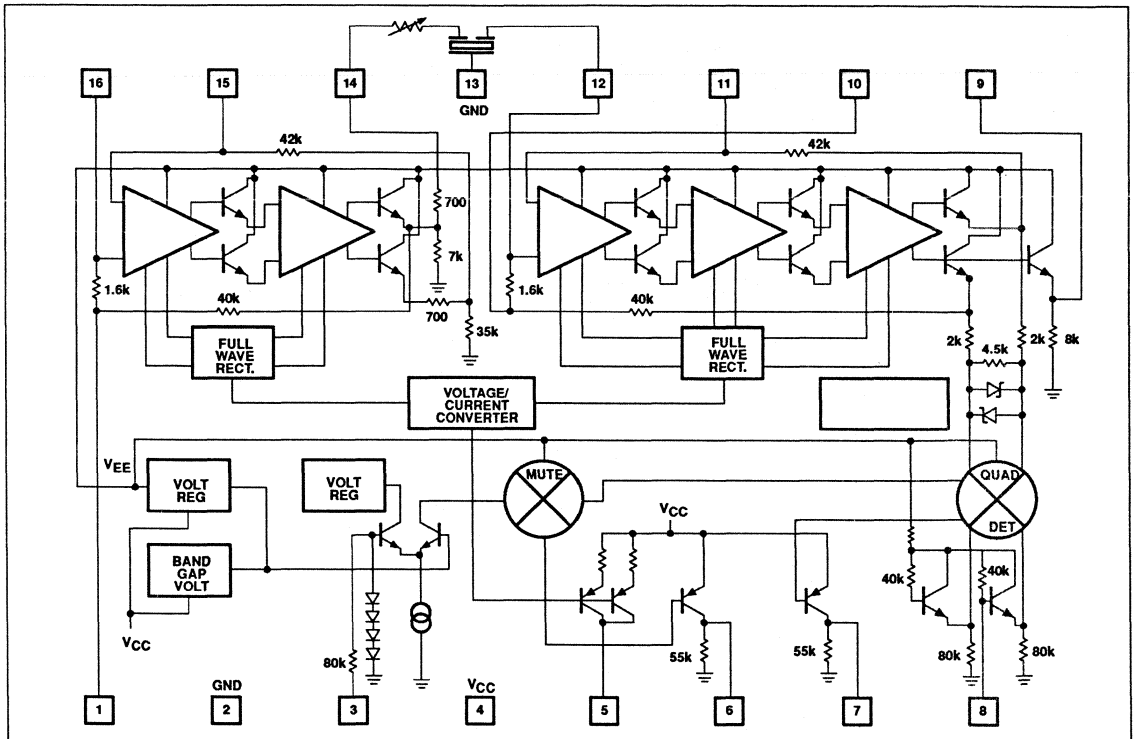


Figure 2. Equivalent Circuit

Low power FM IF system

NE/SA614A

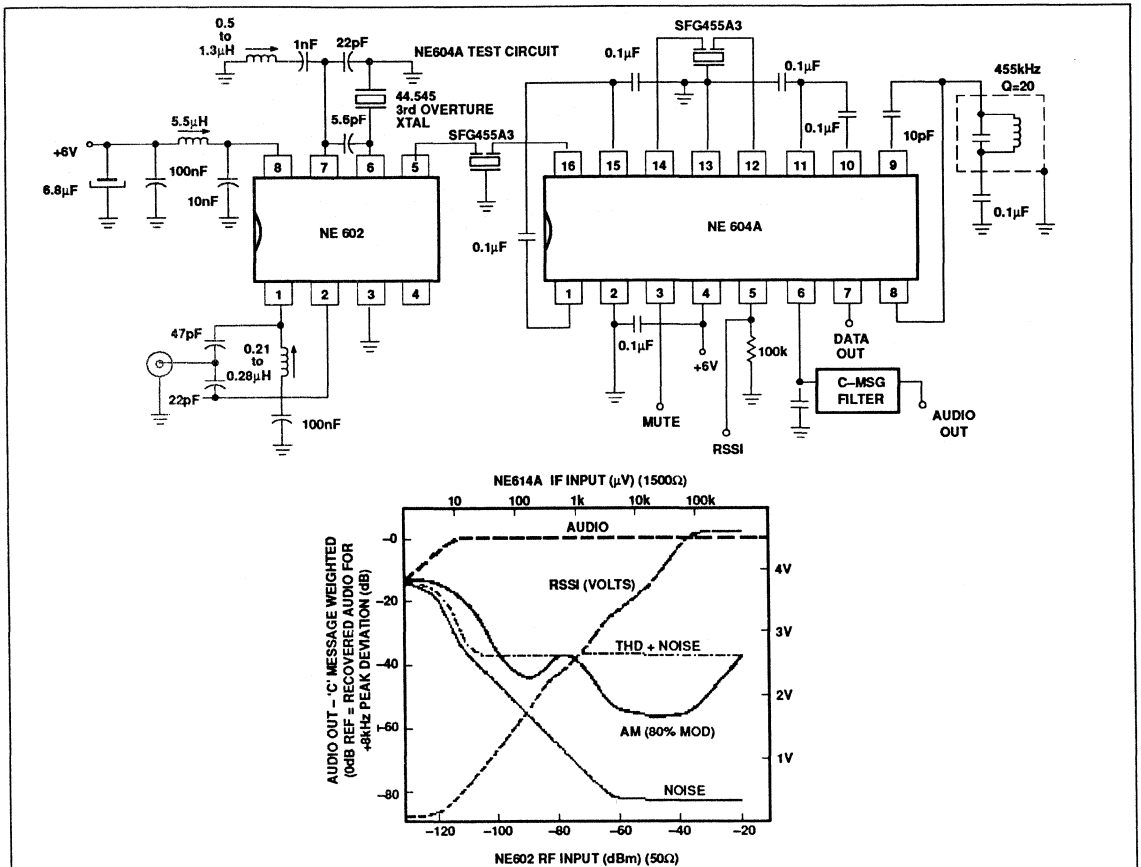


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA614A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA614A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA614A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

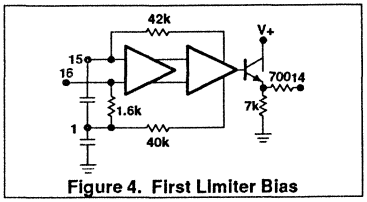


Figure 4. First Limiter Bias

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields)

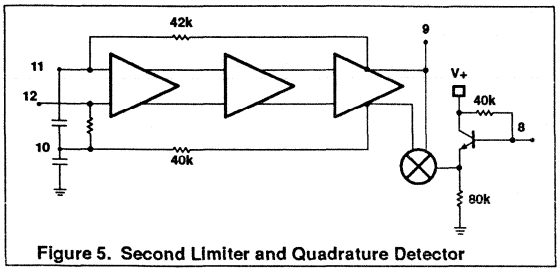


Figure 5. Second Limiter and Quadrature Detector

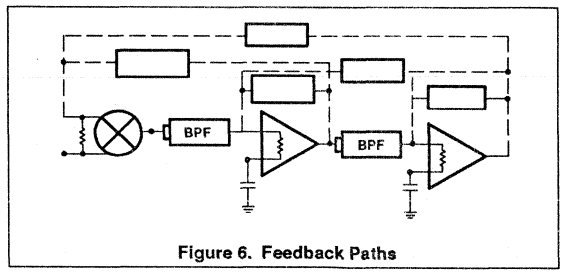


Figure 6. Feedback Paths

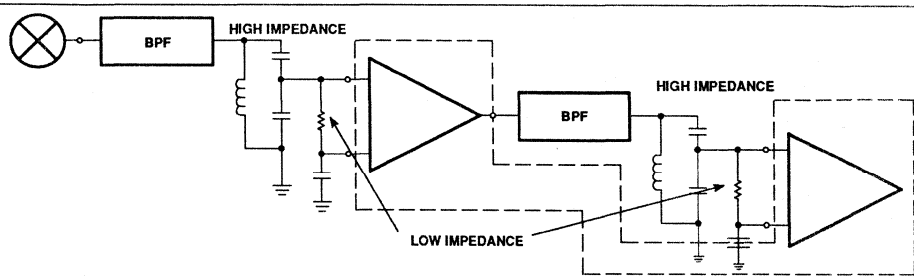


Figure 7. Terminating High Impedance Filters with Transformation to Low Impedance

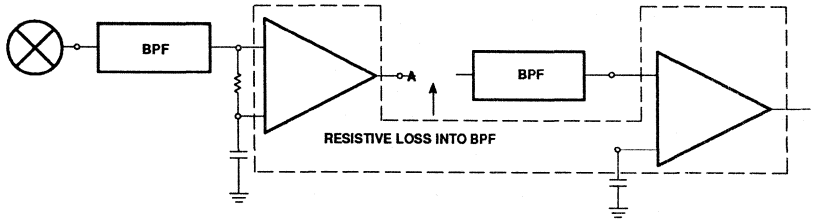


Figure 7. Low Impedance Termination and Gain Reduction
Figure 7. Practical Termination

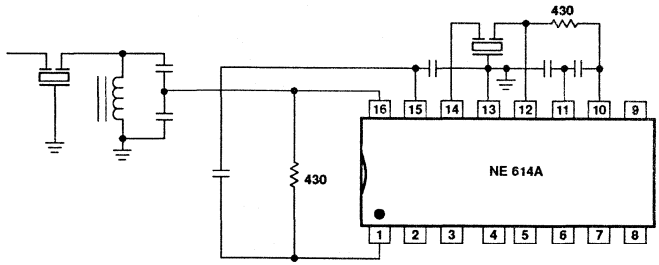


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in

Figure 7. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE614A IF amplifiers, which is not specified, is low phase shift. The NE614A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

Stability Considerations

The high gain and bandwidth of the NE614A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{CC} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430W external resistors are applied in parallel to the internal 1.6kW load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE614A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE614A

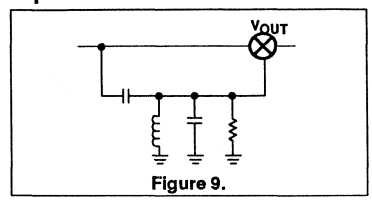


Figure 9.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1 \omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 10 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$ with respect to the V_{IN}.

$$\text{If } V_{IN} = A \sin \omega t \Rightarrow V_O = A \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (3)$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \sin \omega t \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (4)$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (5)$$

$$= \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1 \frac{\omega_1}{\omega} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5kHz}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 10) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) $\Rightarrow$ Choose a Q = 20

The internal R of the 614A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174pF$ and $L = 0.7mH$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10pF$ and $C_P = 164pF$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1pF$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current–to–voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current–to–voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers.

Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no–signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE614A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in–band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current–to–voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE614A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

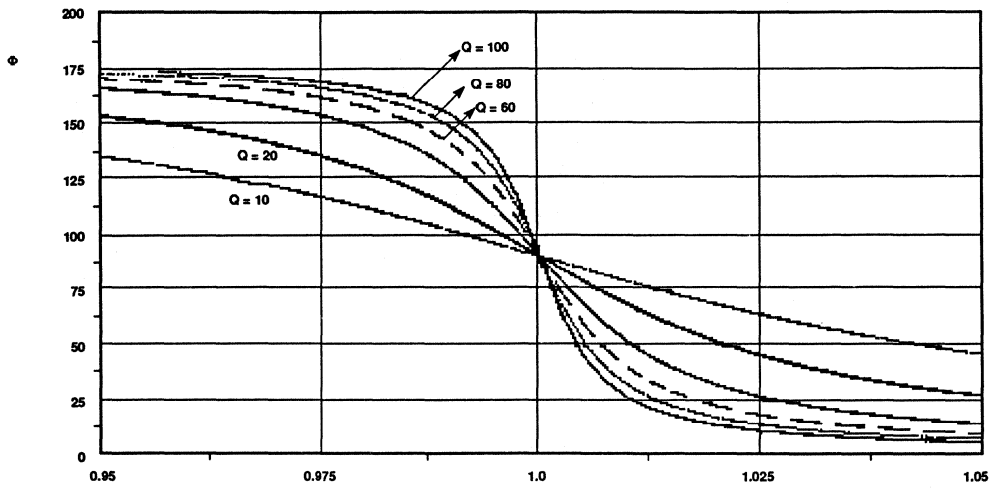


Figure 10. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

Philips Components

Document	853–1402
ECN No.	97977
Date of Issue	October 27, 1989
Status	Product Specification
RF Communications	

NE/SA615

High performance low power mixer FM IF system

DESCRIPTION

The NE/SA615 is a consumer monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA615 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package).

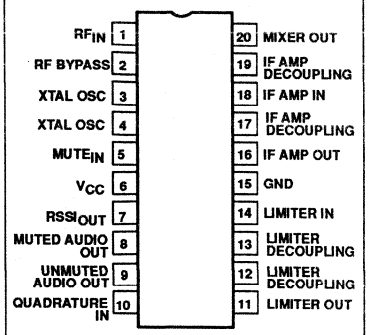
The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. the NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA605. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs – muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- ESD hardened

PIN CONFIGURATION

D[1] and N Packages



NOTE:
1. Large SO (SOL) package only.

APPLICATIONS

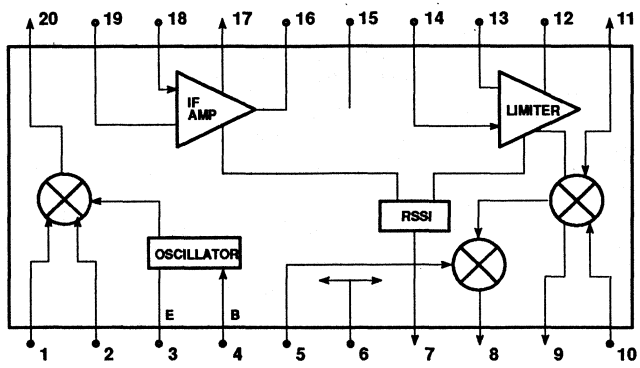
- Consumer cellular radio FM IF
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE615N
20-Pin Plastic SOL (Surface–mount)	0 to +70°C	NE615D
20-Pin Plastic DIP	–40 to +85°C	SA615N
20-Pin Plastic SOL (Surface–mount)	–40 to +85°C	SA615D

High performance low power mixer FM IF system NE/SA615

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range	NE615	0 to +70	°C
		SA615	-40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		N package	75	°C/W

DC ELECTRICAL CHARACTERISTICS V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA615			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain			5.7	7.4	mA
	Mute switch input threshold (ON)		1.7			V
	(OFF)				1.0	V

AC ELECTRICAL CHARACTERISTICS

Typical reading at T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz +14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA615			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order input intercept point	f1 = 45.00; f2 = 45.06MHz		-12		dBm
	Conversion power gain	Matched 14.5dBV step-up	8.0	13		dB
		50Ω source		-1.7		dB
	RF input resistance	Single-ended input	3.0	4.7		kΩ
	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.50		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-109		dBm
	AM rejection	80% AM 1kHz	25	33	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	60	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		530		mV

High performance low power mixer FM IF system NE/SA615

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA615			
			MIN	TYP	MAX	
	SINAD sensitivity	RF level -118dB		12		dB
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	IF RSSI output, R_g = 100kΩ[1]	IF level = -118dBm	0	160	800	mV
		IF level = -68dBm	1.7	2.5	3.3	V
		IF level = -18dBm	3.6	4.8	5.8	V
	RSSI range	R_g = 100kΩ Pin 16		80		dB
	RSSI accuracy	R_g = 100kΩ Pin 16		±2		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ
RF/IF section (Int LO)						
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA615 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for x-tal configurations. Butler oscillators are recommended for x-tal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

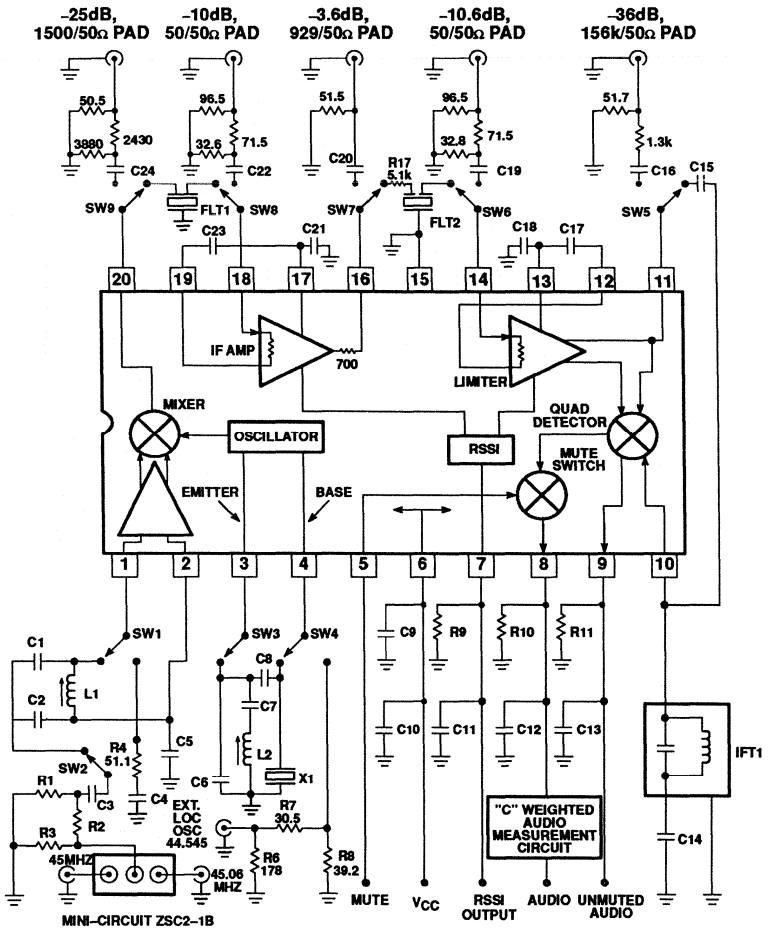
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

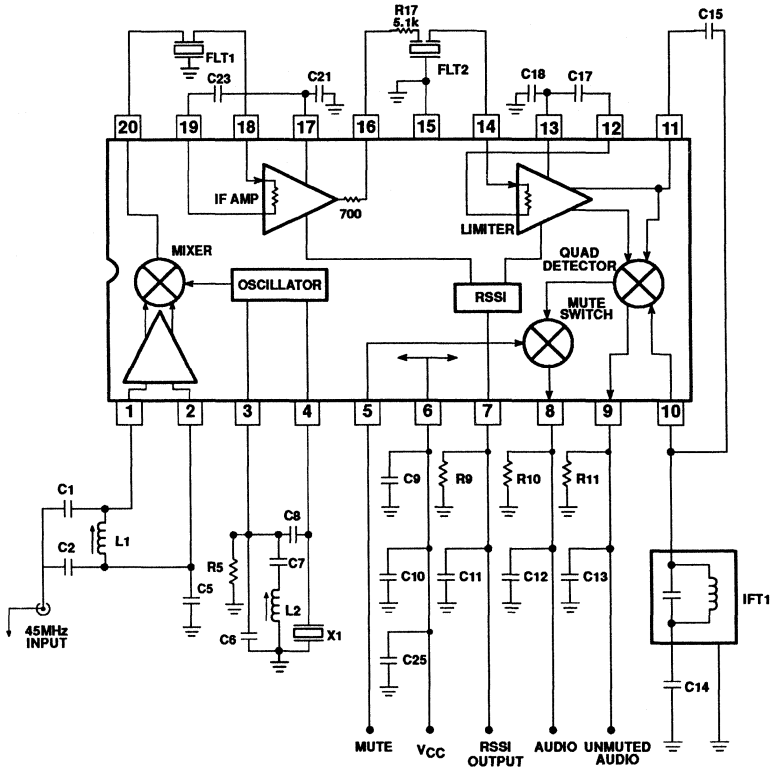
NOTE: dB(v) = 20log V_{OUT}/V_{IN}



Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
L1	147-160nH Coilcraft UNI-10/142-04J08S
L2	3.3μH nominal Toko 292CNS-T1046Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

Figure 1. NE/SA615 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	3.3μH nominal Toko 292CNS–T1046Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

Figure 2. NE/SA615 45MHz Application Circuit

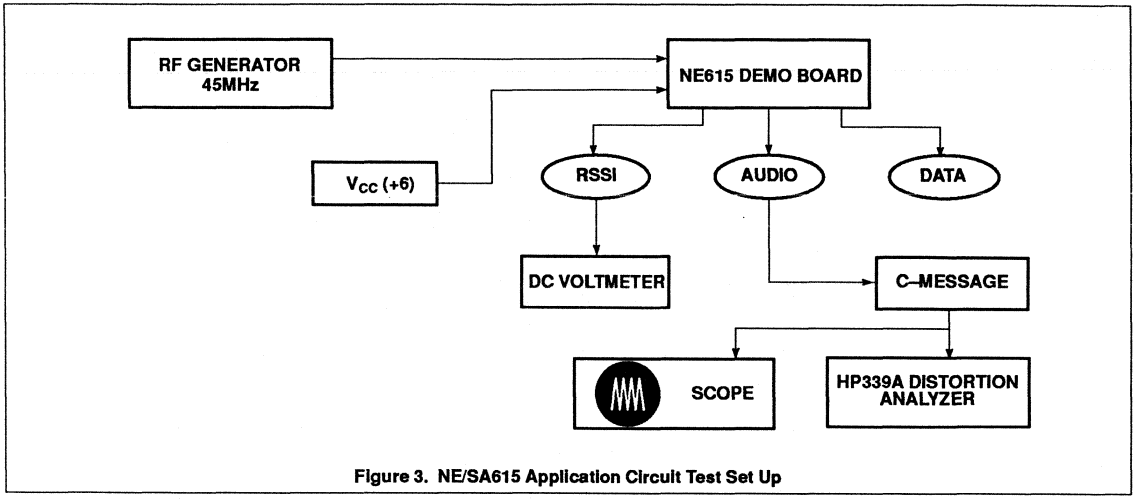


Figure 3. NE/SA615 Application Circuit Test Set Up

NOTES:
1. C–message: The C–message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10–15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2–3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

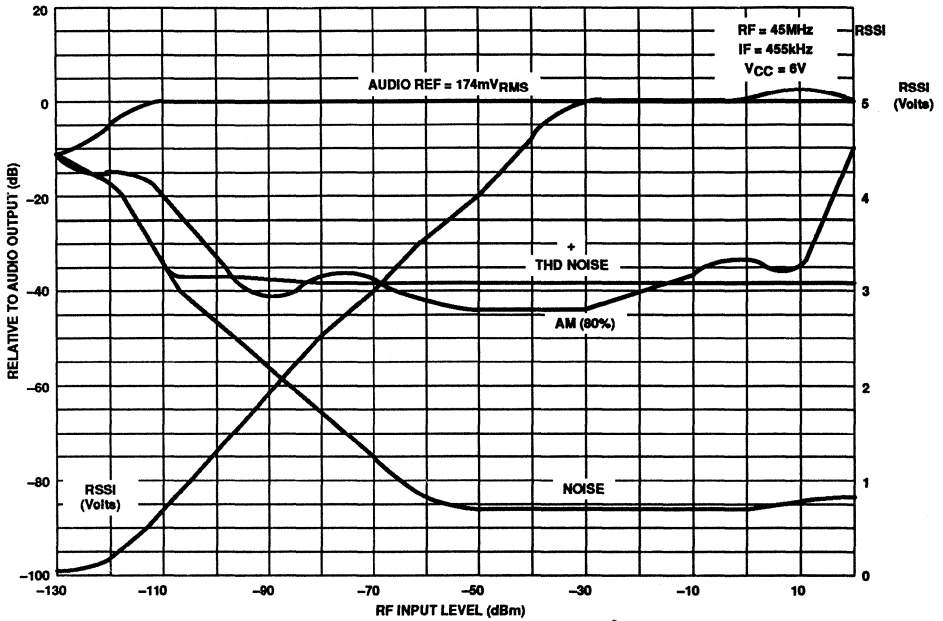


Figure 4. NE615 Application Board at 25°C

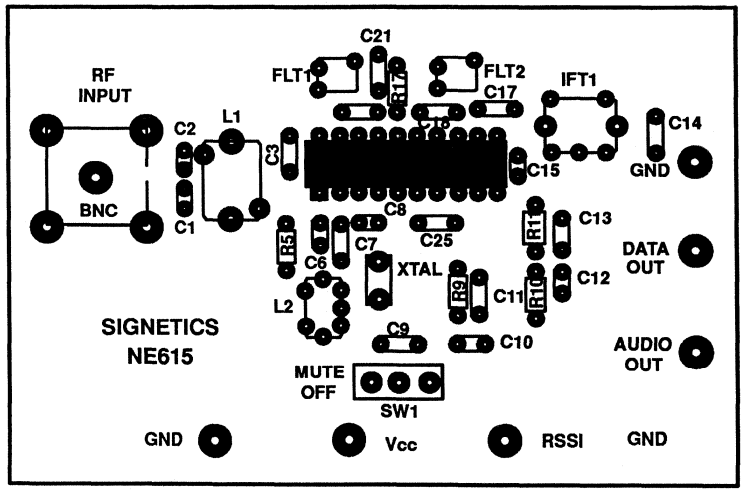
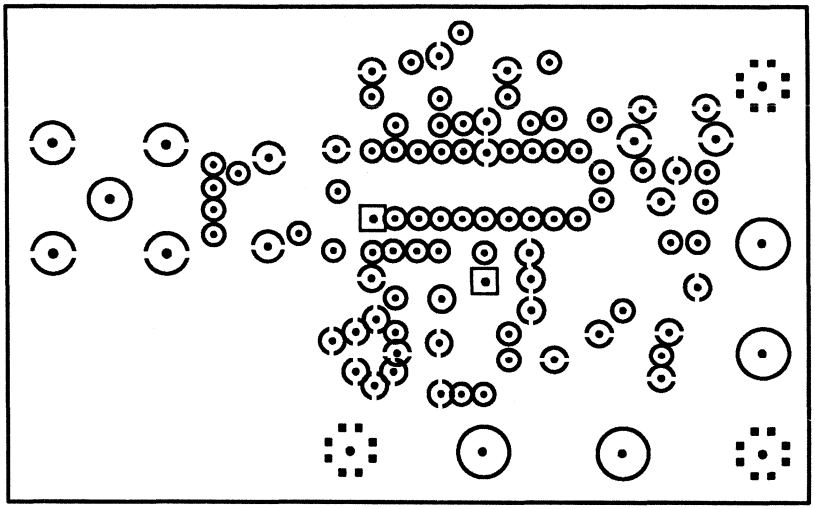
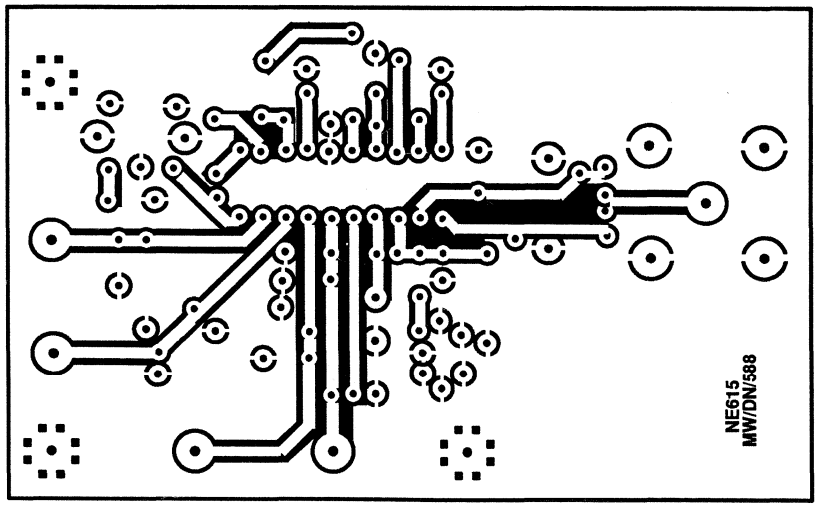


Figure 5. Component Placement for NE615 Application Circuit



TOP VIEW



BOTTOM VIEW

Figure 6. Layout for NE/SA615 Application Board

NE/SA5204
Wide-band High-Frequency Amplifier

Product Specification

DESCRIPTION

The NE/SA5204 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ± 0.5dB from DC to 200MHz. The −3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204 operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204 is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

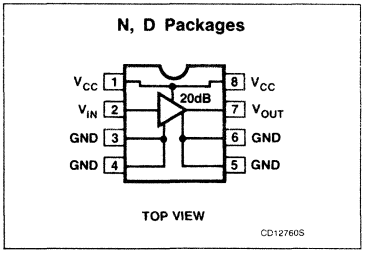
No external components are needed other than AC-coupling capacitors because the NE/SA5204 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204s in series as required, without any degradation in amplifier stability.

FEATURES

- **Bandwidth (min.)**
  200 MHz, ± 0.5dB
  350 MHz, − 3dB
- **20dB insertion gain**
- **4.8dB (6dB) noise figure**
  Z_O = 75Ω (Z_O = 50Ω)
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface-mount package available**
- **Cascadable**

PIN CONFIGURATION



APPLICATIONS

- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broadband LANs**
- **Networks**
- **Modems**
- **Mobile radio**
- **Security systems**
- **Telecommunications**

ORDERING INFORMATION

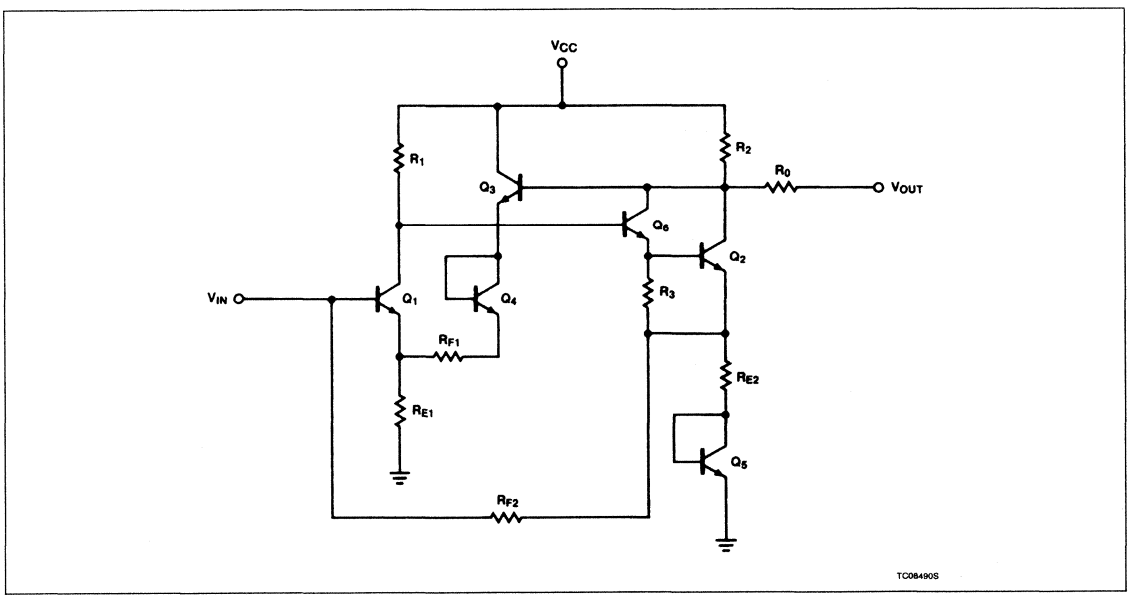
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5204N
	−40 to +85°C	SA5204N
8-Pin Plastic SO package	0 to +70°C	NE5204D
	−40 to +85°C	SA5204D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range NE grade SA grade	 0 to +70 −40 to +85	 °C °C
P_{DMAX}	Maximum power dissipation[1, 2] T_A = 25°C (still-air) N package D package	 1160 780	 mW mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C.
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	24	31	mA
S21	Insertion gain	f = 100MHz, over temperature	16	19	22	dB
S11	Input return loss	f = 100MHz		25		dB
		DC –550MHz		12		dB
S22	Output return loss	f = 100MHz		27		dB
		DC –550MHz		12		dB
S12	Isolation	f = 100MHz		–25		dB
		DC –550MHz		–18		dB
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	–3dB	350	550		MHz
	Noise figure (75Ω)	f = 100MHz		4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0		dB
	Saturated output power	f = 100MHz		+7.0		dBm
	1dB gain compression	f = 100MHz		+4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+24		dBm
t_R	Rise time			5		ps
	Propagation delay			5		ps

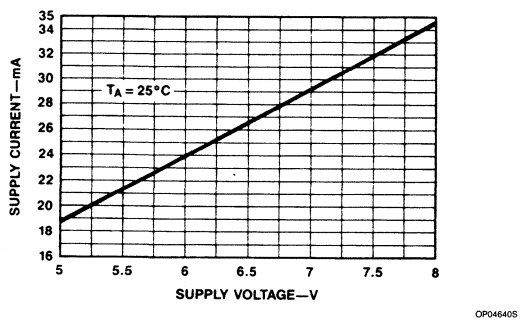


Figure 1. Supply Current vs Supply Voltage

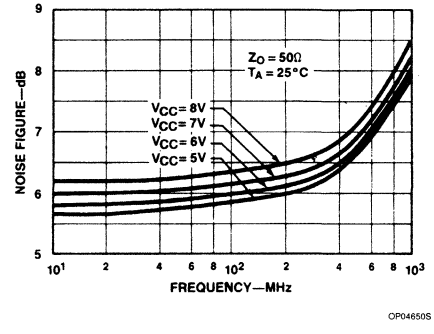


Figure 2. Noise Figure vs Frequency

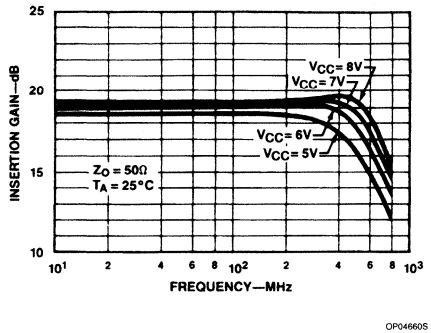


Figure 3. Insertion Gain vs Frequency (S_{21})

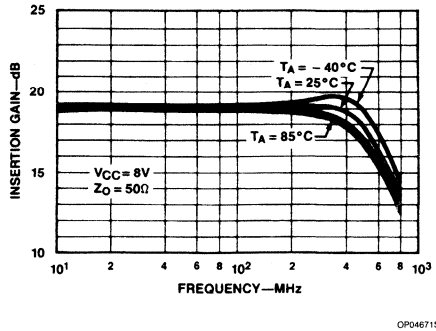


Figure 4. Insertion Gain vs Frequency (S_{21})

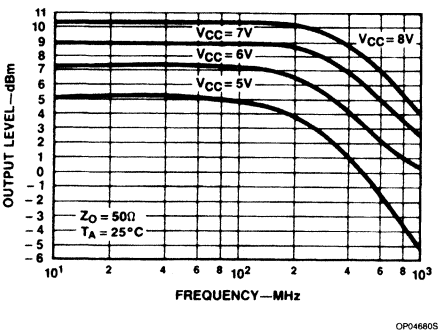


Figure 5. Saturated Output Power vs Frequency

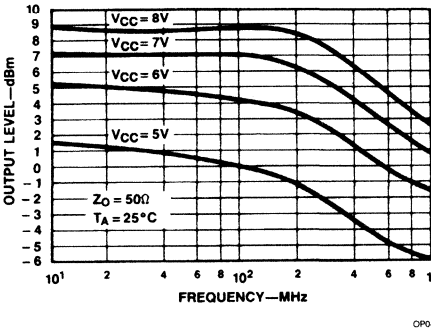


Figure 6. 1dB Gain Compression vs Frequency

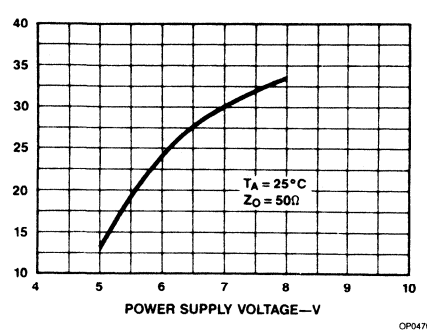


Figure 7. Second-Order Output Intercept vs Supply Voltage

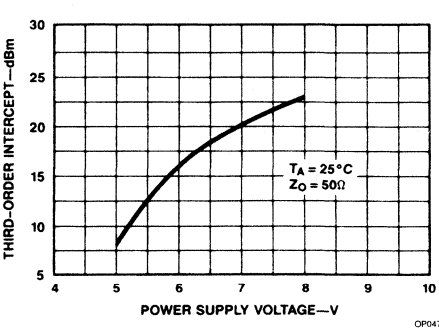


Figure 8. Third-Order Intercept vs Supply Voltage

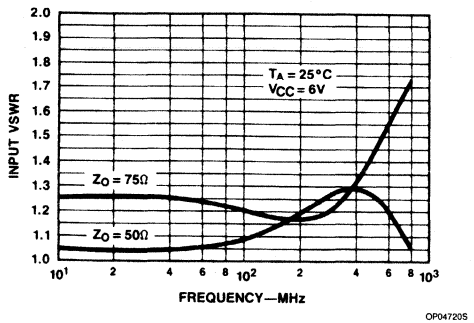


Figure 9. Input VSWR vs Frequency

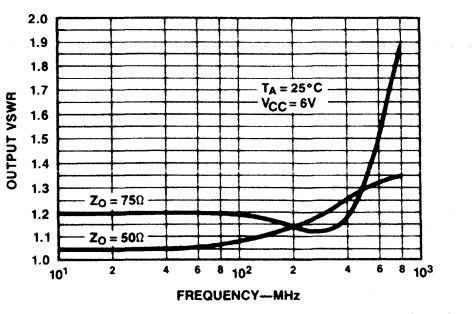


Figure 10. Output VSWR vs Frequency

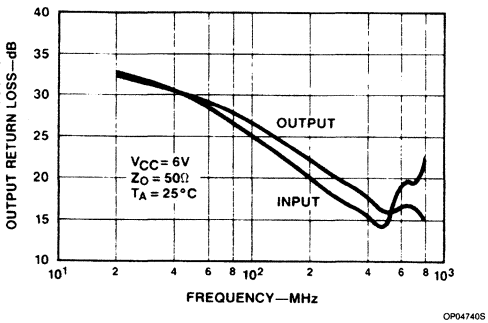


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

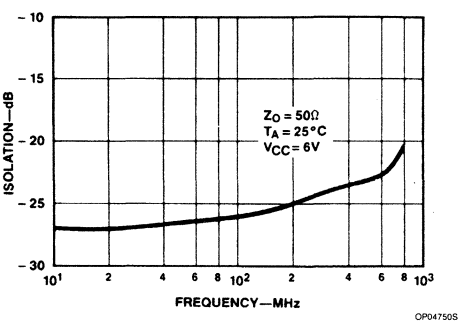


Figure 12. Isolation vs Frequency (S_{12})

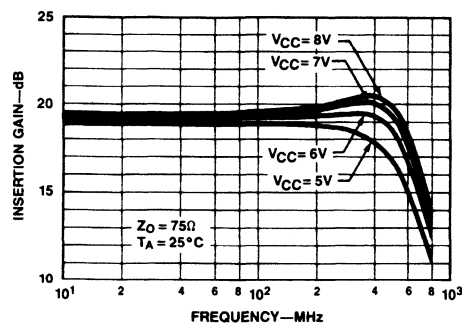


Figure 13. Insertion Gain vs Frequency (S_{21})

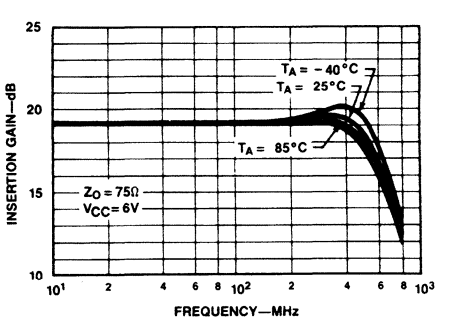


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10\text{Log}\left\{1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_0}\right\} \text{dB} \quad (2)$$

where I_{C1} = 5.5mA, R_{E1} = 12Ω, r_b = 130Ω, KT/q = 26mV at 25°C and R_0 = 50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})\,R_{E1} \quad (3)$$

where R_{E1} = 12Ω, V_{BE} = 0.8V, I_{C1} = 5mA and I_{C3} = 7mA (currents rated at V_{CC} = 6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of R_{F1} = 140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \quad (4)$$

where V_{CC} = 6V, R_2 = 225Ω, I_{C2} = 7mA and I_{C6} = 5mA.

From here, it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

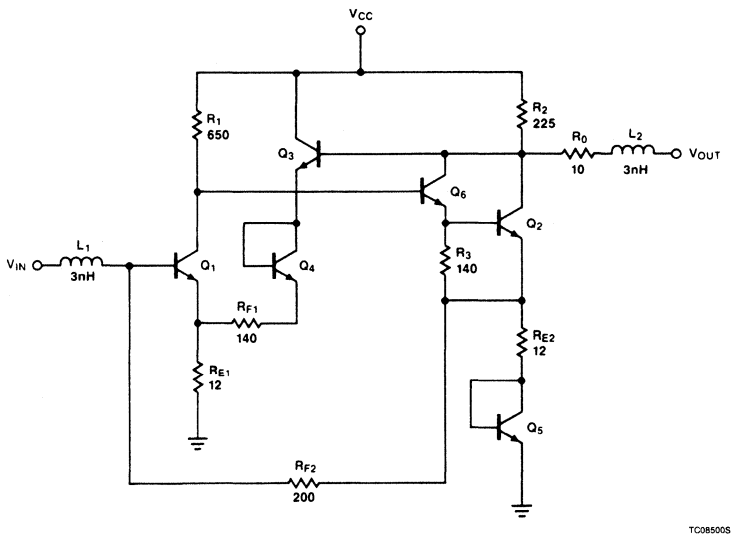


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at $V_{CC} = 6V$, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

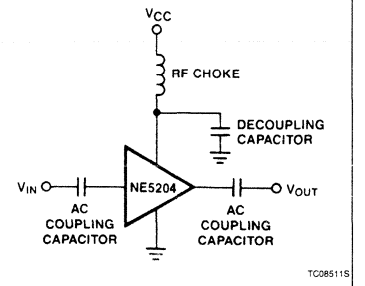
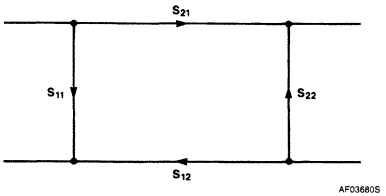


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

SCATTERING PARAMETERS

The primary specifications for the NE5204 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

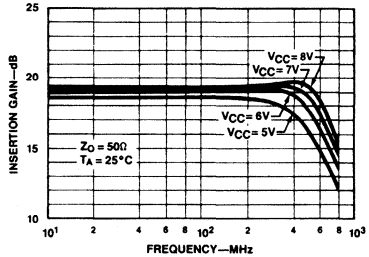
$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

AF03690S

b.

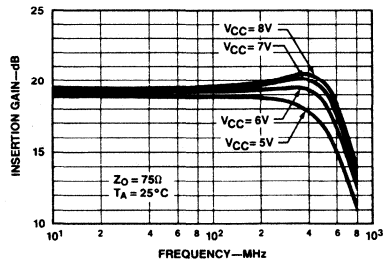
Figure 17

50Ω System

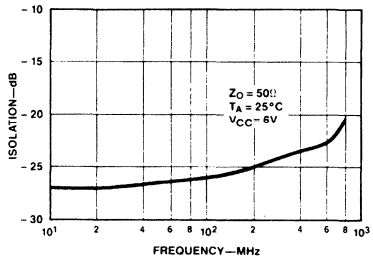


a. Insertion Gain vs Frequency (S_{21})

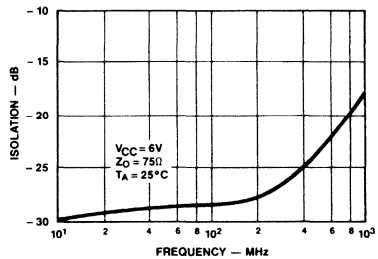
75Ω System



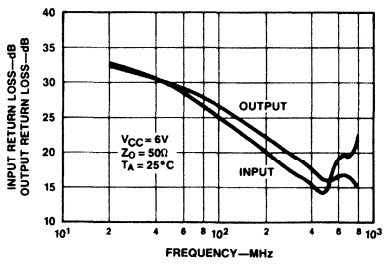
b. Insertion Gain vs Frequency (S_{21})



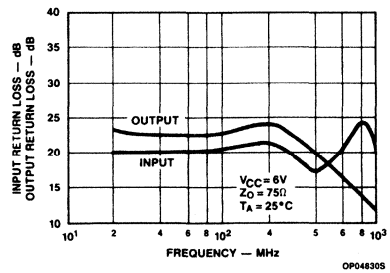
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency



f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18

Actual S-parameter measurements, using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B), are shown in Figure 18.

Values for Figure 20 are measured and specified in the data sheet to ease adaptation and comparison of the NE5204 to other high-frequency amplifiers. The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE5204

$$P_{IN} = \frac{V_{IN}^2}{Z_D} \quad \boxed{\text{NE5204}\ Z_D} \quad P_{OUT} = \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I = Insertion Power Gain
V_I = Insertion Voltage Gain

Measured value for the NE5204 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10\text{Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20\text{Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing-wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = S_{11}dB
$S_{11}\text{dB} = 20\text{Log } |S_{11}|$

OUTPUT RETURN LOSS = S_{22}dB
$S_{22}\text{dB} = 20\text{Log } |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leqslant 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leqslant 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to non-linearities in the amplifier, an indication of the point of transition between small-signal operation and the large-signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

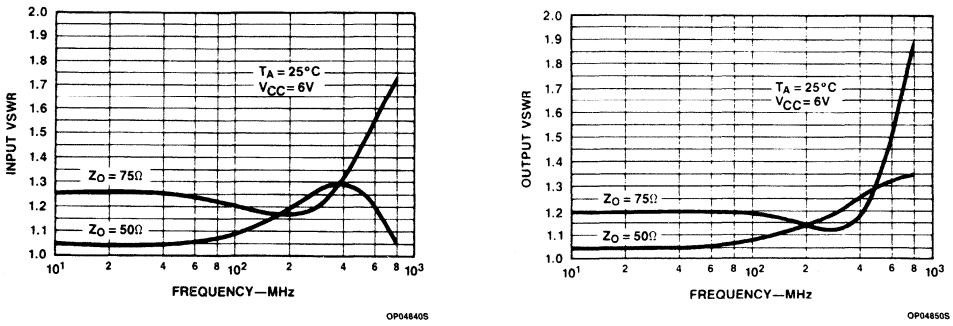
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second-order IMR is equal to the difference between the second-order intercept and the fundamental output level. The third-order IMR is equal to twice the difference between the third-order intercept and the fundamental output level. These are expressed as:

$$IP_2 = P_{OUT} + IMR_2$$

$$IP_3 = P_{OUT} + IMR_3/2$$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second- and third-order output intercepts in dBm, and IMR_2 and IMR_3 are the second- and third- order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small-signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point, the intermodulation products no longer follow the straight-line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be care-



a. Input VSWR vs Frequency

b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ful, however, not to select levels which are too low, because the test equipment may not be able to recover the signal from the noise. For the NE5204, an output level of −10.5dBm was chosen with fundamental frequencies of 100.000 and 100.01MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers*; by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985, published by John Wiley & Sons, Inc.

S-Parameter Techniques for Faster, More Accurate Network Design, HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

S-Parameter Design, HP App Note 154, 1972.

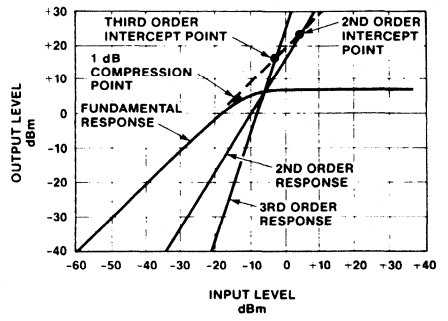


Figure 20

NE/SA/SE5205
Wide-band High-Frequency Amplifier

Product Specification

DESCRIPTION

The NE/SA/SE5205 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the −3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205 operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205 solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the −3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects. A TO-46 metal can is also available that has a case connection for RF grounding which increases the −3dB frequency to 600MHz. The Cerdip package is hermetically sealed, and can operate over the full −55°C to +125°C range.

No external components are needed other than AC coupling capacitors because the NE/SA/SE5205 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205s in series as required, without any degradation in amplifier stability.

FEATURES

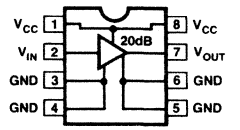
- **600MHz bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)**
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface mount package available**
- **MIL-STD processing available**

APPLICATIONS

- **75Ω cable TV decoder boxes**
- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broad-band LANs**
- **Fiber-optics**
- **Modems**
- **Mobile radio**
- **Security systems**
- **Telecommunications**

PIN CONFIGURATIONS

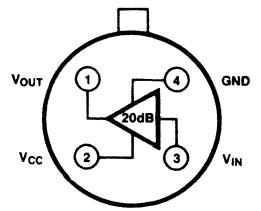
N, FE, D Packages



TOP VIEW

CD12760S

EC Package



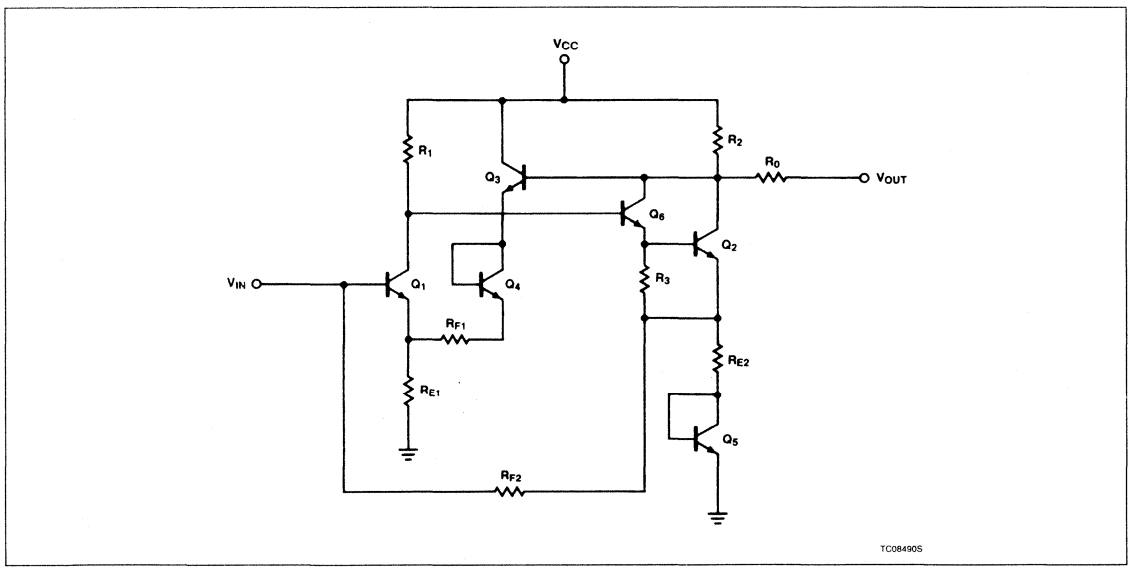
CD09850S

NOTE:
Tab denotes Pin 1.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5205D
4-Pin Metal can	0 to +70°C	NE5205EC
8-Pin Cerdip	0 to +70°C	NE5205FE
8-Pin Plastic DIP	0 to +70°C	NE5205N
8-Pin Plastic SO	−40°C to +85°C	SA5205D
8-Pin Plastic DIP	−40°C to +85°C	SA5205N
8-Pin Cerdip	−40°C to +85°C	SA5205FE
8-Pin Cerdip	−55°C to +125°C	SE5205FE
8-Pin Plastic DIP	−55°C to +125°C	SE5205N

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	−40 to +85	°C
	SE grade	−55 to +125	°C
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[1, 2]		
	FE package	780	mW
	N package	1160	mW
	D package	780	mW
	EC package	1250	mW

NOTES:
1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
   EC package at 10.0mW/°C
2. See "Power Dissipation Considerations" section.

DC ELECTRICAL CHARACTERISTICS

at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Operating supply voltage range	Over temperature	5 5		6.5 6.5	5 5		8 8	V V
I_{CC}	Supply current	Over temperature	20 19	24	30 31	20 19	24	30 31	mA mA
S21	Insertion gain	f = 100MHz Over temperature	17 16.5	19	21 21.5	17 16.5	19	21 21.5	dB
S11	Input return loss	f = 100MHz D, N, FE		25			25		dB
		DC − f_{MAX} D, N, FE	12			12			dB
S11	Input return loss	f = 100MHz EC package					24		dB
		DC − f_{MAX} EC				10			dB
S22	Output return loss	f = 100MHz D, N, FE		27			27		dB
		DC − f_{MAX}	12			12			dB
S22	Output return loss	f = 100MHz EC package					26		dB
		DC − F_{MAX}				10			dB
S12	Isolation	f = 100MHz		−25			−25		dB
		DC − f_{MAX}	−18			−18			dB
t_R	Rise time			5			5		ps
	Propagation delay			5			5		ps

DC ELECTRICAL CHARACTERISTICS at V_{CC} = 6V, $Z_S = Z_L = Z_O$ = 50Ω and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth	±0.5dB D, N					450		MHz
f_{MAX}	Bandwidth	±0.5dB EC					500		MHz
f_{MAX}	Bandwidth	±0.5dB FE		300			300		MHz
f_{MAX}	Bandwidth	-3dB D, N				550			MHz
f_{MAX}	Bandwidth	-3dB EC				600			MHz
f_{MAX}	Bandwidth	-3dB FE	400			400			MHz
	Noise figure (75Ω)	f = 100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0			6.0		dB
	Saturated output power	f = 100MHz		+7.0			+7.0		dBm
	1dB gain compression	f = 100MHz		+4.0			+4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+17			+17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+24			+24		dBm

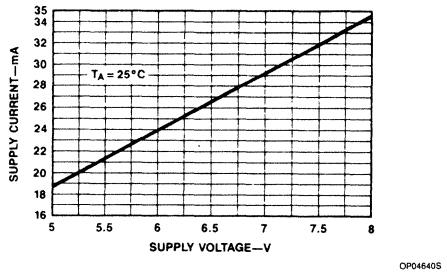


Figure 1. Supply Current vs Supply Voltage

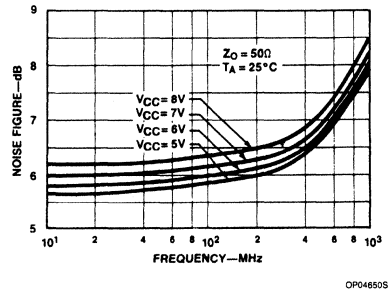


Figure 2. Noise Figure vs Frequency

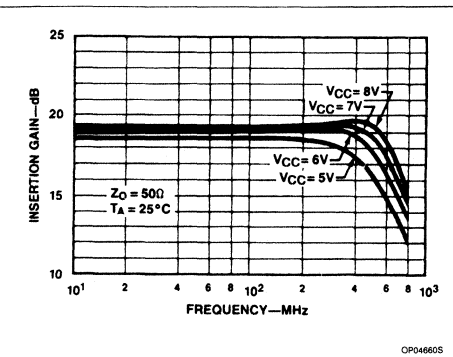


Figure 3. Insertion Gain vs Frequency (S_{21})

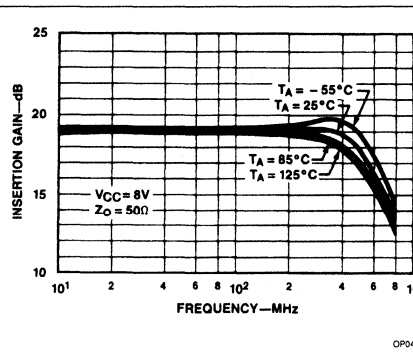


Figure 4. Insertion Gain vs Frequency (S_{21})

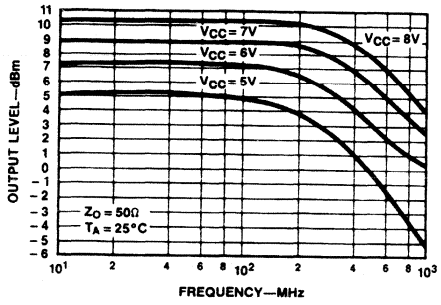


Figure 5. Saturated Output Power vs Frequency

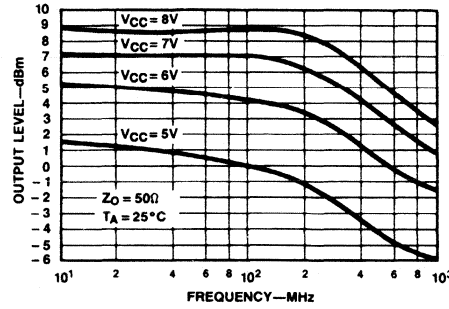


Figure 6. 1dB Gain Compression vs Frequency

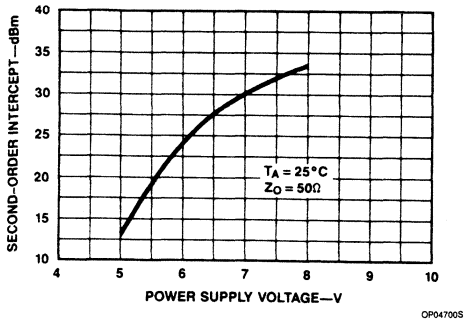


Figure 7. Second-Order Output Intercept vs Supply Voltage

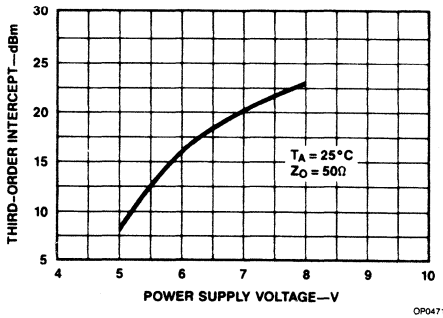


Figure 8. Third-Order Intercept vs Supply Voltage

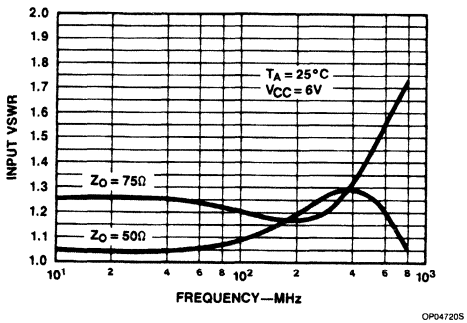


Figure 9. Input VSWR vs Frequency

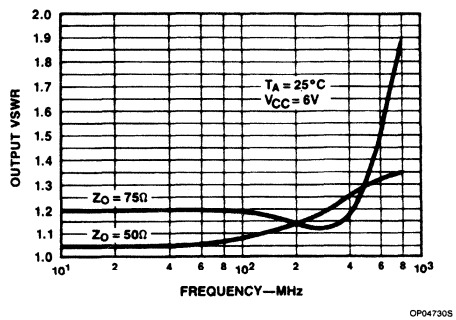


Figure 10. Output VSWR vs Frequency

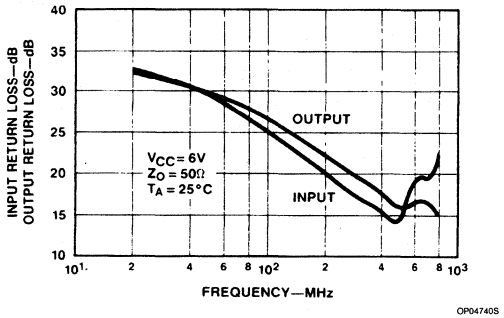


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

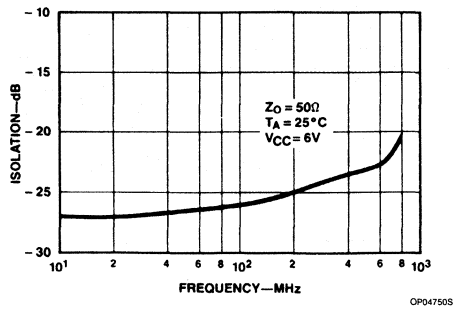


Figure 12. Isolation vs Frequency (S_{12})

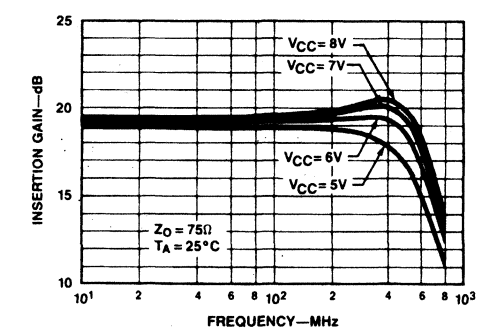


Figure 13. Insertion Gain vs Frequency (S_{21})

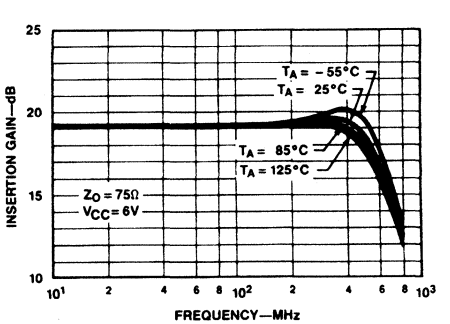


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10 \text{ Log} \left\{ 1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_0} \right\} \text{ dB} \quad (2)$$

where I_{C1} = 5.5mA, R_{E1} = 12Ω, r_b = 130Ω, KT/q = 26mV at 25°C and R_0 = 50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})\ R_{E1}$$

where R_{E1} = 12Ω, V_{BE} = 0.8V, I_{C1} = 5mA and I_{C3} = 7mA (currents rated at V_{CC} = 6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of R_{F1} = 140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \quad (4)$$

where V_{CC} = 6V, R_2 = 225Ω, I_{C2} = 7mA and I_{C6} = 5mA.

From here it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA Max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D and EC package body against the PC board plane.

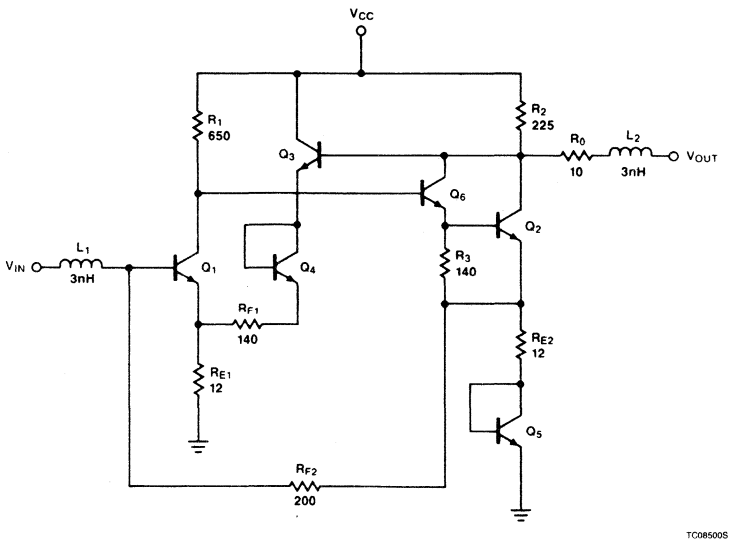


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). In addition, if the EC package is used, the case should be soldered to the ground plane. The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at V_{CC} = 6V, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

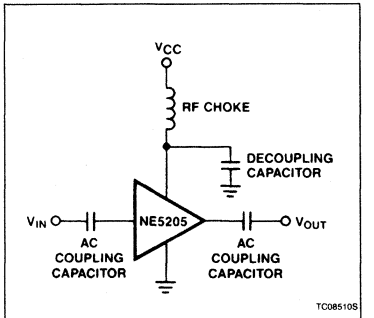


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

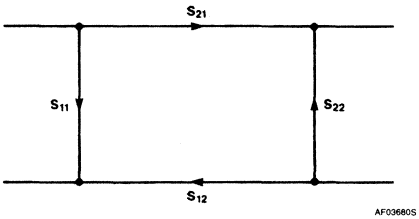


Figure 17a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

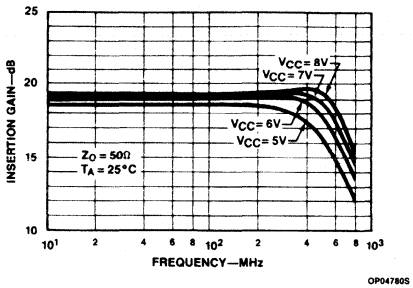
AF03690S

Figure 17b

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

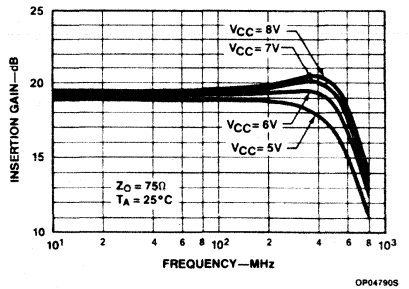
Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205 to other high-frequency amplifiers.

50Ω System

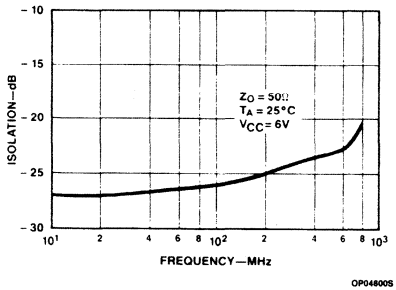


a. Insertion Gain vs Frequency (S_{21})

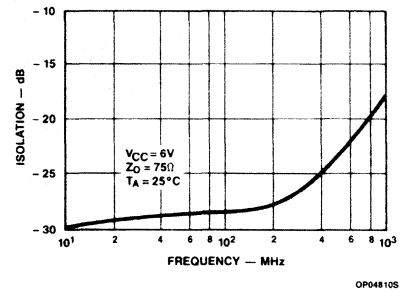
75Ω System



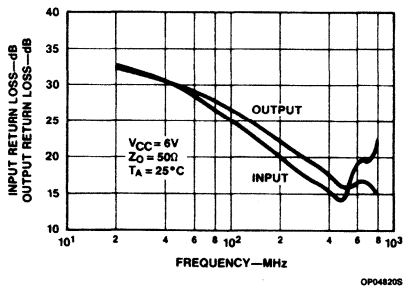
b. Insertion Gain vs Frequency (S_{21})



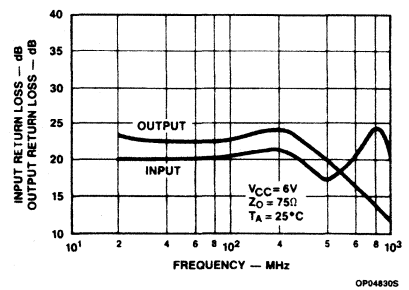
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency



f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE/SA/SE5205

$$P_{IN} = \frac{V_{IN}^2}{Z_D} \quad \boxed{\text{NE/SA/SE5205}\ Z_D} \quad P_{OUT} = \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I = Insertion Power Gain

V_I = Insertion Voltage Gain

Measured value for the NE/SA/SE5205 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20dB$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20dB$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20dB$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = $S_{11}dB$

$S_{11}dB = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS = $S_{22}dB$

$S_{22}dB = 20 \text{ Log } |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leqslant 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leqslant 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

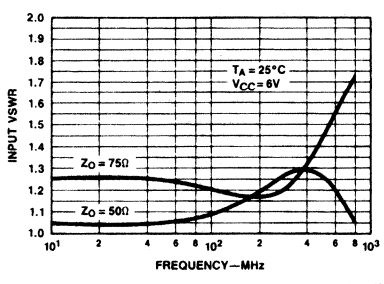
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

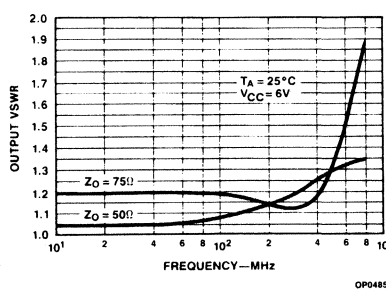
$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205 we have chosen an output level of −10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency



b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers* by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

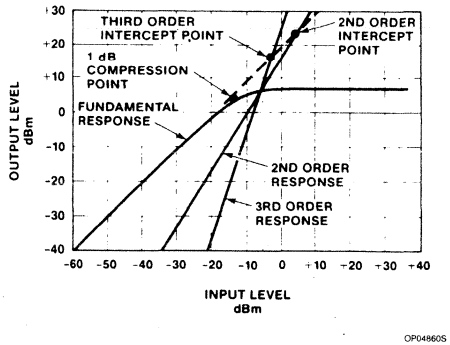


Figure 20

Document	853-1453
ECN No.	00223
Date of Issue	August 20, 1990
Status	Product Specification
RF Communications	

NE/SA5209

Wideband variable gain amplifier

DESCRIPTION

The NE5209 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5209 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5209 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

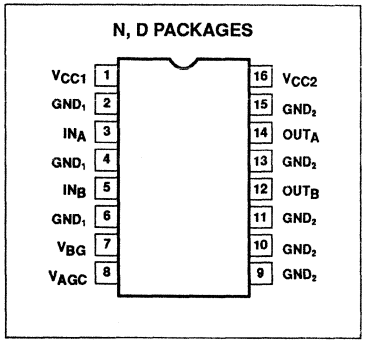
FEATURES

- Gain to 1.5GHz
- 850MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE5209D
16-Pin Plastic DIP	0 to +70°C	NE5209N
16-Pin Plastic SO	–40 to +85°C	SA5209D
16-Pin Plastic DIP	–40 to +85°C	SA5209N

Wideband variable gain amplifier — NE/SA5209

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	–0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	–65 to +150	°C

NOTES:
3.Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
16-Pin DIP: θ_{JA} = 85°C/W
16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 –40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 –40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	38	43	48	mA
		Over temperature[1]	30		55	mA
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	17	19	21	dB
		Over temperature[1]	16		22	dB
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	23	25	27	dB
		Over temperature[1]	22		28	dB
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.9	1.2	1.5	kΩ
		Over temperature[1]	0.8		1.7	kΩ
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	40	60	75	Ω
		Over temperature[1]	35		90	Ω
V_{OS}	Output offset voltage (output referred)			±20	±100	mV
		Over temperature[1]			±250	mV
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
		Over temperature[1]	1.4		2.6	V
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
		Over temperature[1]	1.7		3.1	V
PSRR	Output offset supply rejection ratio		20	45		dB
	(output referred)	Over temperature[1]	15			dB
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
		Over temperature[1]	1.1		1.55	V

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC1} = V_{CC2} = +5.0V$, $V_{AGC} = 1.0V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
R_{BG}	Bandgap loading	Over temperature[1]	2	10		kΩ
V_{AGC}	AGC DC control voltage range	Over temperature[1]		0-1.3		V
I_{BAGC}	AGC pin DC bias current	$0V<V_{AGC}<1.3V$		–0.7	–6	µA
		Over temperature[1]			–10	µA

NOTES:
1."Over Temperature Range" testing is as follows:
NE is 0 to +70°C
SA is –40 to +85°C
At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC1} = V_{CC2} = +5.0V$, $V_{AGC} = 1.0V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	–3dB bandwidth		600	850		MHz
		Over temperature[1]	500			MHz
GF	Gain flatness	DC – 500MHz		±0.4		dB
		Over temperature[1]		±0.6		dB
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[2]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation[2]	$R_L = 50Ω$		400		mV_{P-P}
		$R_L = 1kΩ$		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	$R_S = 50Ω$, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		$nV/\sqrt{Hz}$
S12	Reverse isolation	f = 100MHz		–60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	$R_L = 50Ω$		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	–3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		–3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		–10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:
1."Over Temperature Range" testing is as follows:
NE is 0 to +70°C
SA is –40 to +85°C
At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.
2.With $R_L > 1kΩ$, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With $R_L = 50Ω$, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

Wideband variable gain amplifier NE/SA5209

NE5209 APPLICATIONS

The NE5209 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5209 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 – 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5209 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5209 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5209 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5209. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5209 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5209 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5209 is shown in Figure 2. Three NE5209s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5209s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5209s will give a dynamic range in excess of 60dB.

The NE5209 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

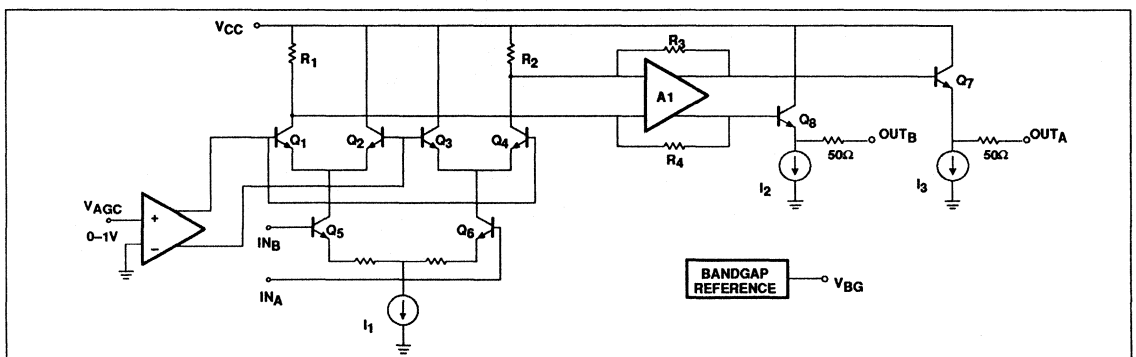


Figure 1. Equivalent Schematic of the VGA

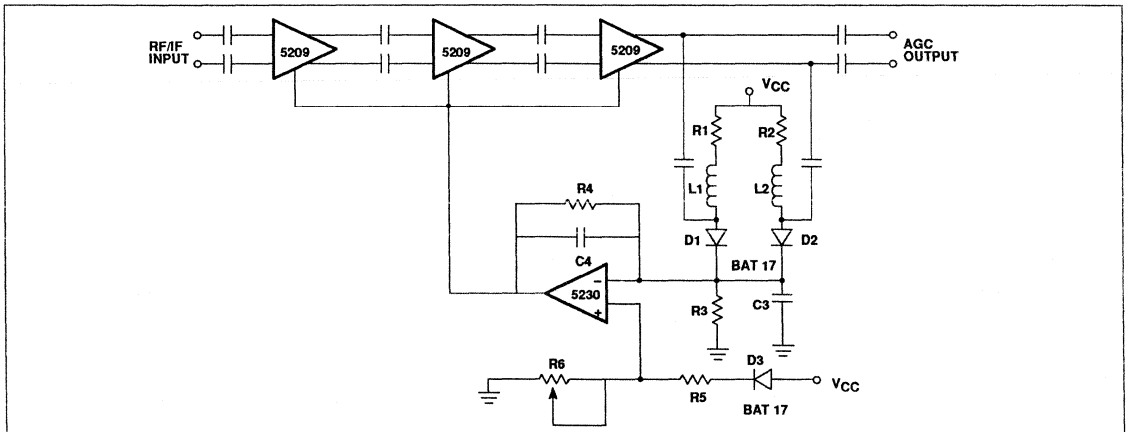


Figure 2. AGC Configuration Using Cascaded NE5209s

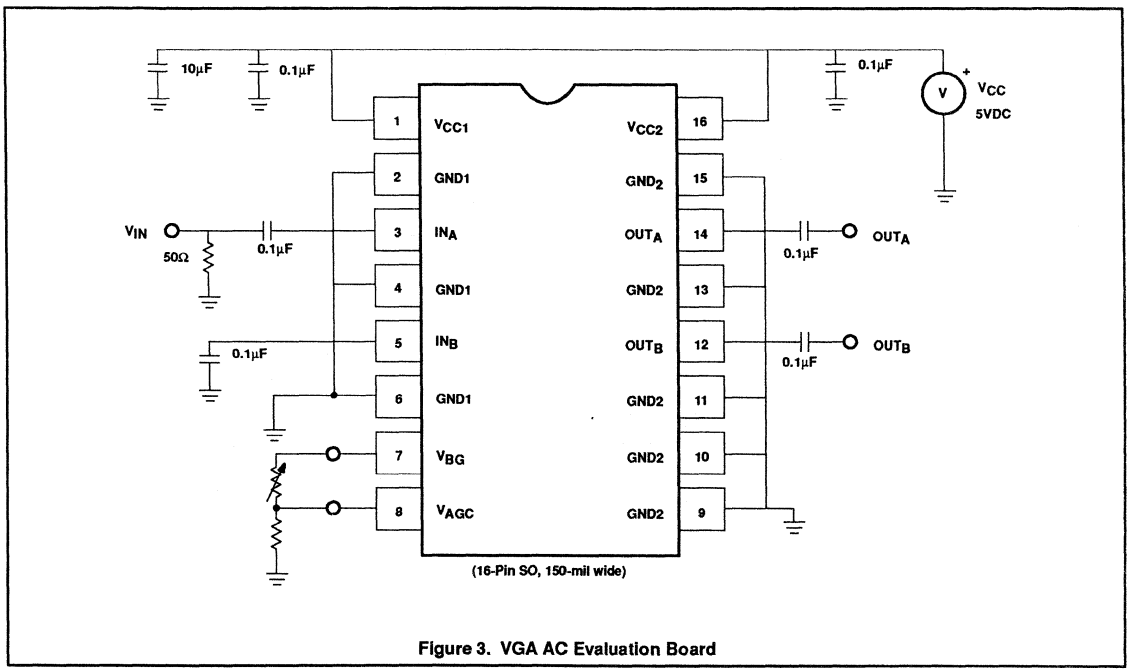
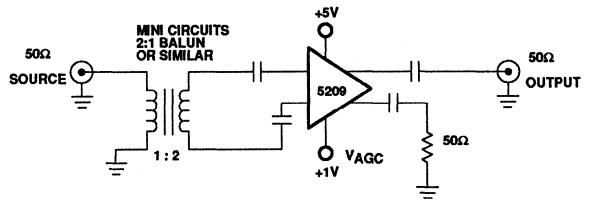
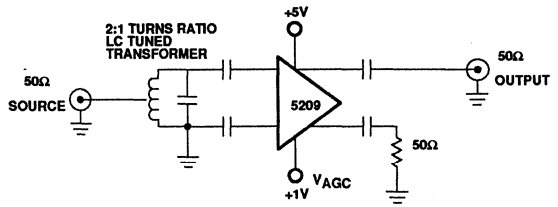


Figure 3. VGA AC Evaluation Board



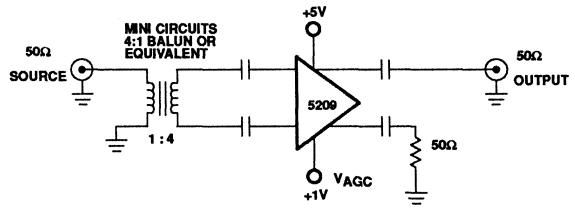
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



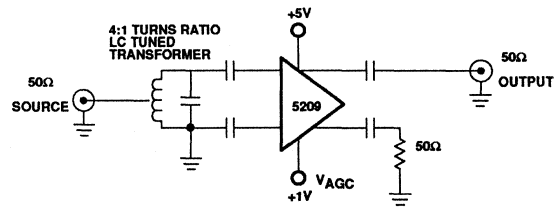
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization



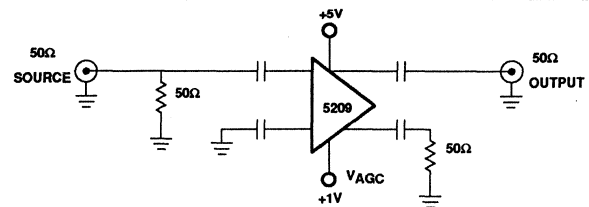
This circuit will exhibit about an 8dB noise figure with 24dB gain.

Figure 6. Broadband Gain Optimization



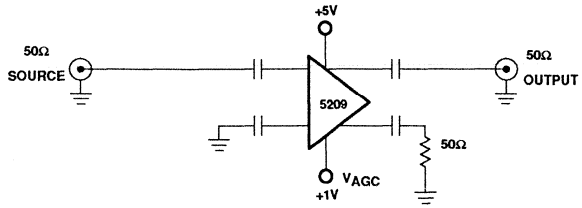
This circuit will exhibit approximately an 8dB noise figure and 25dB gain.

Figure 7. Narrowband Gain Optimization



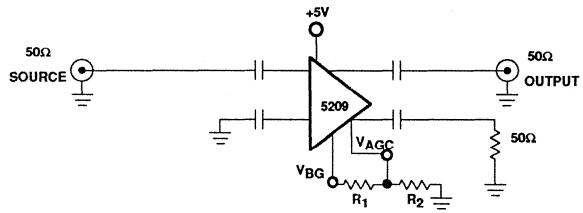
The noise figure of this configuration will be approximately 15dB.

Figure 8. Simple Amplifier Configuration



With the 50Ω source left unterminated, the noise figure is 9dB.

Figure 9 Unterminated Configuration

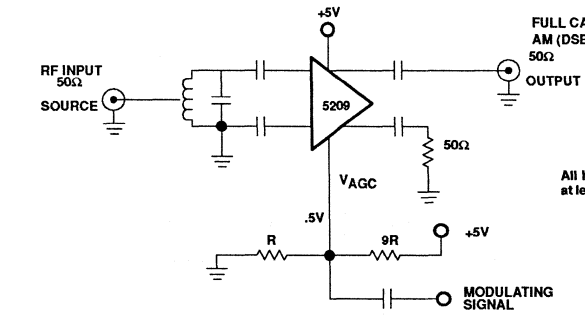


Gain = 19dB + 20log$_{10}$ V_{AGC}

where $V_{AGC} = \left[\frac{R_2}{R_1 + R_2} V_{BG}\right]$

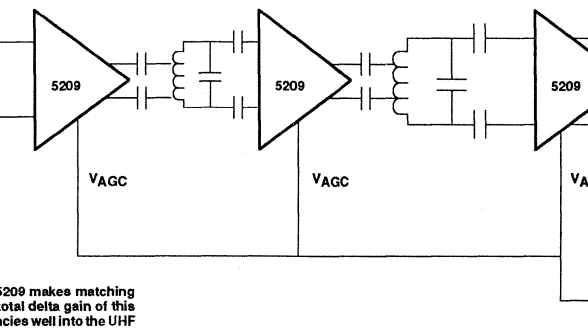
and is in units of Volts, for $V_{AGC} \leq 1V$

Figure 10. User-Programmable Fixed Gain Block



All harmonic distortion products will be at least –50dBc over the audio spectrum.

Figure 11. AM Modulator



The high input impedance to the NE5209 makes matching to crystal filters relatively easy. The total delta gain of this system will approach 80dB. IF frequencies well into the UHF region can be configured with this type of architecture.

Figure 12. Receiver AGC IF Chain

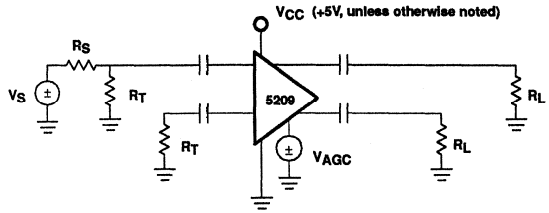


Figure 13. Test Set-up 1 (Used for all Graphs)

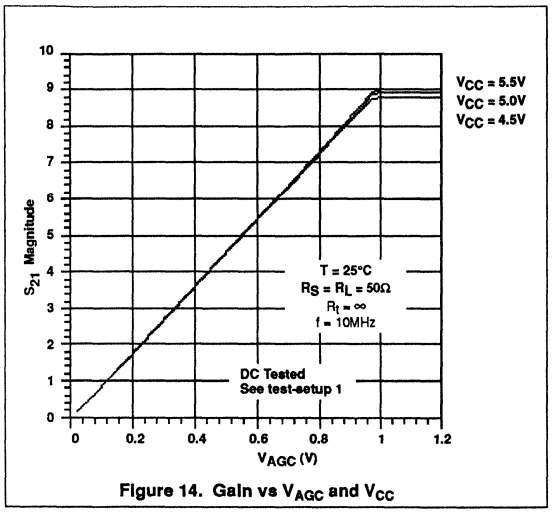


Figure 14. Gain vs V_{AGC} and V_{CC}

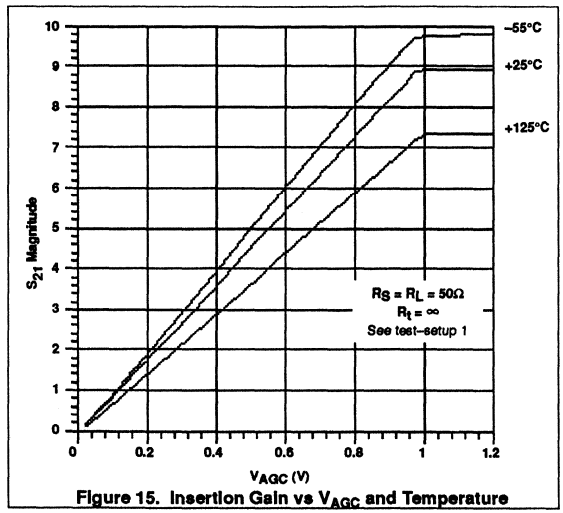


Figure 15. Insertion Gain vs V_{AGC} and Temperature

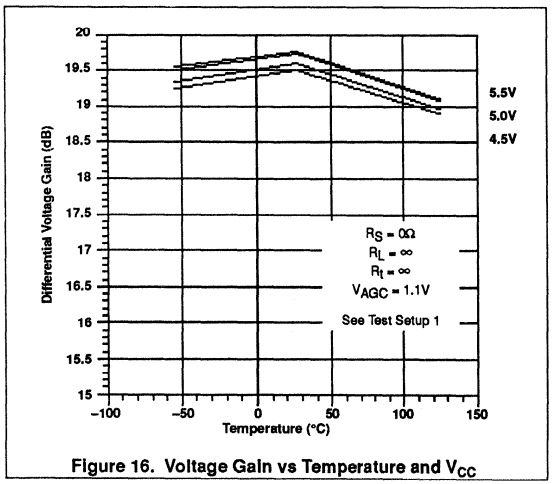


Figure 16. Voltage Gain vs Temperature and V_{CC}

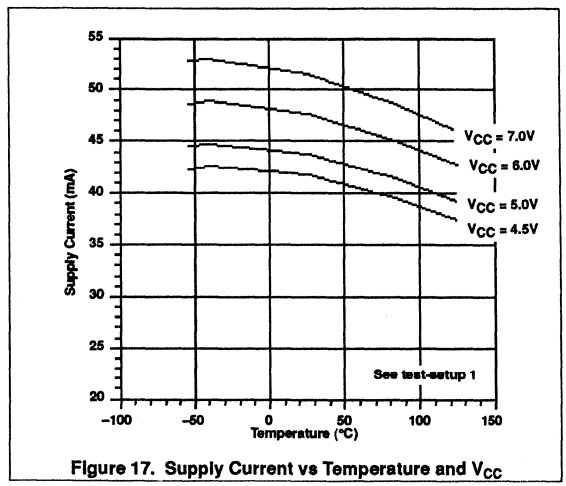


Figure 17. Supply Current vs Temperature and V_{CC}

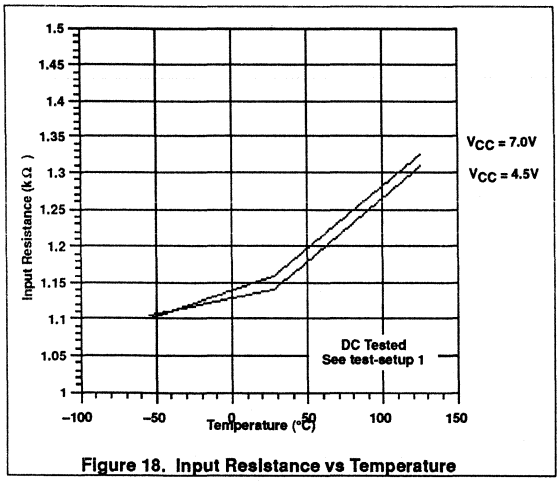


Figure 18. Input Resistance vs Temperature

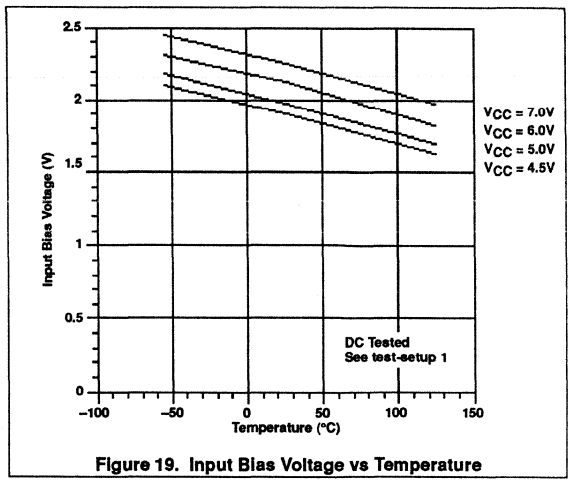


Figure 19. Input Bias Voltage vs Temperature

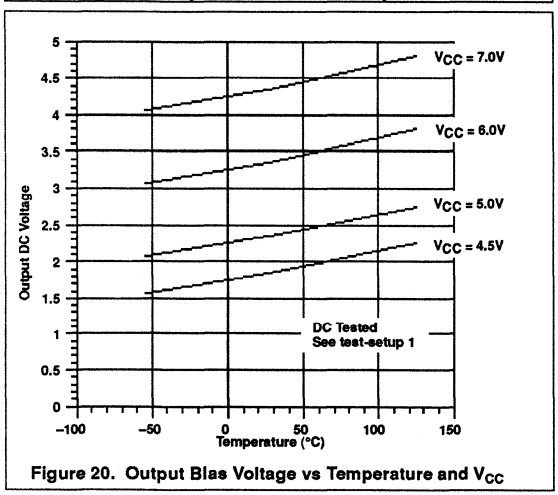


Figure 20. Output Bias Voltage vs Temperature and V_{CC}

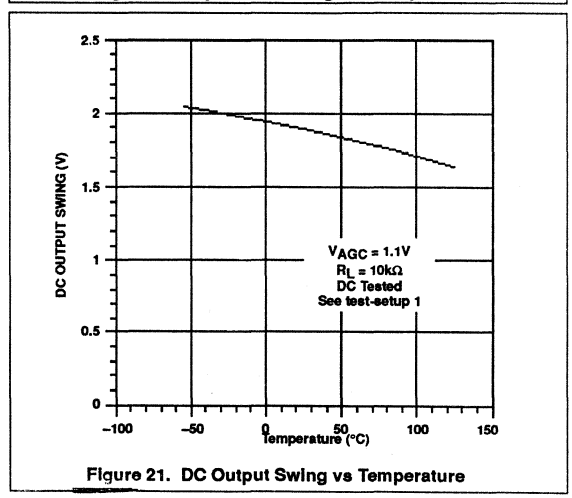


Figure 21. DC Output Swing vs Temperature

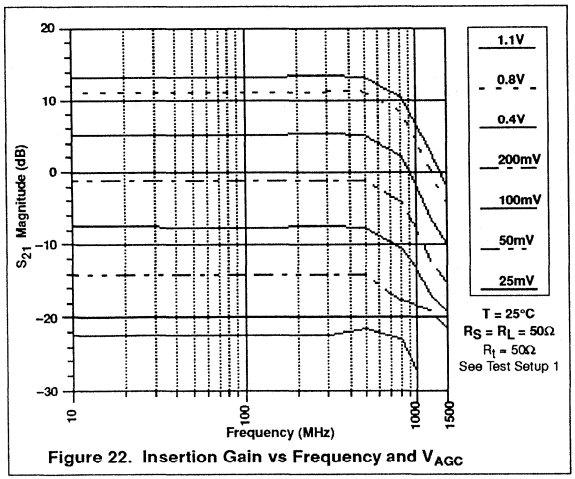


Figure 22. Insertion Gain vs Frequency and V_{AGC}

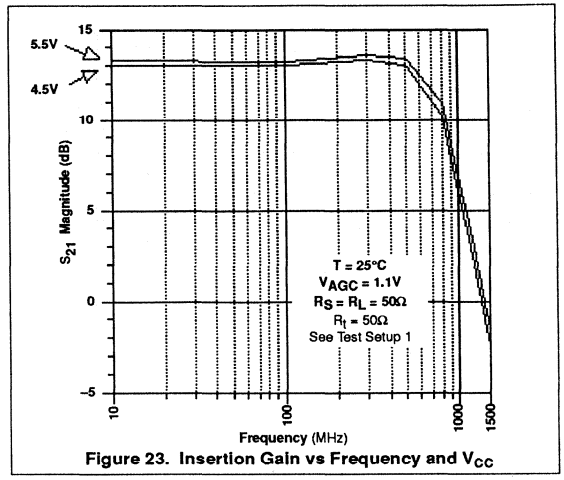


Figure 23. Insertion Gain vs Frequency and V_{CC}

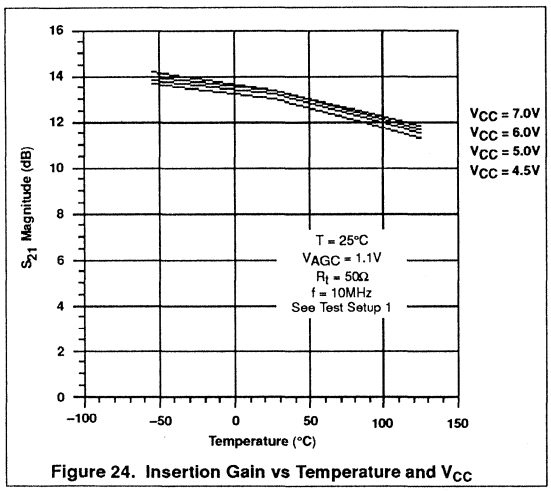


Figure 24. Insertion Gain vs Temperature and V_{CC}

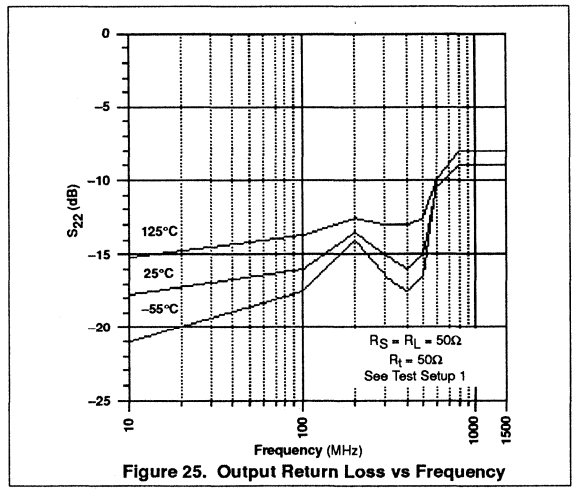


Figure 25. Output Return Loss vs Frequency

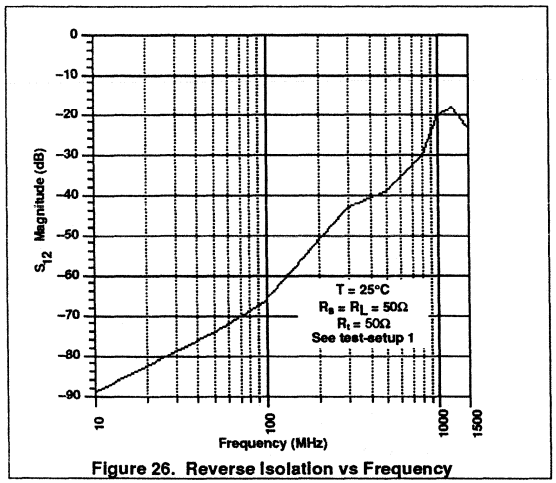


Figure 26. Reverse Isolation vs Frequency

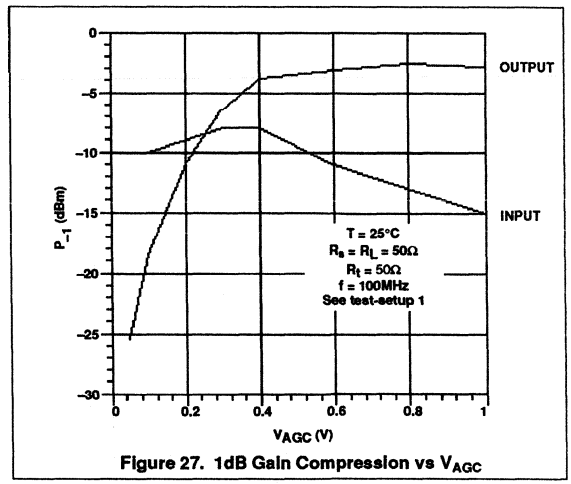


Figure 27. 1dB Gain Compression vs V_{AGC}

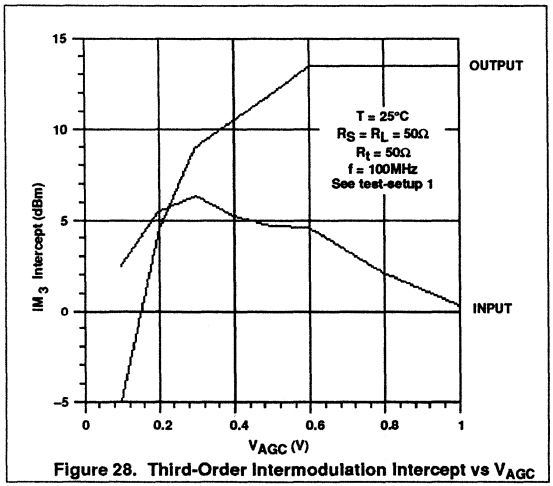


Figure 28. Third-Order Intermodulation Intercept vs V_{AGC}

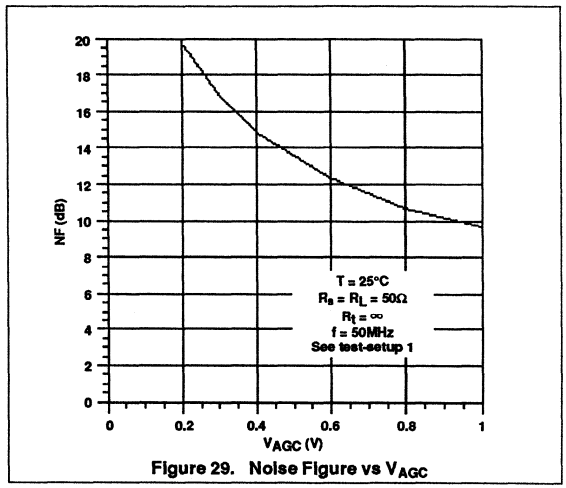


Figure 29. Noise Figure vs V_{AGC}

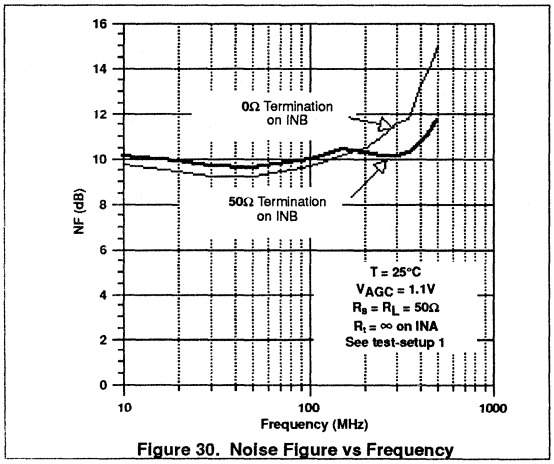


Figure 30. Noise Figure vs Frequency

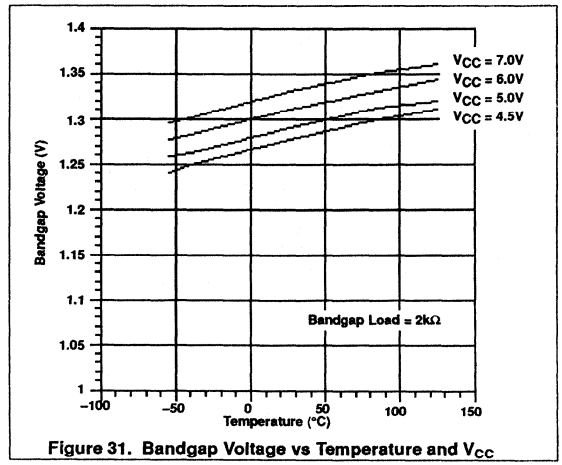


Figure 31. Bandgap Voltage vs Temperature and V_{CC}

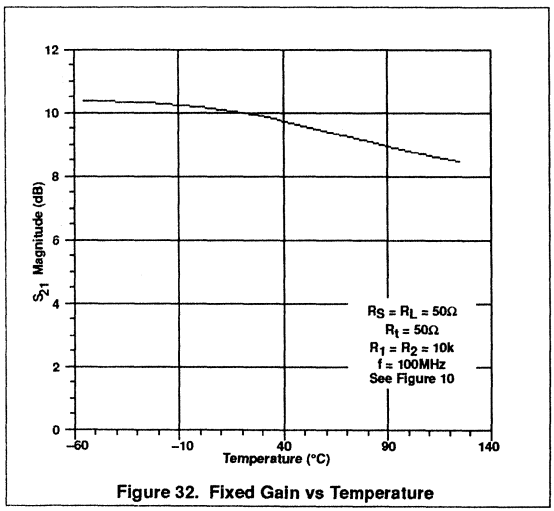
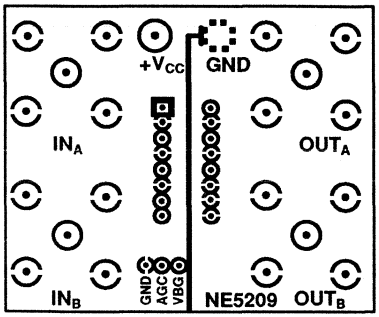
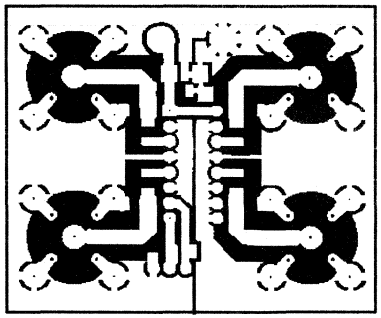


Figure 32. Fixed Gain vs Temperature

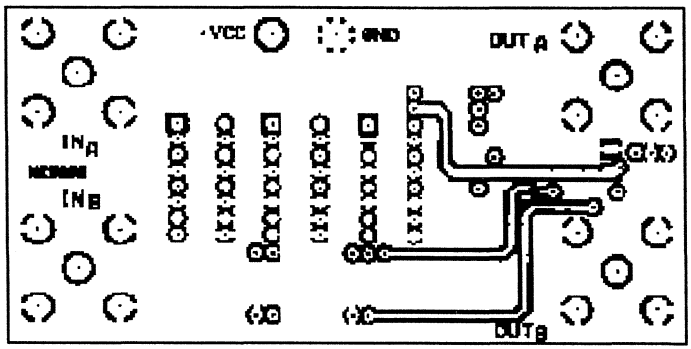


TOP VIEW - COMPONENT SIDE

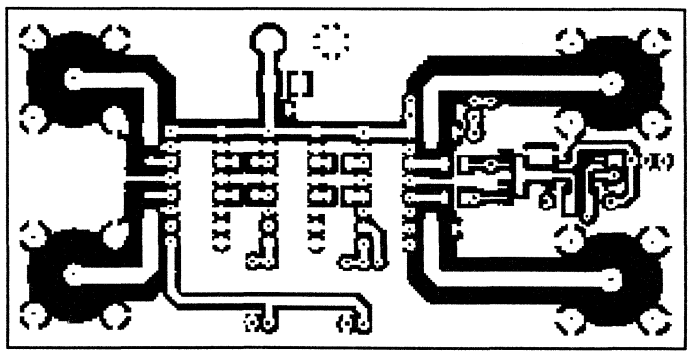


TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout



TOP VIEW - COMPONENT SIDE



TOP VIEW - SOLDER SIDE

AGC Configuration Using Cascaded NE5209s - Layout

NE/SA5230
Low Voltage Operational Amplifier

Product Specification

DESCRIPTION

The NE5230 is a very low voltage operational amplifier that can perform with a voltage supply as low as 1.8V or as high as 15V. In addition, split or single supplies can be used, and the output will swing to ground when applying the latter. There is a bias adjusting pin which controls the supply current required by the device and thereby controls its power consumption. If the part is operated at ±0.9V supply voltages, the current required is only 110μA when the current control pin is left open. Even with this low power consumption, the device obtains a typical unity gain bandwidth of 180kHz. When the bias adjusting pin is connected to the negative supply, the unity gain bandwidth is typically 600kHz while the supply current is increased to 600μA. In this mode, the part will supply full power output beyond the audio range.

The NE5230 also has a unique input stage that allows the common-mode input range to go above the positive and below the negative supply voltages by 250mV. This provides for the largest possible input voltages for low voltage applications. The part is also internally-compensated to reduce external component count.

The NE5230 has a low input bias current of typically ±40nA, and a large open-loop gain of 125dB. These two specifications are beneficial when using the device in transducer applications. The large open-loop gain gives very accurate signal processing because of the large "excess" loop gain in a closed-loop system.

The output stage is a class AB type that can swing to within 100mV of the supply voltages for the largest dynamic range that is needed in many applications. The NE5230 is ideal for portable audio equipment and remote transducers because of its low power consumption, unity gain bandwidth, and 30nV/$\sqrt{Hz}$ noise specification.

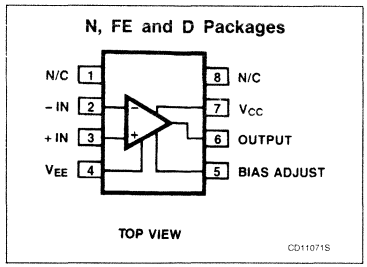
FEATURES

- **Works down to 1.8V supply voltages**
- **Adjustable supply current**
- **Low noise**
- **Common-mode includes both rails**
- **V_{OUT} within 100mV of both rails**

APPLICATIONS

- **Portable precision instruments**
- **Remote transducer amplifier**
- **Portable audio equipment**
- **Rail-to-rail comparators**
- **Half-wave rectification without diodes**
- **Remote temperature transducer with 4 to 20mA output transmission**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5230D
8-Pin Ceramic DIP	0 to +70°C	NE5230FE
8-Pin Plastic DIP	0 to +70°C	NE5230N
8-Pin Plastic SO	-40°C to +85°C	SA5230D
8-Pin Ceramic DIP	-40°C to +85°C	SA5230FE
8-Pin Plastic DIP	-40°C to +85°C	SA5230N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Single supply voltage	18	V
V_S	Dual supply voltage	±9	V
V_{IN}	Input voltage[1]	±9 (18)	V
	Differential input voltage[1]	$\pm V_S$	V
V_{CM}	Common-mode voltage (positive)	V_{CC} + 0.5	V
V_{CM}	Common-mode voltage (negative)	V_{EE} – 0.5	V
P_D	Power dissipation[2]	500	mW
T_J	Operating junction temperature[2]	150	°C
	Output short-circuit duration to either power supply pin[2, 3]	Indefinite	s
T_{STG}	Storage temperature	–65 to 150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Can exceed the supply voltages when $V_S \leqslant \pm 7.5V$ (15V).
2. The maximum operating junction temperature is 150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions.
   Derate above 25°C at the following rates:
   FE package at 6.7mW/°C
   N package at 9.5mW/°C
   D package at 6.25mW/°C
3. Momentary shorts to either supply are permitted in accordance to transient thermal impedance limitations determined by the package and device mounting conditions.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNIT
Single supply voltage	1.8 to 15	V
Dual supply voltage	±0.9 to ±7.5	V
Common-mode voltage (positive)	V_{CC} + 0.25	V
Common-mode voltage (negative)	V_{EE} – 0.25	V
Temperature NE grade SA grade	 0 to 70 –40 to 85	 °C °C

DC AND AC ELECTRICAL CHARACTERISTICS Unless otherwise specified, $\pm 0.9V \leq V_S \leq \pm 7.5V$ or equivalent single supply, $R_L = 10k\Omega$, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER		TEST CONDITIONS		BIAS	NE/SA5230			UNIT
						Min	Typ	Max	
V_{OS}	Offset voltage		$T_A = 25°C$		Any		0.4	3	mV
					Any		3	4	mV
V_{OS}	Drift				Any		2	5	μV/°C
I_{OS}	Offset current		$T_A = 25°C$		High		3	50	nA
			$T_A = 25°C$		Low		3	30	nA
					High			100	nA
					Low			60	nA
I_{OS}	Drift				High		0.5	1.4	nA/°C
					Low		0.3	1.4	nA/°C
I_B	Bias current		$T_A = 25°C$		High		40	150	nA
			$T_A = 25°C$		Low		20	60	nA
					High			200	nA
					Low			150	nA
I_B	Drift				High		2	4	nA/°C
					Low		2	4	nA/°C
I_S	Supply current		$V_S = \pm 0.9V$	$T_A = 25°C$	Low		110	160	μA
				$T_A = 25°C$	High		600	750	μA
					Low			250	μA
					High			800	μA
			$V_S = \pm 7.5V$	$T_A = 25°C$	Low		320	550	μA
				$T_A = 25°C$	High		1.1	1.6	mA
					Low			600	μA
					High			1.7	mA
V_{CM}	Common-mode input range		$V_{OS} \leq 6mV$, $T_A = 25°C$		Any	$V^- - 0.25$		$V^+ + 0.25$	V
					Any	V^-		V^+	V
CMRR	Common-mode rejection ratio		$V_S = \pm 7.5V$	$R_S = 10k\Omega$, $V_{CM} = \pm 7.5V$, $T_A = 25°C$	Any	85	95		dB
				$R_S = 10k\Omega$, $V_{CM} = \pm 7.5V$	Any	80			dB
PSRR	Power supply rejection ratio		$T_A = 25°C$		High	90	105		dB
			$T_A = 25°C$		Low	85	95		dB
					High	75			dB
					Low	80			dB
I_L	Load current	source	$V_S = \pm 7.5V$		Any	4	10		mA
		sink	$V_S = \pm 7.5V$		Any	5	15		mA
		source	$V_S = \pm 0.9V$		Any	1	5		mA
		sink	$V_S = \pm 0.9V$		Any	2	6		mA
		source	$V_S = \pm 0.9V$, $T_A = 25°C$		High	4	6		mA
		sink	$V_S = \pm 0.9V$, $T_A = 25°C$		High	5	7		mA
		source	$V_S = \pm 7.5V$, $T_A = 25°C$		High		16		mA
		sink	$V_S = \pm 7.5V$, $T_A = 25°C$		High		32		mA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) Unless otherwise specified, $\pm 0.9V \leq V_S \leq \pm 7.5V$ or equivalent single supply, $R_L = 10k\Omega$, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS		BIAS	NE/SA5230			UNIT
					Min	Typ	Max	
A_{VOL}	Large-signal open-loop gain	$V_S = \pm 7.5V$	$R_L = 10k\Omega$, $T_A = 25°C$	High	120	2000		V/mV
			$R_L = 10k\Omega$, $T_A = 25°C$	Low	60	750		V/mV
				High	100			V/mV
				Low	50			V/mV
V_{OUT}	Output voltage swing	$V_S = \pm 0.9V$	$T_A = 25°C$, +SW	Any	750	800		mV
			$T_A = 25°C$, -SW	Any	750	800		mV
			+SW	Any	700			mV
			-SW	Any	700			mV
		$V_S = \pm 7.5V$	$T_A = 25°C$, +SW	Any	7.30	7.35		V
			$T_A = 25°C$, -SW	Any	-7.32	-7.35		V
			+SW	Any	7.25	7.30		V
			-SW	Any	-7.30	-7.35		V
SR	Slew rate	$T_A = 25°C$		High		0.25		V/μs
		$T_A = 25°C$		Low		0.09		V/μs
BW	Inverting unity gain bandwidth	$C_L = 100pF$, $T_A = 25°C$		High		0.6		MHz
		$C_L = 100pF$, $T_A = 25°C$		Low		0.25		MHz
θ_M	Phase margin	$C_L = 100pF$, $T_A = 25°C$		Any		70		Deg.
t_S	Settling time	$C_L = 100pF$, 0.1%		High		2		μs
		$C_L = 100pF$, 0.1%		Low		5		μs
V_{INN}	Input noise	$R_S = 0\Omega$, f = 1kHz		High		30		$nV/\sqrt{Hz}$
		$R_S = 0\Omega$, f = 1kHz		Low		60		$nV/\sqrt{Hz}$
THD	Total Harmonic Distortion	$V_S = \pm 7.5V$ $A_V = 1$, $V_{IN} = 500mV$, f = 1kHz		High		0.003		%
		$V_S = \pm 0.9V$ $A_V = 1$, $V_{IN} = 500mV$, f = 1kHz		High		0.002		%

THEORY OF OPERATION

Input Stage

Operational amplifiers which are able to function at minimum supply voltages should have input and output stage swings capable of reaching both supply voltages within a few millivolts in order to achieve ease of quiescent biasing and to have maximum input/output signal handling capability. The input stage of the NE5230 has a common-mode voltage range that not only includes the entire supply voltage range, but also allows either supply to be exceeded by 250mV without increasing the input offset voltage by more than 6mV. This is unequalled by any other operational amplifier today.

In order to accomplish the feat of rail-to-rail input common-mode range, two emitter-coupled differential pairs are placed in parallel so that the common-mode voltage of one can reach the positive supply rail and the other can reach the negative supply rail. The simplified schematic of Figure 1 shows how the complementary emitter-coupler transistors are configured to form the basic input stage cell. Common-mode input signal voltages in the range from 0.8V above V_{EE} to V_{CC} are handled completely by the NPN pair, Q3 and Q4, while common-mode input signal voltages in the range of V_{EE} to 0.8V above V_{EE} are processed only by the PNP pair, Q1 and Q2. The intermediate range of input voltages requires that both the NPN and PNP pairs are operating. The collector currents of the input transistors are summed by the current combiner circuit composed of transistors Q8 through Q11 into one output current. Transistor Q8 is connected as a diode to ensure that the outputs of Q2 and Q4 are properly subtracted from those of Q1 and Q3.

The input stage was designed to overcome two important problems for rail-to-rail capability. As the common-mode voltage moves from the range where only the NPN pair was operating to where both of the input pairs were operating, the effective transconductance would change by a factor of two. Frequency compensation for the ranges where one input pair was operating would, of course, not be optimal for the range where both pairs were operating. Secondly, fast changes in the common-mode voltage would abruptly saturate and restore the emitter current sources, causing transient distortion. These problems were overcome by assuring that only the input transistor pair which is able to function properly is active. The NPN pair is normally activated by the current source I_{B1} through Q5 and the current mirror Q6 and Q7, assuming the PNP pair is non-conducting. When the common-mode input voltage passes below the reference voltage, $V_{B1} = 0.8V$ at the base of Q5, the emitter current is gradually steered toward the PNP pair, away from the NPN pair. The transfer of the emitter currents between the complementary input pairs occurs in a voltage range of about 120mV around the reference voltage V_{B1}. In this way the sum of the emitter currents for each of the NPN and PNP transistor pairs is kept constant; this ensures that the transconductance of the parallel combination will be constant, since the transconductance of bipolar transistors is proportional to their emitter currents.

An essential requirement of this kind of input stage is to minimize the changes in input offset voltage between that of the NPN and PNP transistor pair which occurs when the input common-mode voltage crosses the internal reference voltage, V_{B1}. Careful circuit layout with a cross-coupled quad for each input pair has yielded a typical input offset voltage of less than 0.3mV and a change in the input offset voltage of less than 0.1mV.

Output Stage

Processing output voltage swings that nominally reach to less than 100mV of either supply voltage can only be achieved by a pair of complementary common-emitter connected transistors. Normally, such a configuration causes complex feed-forward signal paths that develop by combining biasing and driving which can be found in previous low supply voltage designs. The unique output stage of the NE5230 separates the functions of driving and biasing, as shown in the simplified schematic of Figure 2, and has the advantage of a shorter signal path which leads to increasing the effective bandwidth.

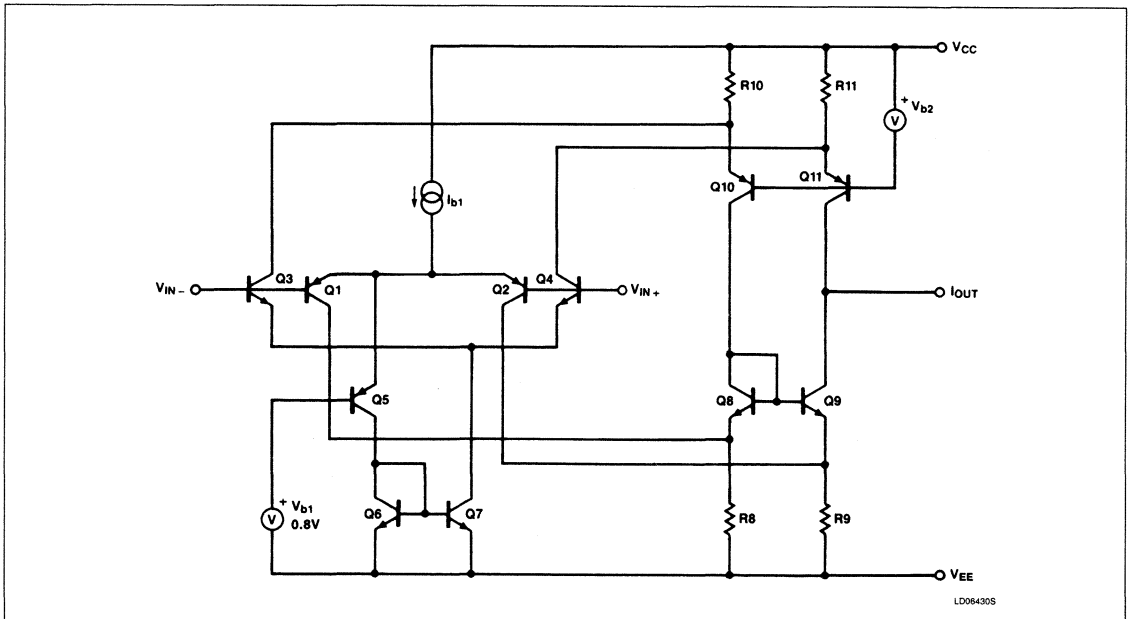


Figure 1. Input Stage

This output stage consists of two parts: the Darlington output transistors and the class AB control regulator. The output transistor Q3 connected with the Darlington transistors Q4 and Q5 can source up to 10mA to an output load. The output of NPN Darlington connected transistors Q1 and Q2 together are able to sink an output current of 10mA. Accurate and efficient class AB control is necessary to insure that none of the output transistors are ever completely cut off. This is accomplished by the differential amplifier (formed by Q8 and Q9) which controls the biasing of the output transistors. The differential amplifier compares the summed voltages across two diodes, D1 and D2, at the base of Q8 with the summed voltages across the base-emitter diodes of the output transistors Q1 and Q3. The base-emitter voltage of Q3 is converted into a current by Q6 and R6 and reconverted into a voltage across the base-emitter diode of Q7 and R7. The summed voltage across the base-emitter diodes of the output transistors Q3 and Q1 is proportional to the logarithm of the product of the push and pull currents I_{OP} and I_{ON}, respectively. The combined voltages across diodes D1 and D2 are proportional to the logarithm of the square of the reference current I_{B1}. When the diode characteristics and temperatures of the pairs Q1, D1 and Q3, Q2 are equal, the relation $I_{OP} \times I_{ON} = I_{B1} \times I_{B1}$ is satisfied.

Separating the functions of biasing and driving prevents the driving signals from becoming delayed by the biasing circuit. The output Darlington transistors are directly accessible for in-phase driving signals on the bases of Q5 and Q2. This is very important for simple high-frequency compensation. The output transistors can be high-frequency compensated by Miller capacitors CM1A and CM1B connected from the collectors to the bases of the output Darlington transistors.

A general-purpose op amp of this type must have enough open-loop gain for applications when the output is driving a low resistance load. The NE5230 accomplishes this by inserting an intermediate common-emitter stage between the input and output stages. The three stages provide a very large gain, but the op amp now has three natural dominant poles — one at the output of each common-emitter stage. Frequency compensation is implemented with a simple scheme of nested, pole-splitting Miller integrators. The Miller capacitors CM1A and CM1B are the first part of the nested structure, and provide compensation for the output and intermediate stages. A second pair of Miller integrators provide pole-splitting compensation for the pole from the input stage and the pole resulting from the compensated combination of poles from the intermediate and output stages. The result is a stable, internally-compensated op amp with a phase margin of 70 degrees.

THERMAL CONSIDERATIONS

When using the NE5230, the internal power dissipation capabilities of each package should be considered. Signetics does not recommend operation at die temperatures above 110°C in the SO package because of its inherently smaller package mass. Die temperatures of 150°C can be tolerated in all the other packages. With this in mind, the following equation can be used to estimate the die temperature:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

Where $T_A \equiv$ Ambient Temperature
T_J = Die Temperature
$P_D \equiv$ Power Dissipation
$= (I_{CC} \times V_{CC})$
$\theta_{JA} \equiv$ Package thermal resistance
$= 270°C/W$ for SO-8 in PC board mounting

See the packaging section for information regarding other methods of mounting.

$\theta_{JA} = 100°C/W$ for the plastic DIP;
$\theta_{JA} = 110°C/W$ for the ceramic DIP.

The maximum supply voltage for the part is 15V and the typical supply current is 1.1mA (1.6mA max). For operation at supply voltages other than the maximum, see the data

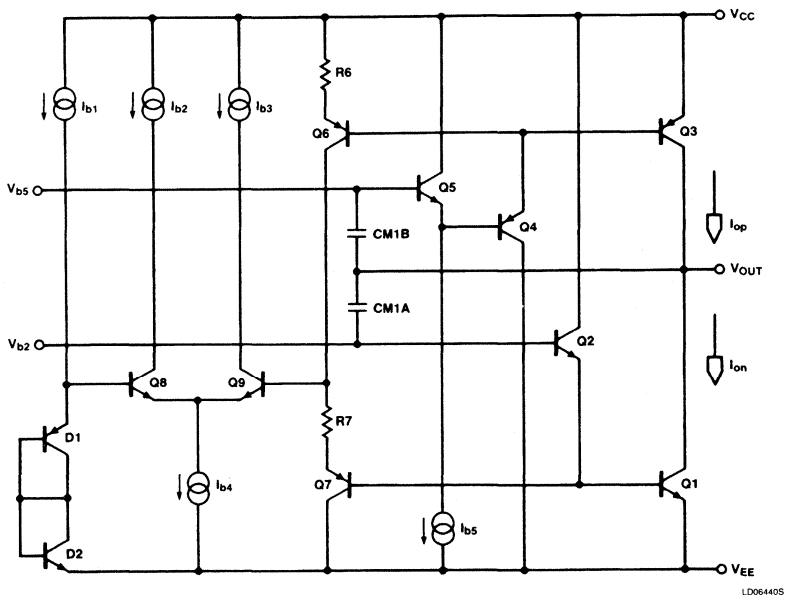


Figure 2. Output Stage

sheet for I_{CC} versus V_{CC} curves. The supply current is somewhat proportional to temperature and varies no more than 100μA between 25°C and either temperature extreme.

Operation at higher junction temperatures than that recommended is possible but will result in lower MTBF (Mean Time Between Failures). This should be considered before operating beyond recommended die temperature because of the overall reliability degradation.

DESIGN TECHNIQUES AND APPLICATIONS

The NE5230 is a very user-friendly amplifier for an engineer to design into any type of system. The supply current adjust pin (Pin 5) can be left open or tied through a pot or fixed resistor to the most negative supply (i.e., ground for single supply or to the negative supply for split supplies). The minimum supply current is achieved by leaving this pin open. In this state it will also decrease the bandwidth and slew rate. When tied directly to the most negative supply, the device has full bandwidth, slew rate and I_{CC}. The programming of the current-control pin depends on the trade-offs which can be made in the designer's application. The graph in Figure 3 will help by showing bandwidth versus I_{CC}. As can be seen, the supply current can be varied anywhere over the range of 100μA to 600μA for a supply voltage of 1.8V. An external resistor can be inserted between the current control pin and the most negative supply. The resistor can be selected between 1Ω to 100kΩ to provide any required supply current over the indicated range. In addition, a small varying voltage on the bias current control pin could be used for such exotic things as changing the gain-bandwidth for voltage controlled low pass filters or amplitude modulation. Furthermore, control over the slew rate and the rise time of the amplifier can be obtained in the same manner. This control over the slew rate also changes the settling time and overshoot in pulse response applications. The settling time to 0.1% changes from 5μs at low bias to 2μs at high bias. The supply current control can also be utilized for wave-shaping applications such as for pulse or triangular waveforms. The gain-bandwidth can be varied from between 250kHz at low bias to 600kHz at high bias current. The slew rate range is 0.08V/μs at low bias and 0.25V/μs at high bias.

The full output power bandwidth range for V_{CC} equals 2V, is above 40kHz for the maximum bias current setting and greater than 10kHz at the minimum bias current setting.

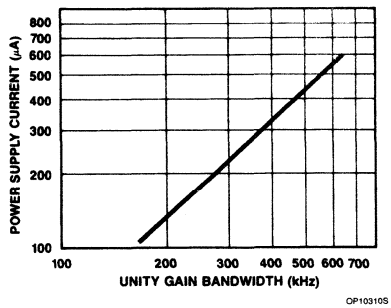
If extremely low signal distortion (< 0.05%) is required at low supply voltages, exclude the common-mode crossover point (V_{B1}) from the common-mode signal range. This can be accomplished by proper bias selection or by using an inverting amplifier configuration.

Most single supply designs necessitate that the inputs to the op amp be biased between V_{CC} and ground. This is to assure that the input signal swing is within the working common-mode range of the amplifier. This leads to another helpful and unique property of the NE5230 that other CMOS and bipolar low voltage parts cannot achieve. It is the simple fact that the input common-mode voltage can go beyond either the positive or negative supply voltages. This benefit is made very clear in a non-inverting voltage-follower configuration. This is shown in Figure 4 where the input sine wave allows an undistorted output sine wave which will swing less than 100mV of either supply voltage. Many competitive parts will show severe clipping caused by input common-mode limitations. The NE5230 in this configuration offers more freedom for quiescent biasing of the inputs close to the positive supply rail where similar op amps would not allow signal processing.

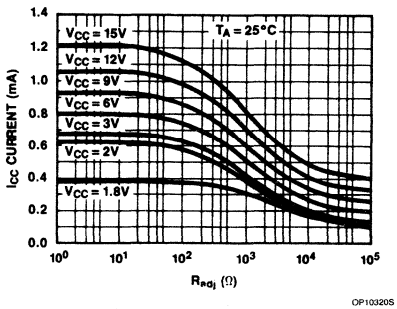
There are not as many considerations when designing with the NE5230 as with other devices. Since the NE5230 is internally-compensated and has a unity gain-bandwidth of 600kHz, board layout is not so stringent as for very high frequency devices such as the NE5205. The output capability of the NE5230 allows it to drive relatively high capacitive loads and small resistive loads. The power supply pins should be decoupled with a low-pass RC network as close to the supply pins as possible to eliminate 60Hz and other external power line noise, although the power supply rejection ratio (PSRR) for the part is very high. The pinout for the NE5230 is the same as the standard single op amp pinout with the exception of the bias current adjusting pin.

REMOTE TRANSDUCER WITH CURRENT TRANSMISSION

There are many ways to transmit information along two wires, but current transmission is



a. Unity Gain Bandwidth vs Power Supply Current for $V_{CC} = \pm 0.9V$



b. I_{CC} Current vs Bias Current Adjusting Resistor for Several Supply Voltages

Figure 3

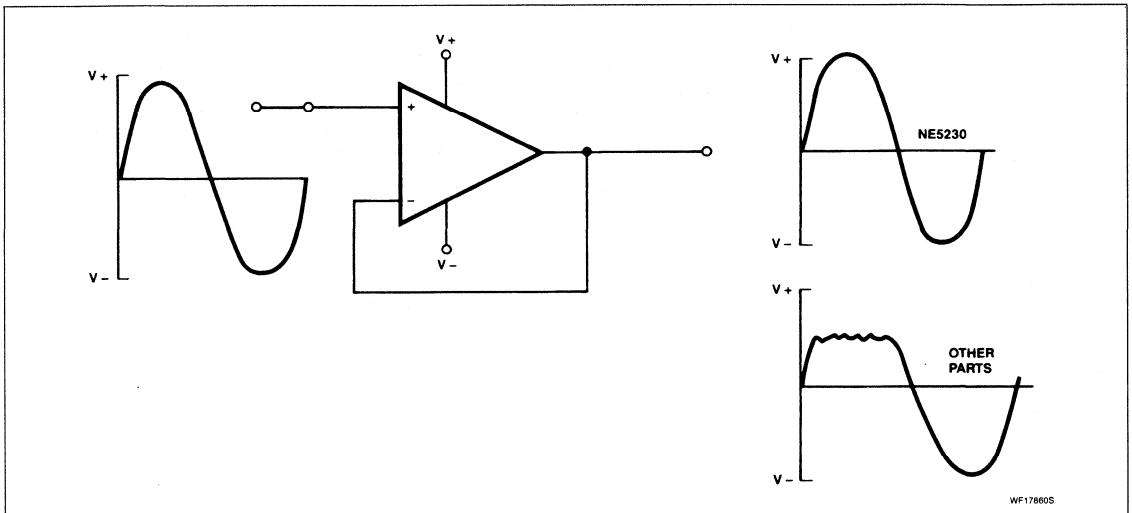


Figure 4. In a Non-Inverting Voltage-Follower Configuration, the NE5230 will Give Full Rail-to-Rail Swing. Other Low Voltage Amplifiers will not Because they are Limited by their Input Common-Mode Range and Output Swing Capability

the most beneficial when the sensing of remote signals is the aim. It is further enhanced in the form of 4 to 20mA information which is used in many control-type systems. This method of transmission provides immunity from line voltage drops, large load resistance variations, and voltage noise pickup. The zero reference of 4mA not only can show if there is a break in the line when no current is flowing, but also can power the transducer at the remote location. Usually the transducer itself is not equipped to provide for the current transmission. The unique features of the NE5230 can provide high output current capability coupled with low power consumption. It can be remotely connected to the transducer to create a current loop with minimal external components. The circuit for this is shown in Figure 5. Here, the part is configured as a voltage-to-current, or transconductance amplifier. This is a novel circuit that takes advantage of the NE5230's large open-loop gain. In AC applications, the load current will decrease as the open-loop gain rolls off in magnitude. The low offset voltage and current sinking capabilities of the NE5230 must also be considered in this application.

The NE5230 circuit shown in Figure 5 is a pseudo transistor configuration. The inverting input is equivalent to the "base," the point where V_{EE} and the non-inverting input meet is the "emitter," and the connection after the output diode meets the V_{CC} pin is the collector. The output diode is essential to keep the output from saturating in this configuration. From here it can be seen that the base and emitter form a voltage-follower and the voltage present at R_C must equal the input voltage present at the inverting input. Also, the emitter and collector form a current-follower and the current flowing through R_C is equivalent to the current through R_L and the amplifier. This sets up the current loop. Therefore, the following equation can be formulated for the working current transmission line. The load current is:

$$I_L = V_{IN} / R_C \quad (2)$$

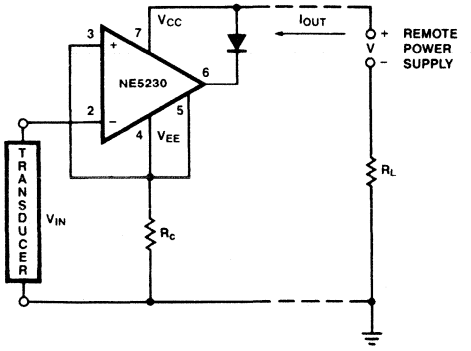
and proportional to the input voltage for a set R_C. Also, the current is constant no matter what load resistance is used while within the operating bandwidth range of the op amp. When the NE5230's supply voltage falls past a certain point, the current cannot remain constant. This is the "voltage compliance" and is very good for this application because of the near rail output voltage. The equation that determines the voltage compliance as well as the largest possible load resistor for the NE5230 is as follows:

$$R_{L\ max} = [V_{remote\ supply}) - V_{CC\ min} - V_{IN\ max}] / I_L \quad (3)$$

Where $V_{CC\ min}$ is the worst-case power supply voltage (approximately 1.8V) that will still keep the part operational. As an example, when using a 15V remote power supply, a current sensing resistor of 1Ω, and an input voltage (V_{IN}) of 20mV, the output current (I_L) is 20mA. Furthermore, a load resistance of zero to approximately 650Ω can be inserted in the loop without any change in current when the bias current-control pin is tied to the negative supply pin. The voltage drop across the load and line resistance will not affect the NE5230 because it will operate down to 1.8V. With a 15V remote supply, the voltage available at the amplifier is still enough to power it with the maximum 20mA output into the 650Ω load.

What this means is that several instruments, such as a chart recorder, a meter, or a controller, as well as a long cable, can be connected in series on the loop and still obtain accurate readings if the total resistance does not exceed 650Ω. Furthermore, any variation of resistance in this range will not change the output current.

Any voltage output type transducer can be used, but one that does not need external DC voltage or current excitation to limit the maximum possible load resistance is preferable. Even this problem can be surmounted if the supply power needed by the transducer is compatible with the NE5230. The power goes up the line to the transducer and amplifier while the transducer signal is sent back via the current output of the NE5230 transconductance configuration. The voltage range on the input can be changed for transducers that produce a large output by simply increasing the current sense resistor to get the corresponding 4 to 20mA output current. If a very long line is used which causes high line resistance, a current repeater could be inserted into the line. The same configuration of Figure 5 can be used

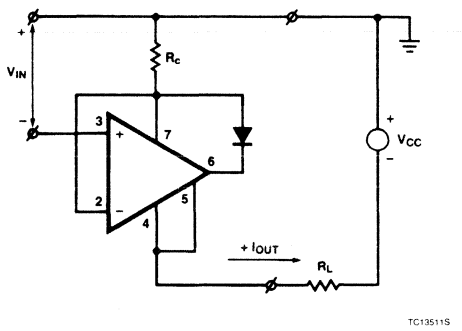


NOTES:
1. $I_{OUT} = V_{IN}/R_C$
2. $R_{L\ max} \simeq \frac{V_{REMOTE} - 1.8V - V_{IN\ max}}{I_{OUT}}$

For $R_C = 1\Omega$

I_{OUT}	V_{IN}
4mA	4mV
20mA	20mV

a. The NE5230 as a Remote Transducer Transconductance Amp With 4 – 20mA Current Transmission Output Capability



b. The Same Type of Circuit as Figure 5a, but for Sourcing Current to the Load

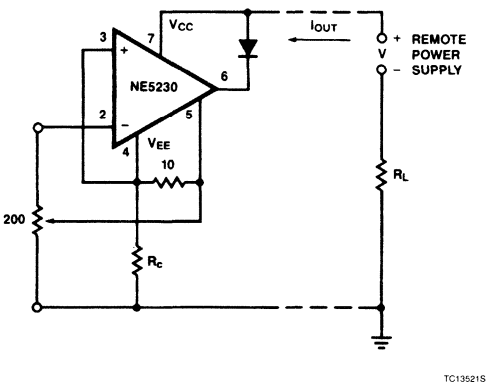
Figure 5

with exception of a resistor across the input and line ground to convert the current back to voltage. Again, the current sensing resistor will set up the transconductance and the part will receive power from the line.

TEMPERATURE TRANSDUCER

A variation on the previous circuit makes use of the supply current control pin. The voltage present at this pin is proportional to absolute temperature (PTAT) because it is produced by the amplifier bias current through an internal resistor divider in a PTAT cell. If the control pin is connected to the input pin, the NE5230 itself can be used as a temperature transducer. If the center tap of a resistive pot is connected to the control pin with one side to ground and the other to the inverting input, the voltage can be changed to give different temperature versus output current conditions (see Figure 6). For additional control, the output current is still proportional to the input voltage differential divided by the current sense resistor.

When using the NE5230 as a temperature transducer, the thermal considerations in the previous section must be kept in mind.



NOTES:
1. $I_{OUT} = V_{IN}/R_C$
2. $R_L Max \simeq \frac{V_{REMOTE} - 1.8V - V_{IN} Max}{I_{OUT}}$

For $RC = 1\Omega$

I_{OUT}	V_{IN}
4mA	4mV
20mA	20mV

Figure 6. NE5230 Remote Temperature Transducer Utilizing 4 – 20mA Current Transmission. This Application Shows the use of the Accessibility of the PTAT Cell in the Device to Make the Part, Itself, a Transducer

HALF-WAVE RECTIFIER WITH RAIL-TO-GROUND OUTPUT SWING

Since the NE5230 input common-mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction becomes a simple task. All that is needed are two external resistors; there is no need for diodes or matched resistors. Moreover, it can have either positive- or negative-going outputs, depending on the way the bias is arranged. This can be seen in Figure 7. Circuit (a) is biased to ground, while circuit (b) is biased to the positive supply. This rather unusual biasing does not cause any problems with the NE5230 because of the unique internal saturation detectors incorporated into the part to keep the PNP and NPN output transistors out of "hard" saturation. It is therefore relatively quick to recover from a saturated output condition. Furthermore, the device does not have parasitic current draw when the output is biased to either rail. This makes it possible to bias the NE5230 into "saturation" and obtain half-wave rectification with good recovery. The simplicity of biasing and the rail-to-ground half-sine wave swing are unique to this device. The circuit gain can be changed by the standard op amp gain equations for an inverting configuration.

It can be seen in these configurations that the op amp cannot respond to one-half of the incoming waveform. It cannot respond because the waveform forces the amplifier to swing the output beyond either ground or the positive supply rail, depending on the biasing, and, also, the output cannot disengage during this half cycle. During the other half cycle, however, the amplifier achieves a half-wave that can have a peak equal to the total supply voltage. The photographs in Figure 8 show the effect of the different biasing schemes, as well as the wide bandwidth (it works over the full audio range), that the NE5230 can achieve in this configuration.

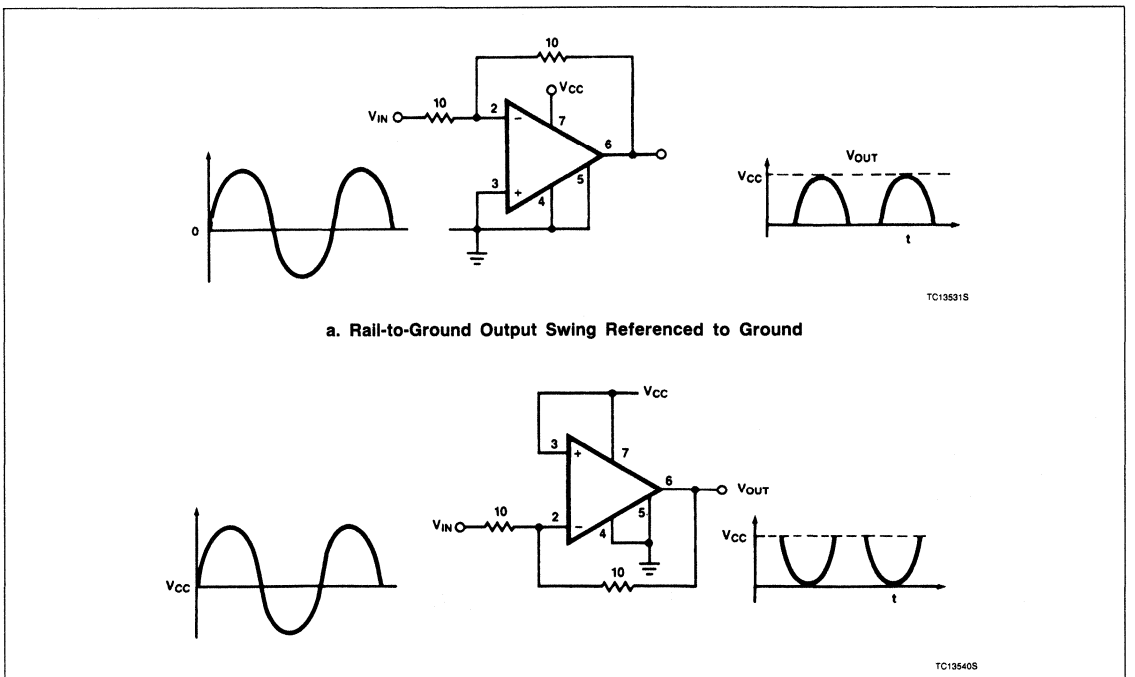
By adding another NE5230 in an inverting summer configuration at the output of the half-wave rectifier, a full-wave can be realized. The values for the input and feedback resistors must be chosen so that each peak will have equal amplitudes. A table for calculating values is included in Figure 9. The summing network combines the input signal at the half-wave and adds it to double the half-wave's output, resulting in the full-wave. The output waveform can be referenced to the supply or ground, depending on the half-wave configuration. Again, no diodes are needed to achieve the rectification.

This circuit could be used in conjunction with the remote transducer to convert a received AC output signal into a DC level at the full-wave output for meters or chart recorders that need DC levels.

CONCLUSION

The NE5230 is a versatile op amp in its own right. The part was designed to give low voltage and low power operation without the limitations of previously available amplifiers that had a multitude of problems. The previous application examples are unique to this amplifier and save the user money by excluding various passive components that would have been needed if not for the NE5230's special input and output stages.

The NE5230 has a combination of novel specifications which allows the designer to implement it easily into existing low-supply voltage designs and to enhance their performance. It also offers the engineer the freedom to achieve greater amplifier system design goals. The low input referenced noise voltage eases the restrictions on designs

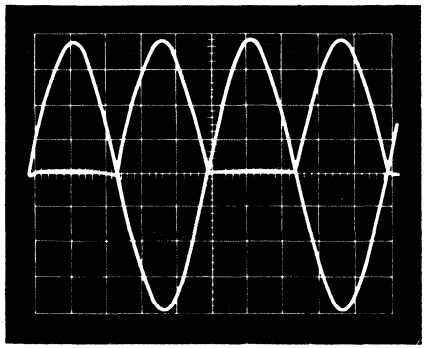


a. Rail-to-Ground Output Swing Referenced to Ground

b. Negative-Going Output Referenced to V_{CC}

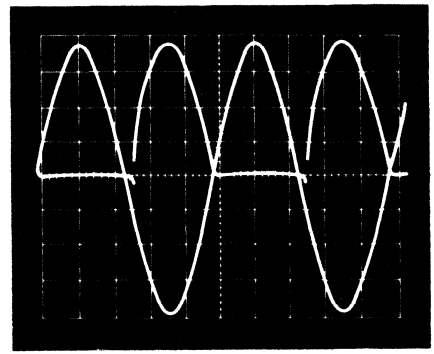
Figure 7. Half-Wave Rectifier With Positive-Going Output Swings

where S/N ratios are important. The wide full-power bandwidth and output load handling capability allow it to fit into portable audio applications. The truly ample open-loop gain and low power consumption easily lend themselves to the requirements of remote transducer applications. The low, untrimmed typical offset voltage and low offset currents help to reduce errors in signal processing designs. The amplifier is well isolated from changes on the supply lines by its typical power supply rejection ratio of 105dB.



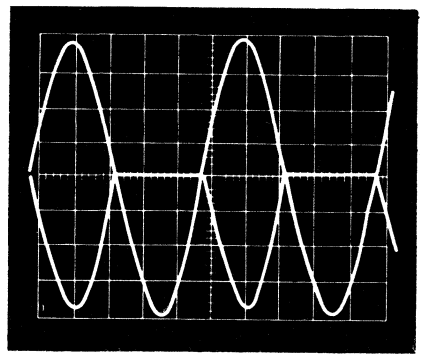
WF17870S

500mV/DIV 200μS/DIV
Biased to Ground



WF17880S

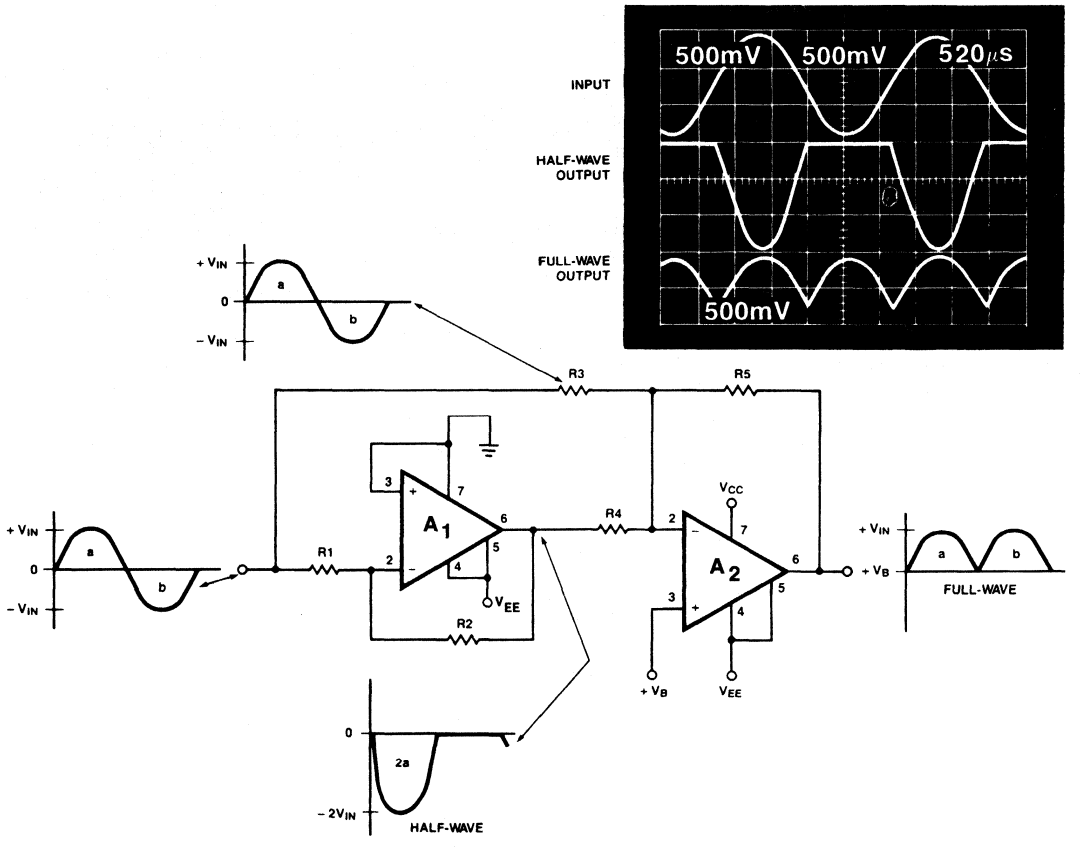
500mV/DIV 20μS/DIV
Biased to Ground



WF17890S

500mV/DIV 20μS/DIV
Biased to Positive Rail

Figure 8. Performance Waveforms for the Circuits in Figure 7. Good Response is Shown at 1 and 10kHz for Both Circuits Under Full Swing With a 2V Supply



NOTES:
R2 = 2 R1
R4 = R5 = R3
$+V_B$ will vary output reference.
For single supply operation V_{EE} can be grounded on A2.

Figure 9. Adding an Inverting Summer to the Input and Output of the Half-Wave Rectifier will Result in Full-Wave

REFERENCES

Johan H. Huijsing, "Multi-stage Amplifier with Capacitive Nesting for Frequency Compensation," U.S. Patent Application Serial No. 602.234, filed April 19, 1984.

Bob Blauschild, "Differential Amplifier with Rail-to-Rail Capability," U.S. Patent Application Serial No. 525.181, filed August 23, 1983.

Operational Amplifiers — Characteristics and Applications, Robert G. Irvine, Prentice-Hall, Inc., Englewood Cliffs, NJ 07632, 1981.

Transducer Interface Handbook — A Guide to Analog Signal Conditioning, Edited by Daniel H. Sheingold, Analog Devices, Inc., Norwood, MA 02062, 1981.

Document	853-1445
ECN No.	99885
Date of Issue	June 28, 1990
Status	Product Specification
Application Specific Product	

NE/SA5234

Matched quad high-performance low-voltage operational amplifier

DESCRIPTION

The NE/SA5234 is a matched, low voltage, high performance quad operational amplifier. Among its unique input and output characteristics is the capability for both input and output rail-to-rail operation, particularly critical in low voltage applications. The output swings to less than 50mV of both rails across the entire power supply range. The NE/SA5234 is capable of delivering 5.5V peak-to-peak across a 600Ω load and will typically draw only 700μA per amplifier. The bandwidth is 2.5MHz and the 1% settling time is 1.4μs.

FEATURES

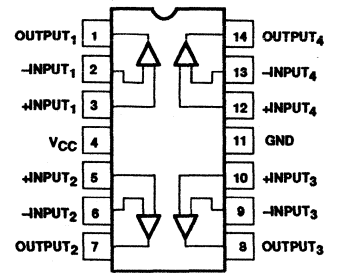
- Wide common-mode input voltage range: 250mV beyond both rails
- Output swing within 50mV of both rails
- Functionality to 1.8V typical
- Low current consumption: 700μA per amplifier
- ±15mA output current capability
- Unity gain bandwidth: 2.5MHz
- Slew rate: 0.8V/μs
- Low noise: 25nV/√Hz
- Electrostatic discharge protection
- Short-circuit protection
- Output inversion prevention

APPLICATIONS

- Automotive electronics
- Signal conditioning and sensing amplification
- Portable instrumentation
  - –Test and measurement
  - –Medical monitors and diagnostics
  - –Remote meters
- Audio equipment
- Security systems
- Communications
  - –Pagers
  - –Cellular telephone
  - –LAN
  - –5V Datacom bus
- Error amplifier in motor drives
- Transducer buffer amplifier

PIN CONFIGURATION

N, and D PACKAGES



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE5234D
14-Pin Plastic DIP	0 to +70°C	NE5234N
14-Pin Plastic SO	–40 to +85°C	SA5234D
14-Pin Plastic DIP	–40 to +85°C	SA5234N

Matched quad high-performance low-voltage operational amplifier

NE/SA5234

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
V_{ESD}	ESD protection voltage at any pin[5] human body model robot model	 2000 200	 V V
V_S	Dual supply voltage	±3.5	V
V_{DP}	Voltage at any device pin[1]	$V_S \pm 0.5$	V
I_{DP}	Current into any device pin[1]	± 50	mA
V_{IN}	Differential input voltage[2]	0.5	V
V_{CM}	Common–mode input voltage (positive)	$V_{CC} + 0.5$	V
V_{CM}	Common–mode input voltage (negative)	$V_{CC} - 0.5$	V
P_D	Power dissipation[3]	500	mW
T_J	Operating junction temperature[3]	+150	°C
V_{SC}	Supply voltage allowing indefinite output short circuit to either rail[3,4]	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C
θ_{JA}	Thermal impedance 14 pin Plastic DIP 14 pin Plastic SO	 80 115	 °C/W °C/W

NOTES:
1. Each pin is protected by ESD diodes. The voltage at any pin is limited by the ESD diodes.
2. The differential input of each amplifier is limited by two internal diodes, connected in parallel and opposite to each other. For more differential input range, use differential resistors in series with the input pins.
3. The maximum operating junction temperature is +150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions. Derates above +25°C: F package at 6.7mW/°C; N package at 9.5mW/°C; D package at 6.25mW/°C.
4. Simultaneous short circuits of two or more amplifiers to the positive or negative rail can exceed the power dissipation ratings and cause eventual destruction of the device.
5. Guaranteed by design.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	+2 to +5.5	V
V_S	Dual supply voltage	±1 to ±2.75	V
V_{CM}	Common–mode input voltage (positive)	$V_{CC} + 0.25$	V
V_{CM}	Common–mode input voltage (negative)	$V_{EE} - 0.25$	V
T_A	Temperature NE SA	 0 to +70 –40 to +85	 °C °C

Matched quad high-performance low-voltage operational amplifier

NE/SA5234

DC ELECTRICAL CHARACTERISTICS V_{CC} = 2 to 5.5V, V_{EE} = 0V, T_A = 25°C; $V_{EE} < V_{CM} < V_{CC}$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234[2]			SA5234[2]			
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_{CC} = 5.5V		2.8	3.5		2.8	3.5	mA
		V_{CC} = 5.5V over full temperature range		3.0	3.7		3.2	3.8	mA
V_{OS}	Offset voltage			±0.2	±4, (±2)		±0.2	±4, (±2)	mV
		Over full temperature range		±0.4	±5, (±2)		±0.6	±5, (±2)	mV
$\Delta V_{OS}/\Delta T$	Offset voltage drift with temperature			4			4		µV/°C
ΔV_{OS}	Offset voltage difference between any amplifiers in the same package at the common mode level[1]			0.4	3, (2)		0.4	3, (2)	mV
		Over full temperature range		0.8	4, (2)		1.2	4, (2)	mV
I_{OS}	Offset current			±3	±20		±3	±30	nA
		Over full temperature range		±4	±30		±6	±60	nA
$\Delta I_{OS}/\Delta T$	Offset current drift with temperature			0.02	.3		0.03	.3	nA/°C
I_B	Input bias current[1]	$V_{EE} < V_{CM} < V_{EE}$ +0.5V	–150	–90		–150	–90		nA
		Over full temperature range	–175	–100		–200	–150		nA
		V_{EE} +1V < V_{CM} < V_{CC}		25	70		25	75	nA
		Over full temperature range		35	100		35	120	nA
$\Delta I_B/\Delta T$	Input bias current drift with temperature			0.5			0.5		nA/°C
ΔI_B	Input bias current difference between any amplifier in the same package at the same common mode level.	$V_{EE} < V_{CM} < V_{EE}$ +0.5V		10	30		10	30	nA
		Over full temperature range		25	50		50	70	nA
		V_{EE} +1V < V_{CM} < V_{CC}		5	20		5	20	nA
		Over full temperature range		15	30		25	50	nA
V_{CM}	Common–mode input range	$V_{OS} \leq$ 6mV	V_{EE}–0.25		V_{CC}+0.25	V_{EE}–0.25		V_{CC}+0.25	V
		$V_{OS} \leq$ 6mV over full temperature range	V_{EE}–0.1		V_{CC}+0.1	V_{EE}–0.1		V_{CC}+0.1	V
CMRR	Common–mode rejection ratio, small signal	$V_{EE} < V_{CM} < V_{EE}$+0.5V, V_{EE}+1V < V_{CM} < V_{CC}	90	100		90	100		dB
		Over full temperature range	90	100		80	90		dB
	Common–mode rejection ratio, large signal	$V_{EE} < V_{CM} < V_{CC}$		100			100		dB
		Over full temperature range		90			90		dB
PSRR	Power supply rejection ratio	$V_{EE} < V_{CM} < V_{CC}$	80	100		80	100		dB
		Over full temperature range	80	90		80	90		dB

Matched quad high-performance low-voltage operational amplifier

NE/SA5234

DC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234[2]			SA5234[2]			
			MIN	TYP	MAX	MIN	TYP	MAX	
I_L	Peak load current, sink and source		10	15		10	15		mA
		Over full temperature range	5	10		5	10		mA
A_{VOL}	Open–loop voltage gain		90	110		90	110		dB
		Over full temperature range		90			90		dB
V_{OUT}	Output voltage swing	I_{PEAK} = 0.1mA	V_{EE}+0.05		V_{CC}–0.05	V_{EE}+0.1		V_{CC}–0.1	V
		I_{PEAK} = 10mA	V_{EE}+0.25		V_{CC}–0.25	V_{EE}+0.25		V_{CC}–0.25	V
		I_{PEAK} = 5mA over full temp range	V_{EE}+0.22		V_{CC}–0.2	V_{EE}+0.2		V_{CC}–0.2	V
	Output voltage swing for V_{CC} = 2.75V, V_{EE} = –2.75V	R_L = 2kΩ	V_{EE}+0.2		V_{CC}–0.2	V_{EE}+0.2		V_{CC}–0.2	V
		R_L = 600Ω,	V_{EE}+0.25		V_{CC}–0.25	V_{EE}+0.25		V_{CC}–0.25	V

NOTES:
1. These parameters are measured for $V_{EE} < V_{CM} < V_{EE}$+.5V and for V_{EE}+1V < $V_{CM} < V_{CC}$. By design these parameters are intermediate for common mode ranges between the measured regions.
2. The values in parentheses are enhanced performance specifications available on a qualified special order basis. An optional –55 to +125°C temperature range is also available.

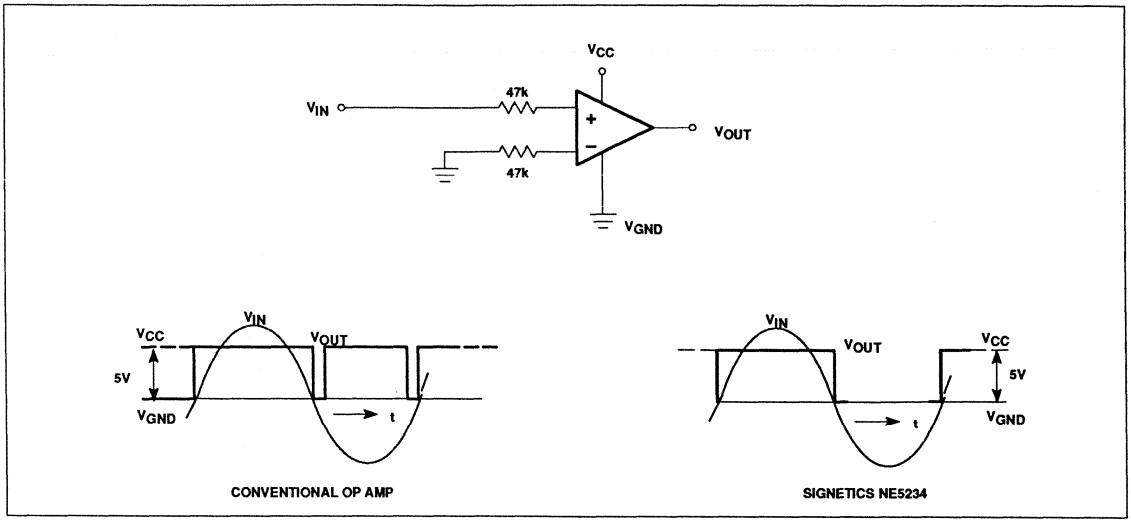
AC ELECTRICAL CHARACTERISTICS T_A = +25°C; V_{CC} = 2 to 5.5V; R_L = 10k; C_L = 100pF; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA/SE5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	Over full temperature range	.5	0.8		.5	0.8		V/μs
BW	Unity gain bandwidth: –3dB	Over full temperature range	2	2.5	4.0	2	2.5	4.0	MHz
θ_M	Phase Margin	C_L = 50pF		55			55		deg
t_S	1% settling time	A_V = 1, 1V step		1.4			1.4		μs
V_N	Input referred voltage noise	A_V = 1, R_S = 0Ω, at 1kHz		25			25		nV/$Hz^{1/2}$
THD	Total harmonic distortion	10kHz, $1V_{P-P}$, A_V = 1		0.1			0.1		%

Matched quad high-performance low-voltage operational amplifier

NE/SA5234

OUTPUT INVERSION PREVENTION



NE/SE5539
High Frequency Operational Amplifier

Product Specification

DESCRIPTION

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

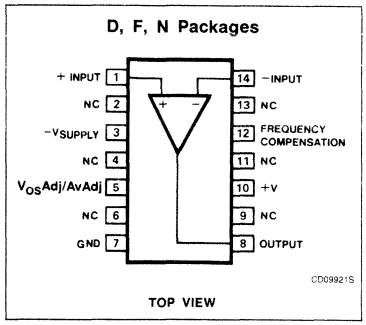
FEATURES

- **Bandwidth**
  - **Unity gain – 350MHz**
  - **Full power – 48MHz**
  - **GBW – 1.2 GHz at 17dB**
- **Slew rate: 600/Vμs**
- **A_{VOL}: 52dB typical**
- **Low noise – 4nV/$\sqrt{Hz}$ typical**
- **MIL-STD processing available**

APPLICATIONS

- **High speed datacomm**
- **Video monitors & TV**
- **Satellite communications**
- **Image processing**
- **RF instrumentation & oscillators**
- **Magnetic storage**
- **Military communications**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5539N
14-Pin Plastic SO	0 to +70°C	NE5539D
14-Pin Cerdip	0 to +70°C	NE5539F
14-Pin Plastic DIP	−55°C to +125°C	SE5539N
14-Pin Cerdip	−55°C to +125°C	SE5539F

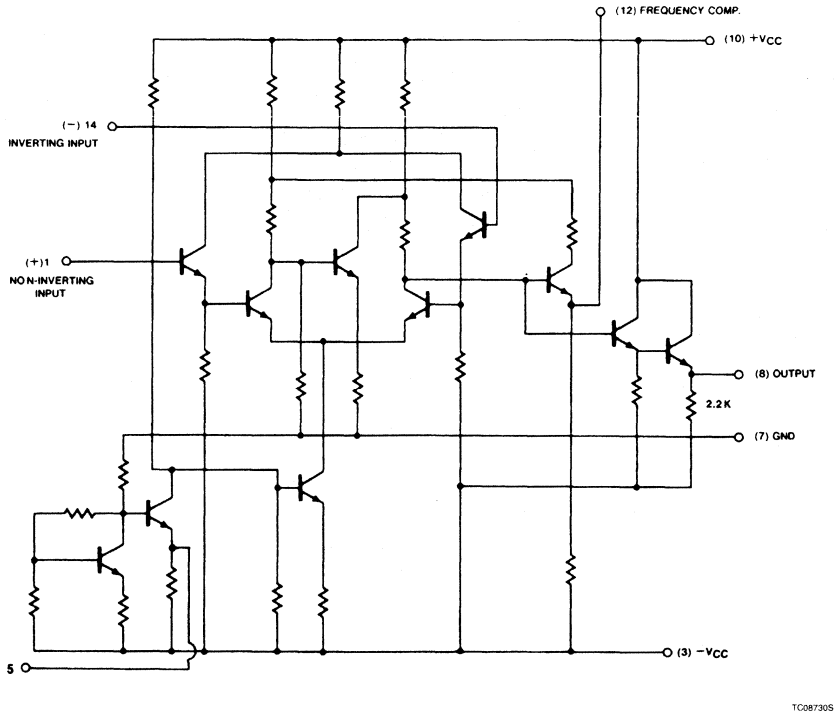
ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±12	V
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[2] F package N package D package	 1.17 1.45 0.99	 W W W
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range NE SE	 0 to 70 −55 to +125	 °C °C
T_{SOLD}	Lead temperature (10sec max)	300	°C

NOTES:

1. Differential input voltage should not exceed 0.25V to prevent excessive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
2. Derate above 25°C, at the following rates:
   F package at 9.3 mW/°C
   N package at 11.6 mW/°C
   D package at 7.9 mW/°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNIT
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$	Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
	$\Delta V_{OS}/\Delta T$				5			5		μV/°C
I_{OS}	Input offset current		Over temp		0.1	3				μA
			$T_A = 25°C$		0.1	1			2	
	$\Delta I_{OS}/\Delta T$				0.5			0.5		nA/°C
I_B	Input bias current		Over temp		6	25				μA
			$T_A = 25°C$		5	13		5	20	
	$\Delta I_B/\Delta T$				10			10		nA/°C
CMRR	Common-mode rejection ratio	F = 1kHz, $R_S = 100\Omega$, $V_{CM} \pm 1.7V$		70	80		70	80		dB
			Over temp	70	80					dB
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			NE5539			UNIT
					Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$		+Swing				+2.3	+2.7		V
				−Swing				−1.7	−2.2		
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ to GND	Over temp	+Swing	+2.3	+3.0					V
				−Swing	−1.5	−2.1					
			$T_A = 25°C$	+Swing	+2.5	+3.1					V
				−Swing	−2.0	−2.7					
$I_{CC}+$	Positive supply current	$V_O = 0$, $R_1 = \infty$		Over temp		14	18				mA
				$T_A = 25°C$		14	17		14	18	
$I_{CC}-$	Negative supply current	$V_O = 0$, $R_1 = \infty$		Over temp		11	15				mA
				$T_A = 25°C$		11	14		11	15	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000				μV/V
				$T_A = 25°C$					200	1000	
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$						47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 2\Omega$ to GND									dB
				$T_A = 25°C$				47	52	57	
A_{VOL}	Large signal voltage gain	$V_O = +2.5V, -2.0V$ $R_L = 2k\Omega$ to GND		Over temp	46		60				dB
				$T_A = 25°C$	48	53	58				

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			UNIT
					Min	Typ	Max	
V_{OS}	Input offset voltage			Over temp		2	5	mV
				$T_A = 25°C$		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	μA
				$T_A = 25°C$		0.1	1	
I_B	Input bias current			Over temp		5	20	μA
				$T_A = 25°C$		4	10	
CMRR	Common-mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$			70	85		dB
$I_{CC}+$	Positive supply current			Over temp		11	14	mA
				$T_A = 25°C$		11	13	
$I_{CC}-$	Negative supply current			Over temp		8	11	mA
				$T_A = 25°C$		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000	μV/V
				$T_A = 25°C$				
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+Swing	+1.4	+2.0		V
				−Swing	−1.1	−1.7		
			$T_A = 25°C$	+Swing	+1.5	+2.0		
				−Swing	−1.4	−1.8		

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 470Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$, $V_O = 0.1\ V_{P-P}$		1200			1200		MHz
	Small-signal bandwidth	$A_{CL} = 2$, $R_L = 150\Omega$[1]		110			110		MHz
t_S	Settling time	$A_{CL} = 2$, $R_L = 150\Omega$[1]		15			15		ns
SR	Slew rate	$A_{CL} = 2$, $R_L = 150\Omega$[1]		600			600		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$, $R_L = 150\Omega$[1]		7			7		ns
	Full power response	$A_{CL} = 2$, $R_L = 150\Omega$[1]		48			48		MHz
	Full power response	$A_V = 7$, $R_L = 150\Omega$[1]		20			20		MHz
	Input noise voltage	$R_S = 50\Omega$, 1MHz		4			4		$nV/\sqrt{Hz}$
	Input noise current	1MHz		6			6		$pA/\sqrt{Hz}$

NOTE:
1. External compensation.

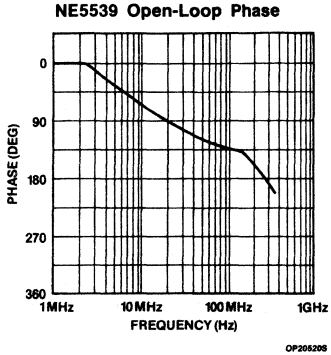
AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNIT
			Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$		700		MHz
	Small-signal bandwidth	$A_{CL} = 2$[1]		120		MHz
t_S	Settling time	$A_{CL} = 2$[1]		23		ns
SR	Slew rate	$A_{CL} = 2$[1]		330		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$[1]		4.5		ns
	Full power response	$A_{CL} = 2$[1]		20		MHz

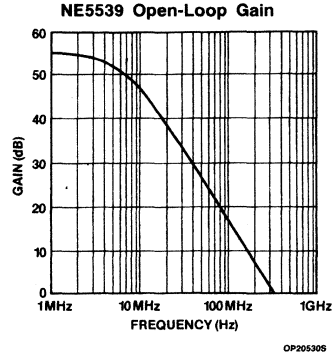
NOTE:
1. External compensation.

TYPICAL PERFORMANCE CURVES

NE5539 Open-Loop Phase

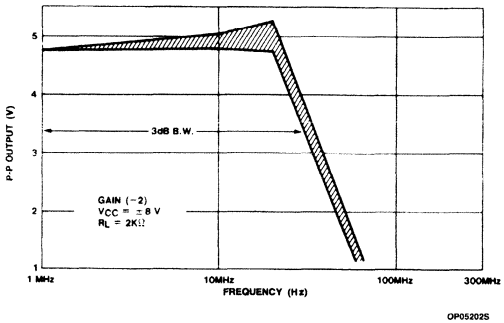


NE5539 Open-Loop Gain



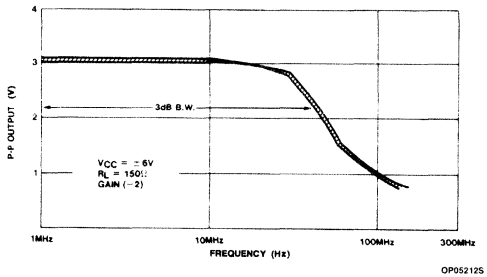
TYPICAL PERFORMANCE CURVES (Continued)

Power Bandwidth (SE)



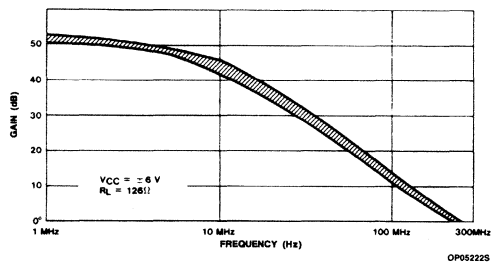
OP05202S

Power Bandwidth (NE)



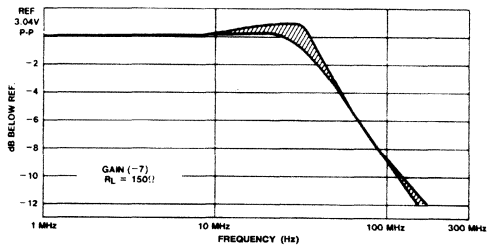
OP05212S

SE5539 Open-Loop Gain vs Frequency



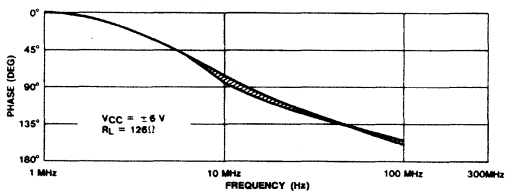
OP05222S

Power Bandwidth

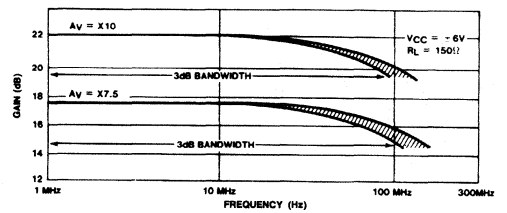


OP05231S

SE5539 Open-Loop Phase vs Frequency



Gain Bandwidth Product vs Frequency



OP05251S

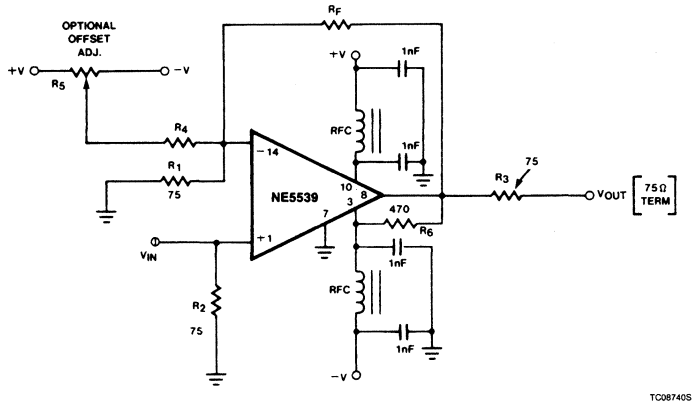
NOTE

Indicates typical distribution $-55°C \leq T_A \leq 125°C$

OP05241S

CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide-gain bandwidth amplifier, the physical circuit layout is extremely critical. Breadboarding is not recommended. A double-sided copper-clad printed cirucit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.

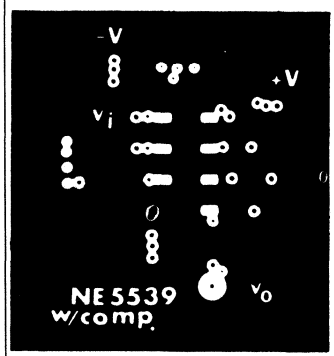


NOTES:
R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36k 5% CARBON

R_5 = 20k TRIMPOT (CERMET)
R_F = 1.5k (28dB GAIN)
R_6 = 470Ω 5% CARBON

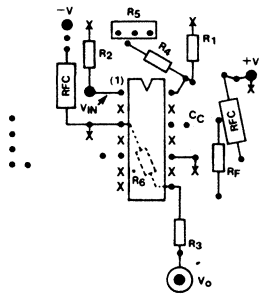
RFC 3T # 26 BUSS WIRE ON FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

Top Plane Copper[1] (Component Side)



DF05910S

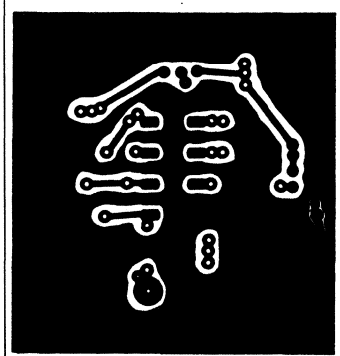
Component Side (Component Layout)



DF05920S

NOTES:
(X) Indicates ground connection to top plane.
*R_6 is on bottom side.

Bottom Plane Copper[1]



DF05930S

NOTE:
1. Bond edges of top and bottom ground plane copper.

Figure 1. 28dB Non-Inverting Amp Sample PC Layout

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in Figure 2 along with vector-scope[1] photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in Figure 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in Figure 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75Ω input and output termination impedance with a gain of approximately 10 (20dB).

NOTE:

1. The input signal was 200mV and the output 2V. V_{CC} was ±8V.

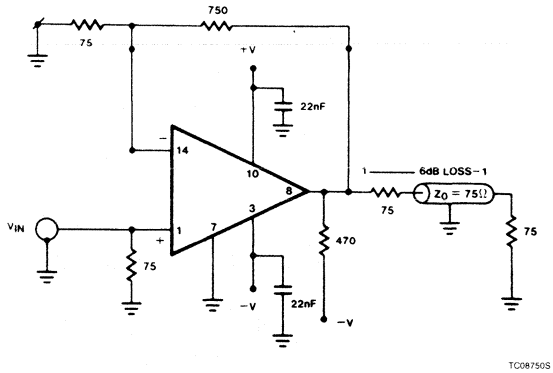


Figure 2. NE5539 Video Amplifier

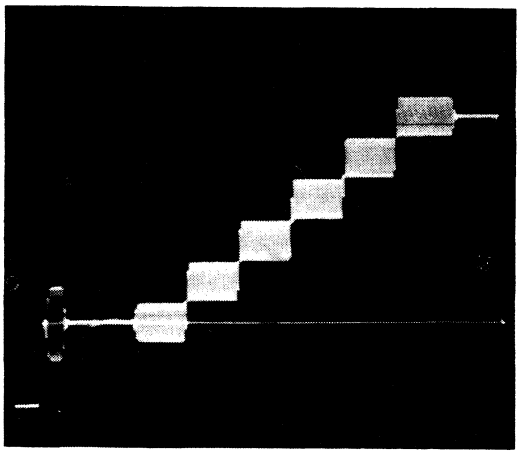


Figure 3. Input Signal

Figure 4. Differential Gain < 0.5%

NOTE:
Instruments used for these measurements were Tektronix 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

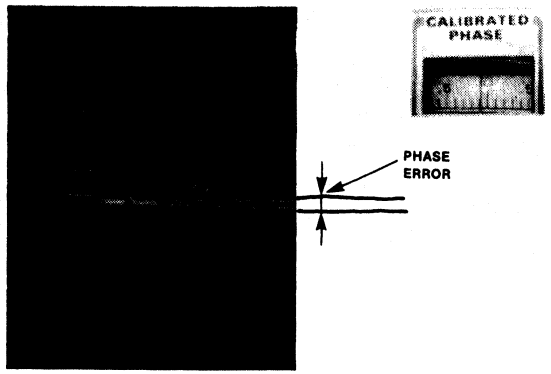


Figure 5. Differential Phase +0.1°

APPLICATIONS

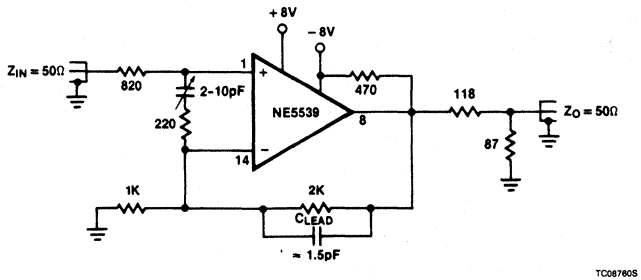


Figure 6. Non-Inverting Follower

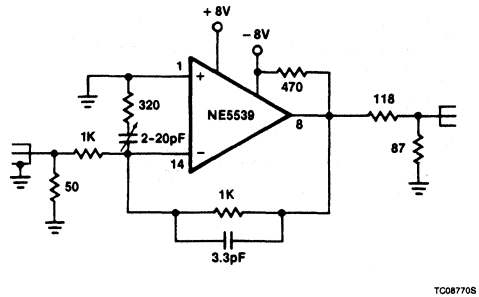


Figure 7. Inverting Follower

Document	853-1451
ECN No.	00210
Date of Issue	August 17, 1990
Status	Product Specification
RF Communications	

NE/SA5750

Audio processor – companding and amplifier section

special components for cellular radio

DESCRIPTION

The NE/SA5750 is a high performance low power audio signal processing system. The NE/SA5750 subsystems include a low noise microphone preamplifier with adustable gain, a noise cancellation switching amplifier with adjustable threshold, a voice operated transmitter (VOX) switch, VOX control, an audio compressor with buffered input, audio expandor, a unity gain power amplifier to drive a speaker, a summing power amplifier for sidetone attenuation and headphone (earpiece) drive, and an internal bandgap voltage regulator with power down capability. When used with Signetics' NE/SA5751, the complete audio processing function of an AMPS or TACS cellular telephone is easily implemented. The NE/SA5750 can also be used without the NE/SA5751 in a wide variety of radio communications applications.

FEATURES

- High performance
- 5V supply
- Adjustable VOX and noise cancellation threshold
- Adjustable gain preamplifier
- Audio companding
- ESD protected
- Open collector VOX output
- Logic inputs CMOS compatible
- Power down mode
- Built-in drivers for speaker and earpiece
- Few external components
- SOL and DIP packages

BENEFITS

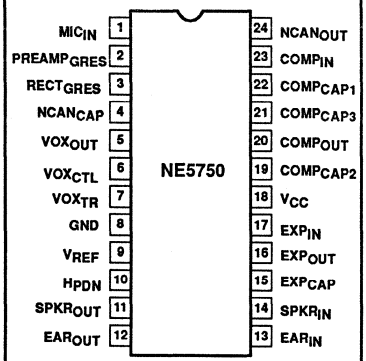
- Very compact applications
- Long battery life in portable equipment
- Complete cellular audio function with the SA5751

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION

D[1] and N PACKAGE



NOTE:
1. Available only in SOL (large SO) package.

ORDERING INFORMATION

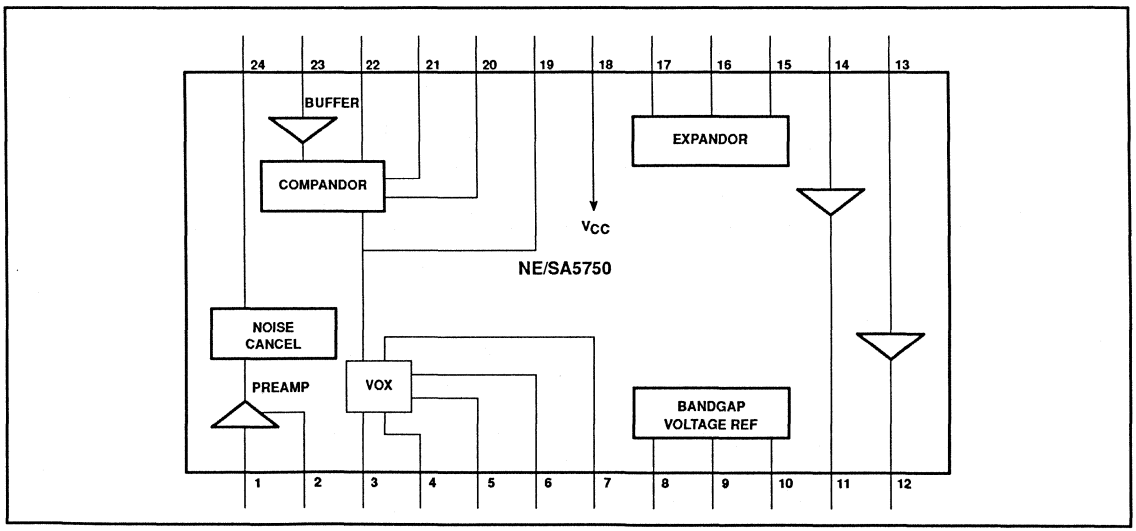
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	0 to +70°C	NE5750N
24-Pin Plastic SOL	0 to +70°C	NE5750D
24-Pin Plastic DIP	–40 to +85°C	SA5750N
24-Pin Plastic SOL	–40 to +85°C	SA5750D

Audio processor – companding and amplifier section NE/SA5750

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	MIC_{IN}	Microphone input
2	$PREAMP_{GRES}$	Preamplifier gain resistor
3	$RECT_{GRES}$	Reactifier gain resistor
4	$NCAN_{CAP}$	Noise cancellation timing capacitor
5	VOX_{OUT}	Voice operated transmission output
6	VOX_{CTL}	Voice operated transmission control
7	VOX_{TR}	Voice operated transmission threshold resistor
8	GND	Ground
9	V_{REF}	Reference voltage
10	H_{PDN}	Hardware power down
11	$SPKR_{OUT}$	Speaker output
12	EAR_{OUT}	Earpiece output
13	EAR_{IN}	Earpiece input, side tone input
14	$SPKR_{IN}$	Speaker input
15	EXP_{CAP}	Expandor timing capacitor
16	EXP_{OUT}	Expandor output
17	EXP_{IN}	Expandor input
18	V_{CC}	Positive supply
19	$COMP_{CAP2}$	Compressor timing capacitor 2
20	$COMP_{OUT}$	Compressor output
21	$COMP_{CAP3}$	Compressor timing capacitor 3
22	$COMP_{CAP1}$	Compressor timing capacitor 1
23	$COMP_{IN}$	Compressor input
24	$NCAN_{OUT}$	Noise cancellation output

BLOCK DIAGRAM



Audio processor – companding and amplifier section | NE/SA5750

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage Voltage applied to any pin	6 –0.3 to (V_{CC} + 0.3)	V V
T_{STG}	Storage temperature	–65 to +150	°C
T_A	Ambient operating temperature NE5750 SA5750	 0 to 70 –40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5.0V, 0dB = 77.5mV_{RMS}. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.75	5.0	5.25	V
I_{CC}	Supply current	No signal Power down mode		8.4 1.8	12.0 3.0	mA mA
Z_L	Load impedance pins $NCAN_{OUT}$, EXP_{OUT}		50			kΩ
	$COMP_{OUT}$[1]		10			kΩ
Z_{IN}	Input impedance $COMP_{IN}$, MIC_{IN}, $SPKR_{IN}$		40	50	60	kΩ
	EXP_{IN}[2]		2.0	2.5		kΩ
	Noise cancellation current	Pin 7, grounded	40	50	60	µA
V_{OS}	DC offset $NCAN_{OUT}$[3]		–50		50	mV

NOTES:
1. Compressor is tested in production with 50kΩ load.
2. Not tested in production.
3. Offset values are identical for both gain states of noise reduction circuit.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5.0V, 0dB level = 77.5mV_{RMS}. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	Preamplifier gain range Preamplifier voltage gain 0dB Preamplifier voltage gain 40dB	 Pin 2 open Pin 2 AC ground	0 –1.0 39.0	 0 40	40 1.0 41.0	dB dB dB
	Preamplifier noise density	Pin 2 AC grounded RS = 0 – 50kΩ unweighted20Hz–20kHz		7		$nV/\sqrt{Hz}$
		weighted CCIR DIN45405 20–20kHz		8		$nV/\sqrt{Hz}$
	Switch amplifier gain		9	10	11	dB
	Sidetone attenuation range				30	dB
Compandor 1kHz, all tests[1]						
$COMP_{OUT}$	Compressor error at –21dB output level	Input level = –42dB		0.38		dB
$COMP_{OUT}$	Compressor error at –10dB output level	Input level = –20dB	–1.0		1.0	dB
$COMP_{OUT}$	Compressor error at 0dB output level	Input level = 0dB	–1.5	0.12	1.5	dB
$COMP_{OUT}$	Compressor error at +5dB output level	Input level = +10dB	–1.0		1.0	dB
$COMP_{OUT}$	Compressor error at +12.3dB output level	Input level = +24.6dB	–1.0		1.0	dB
EXP_{OUT}	Expandor error at –42dB output level	Input level = –21dB		–0.41		dB
EXP_{OUT}	Expandor error at –21dB output level	Input level = –10.5dB	–1.0		1.0	dB

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5.0V$, 0dB level = $77.5mV_{RMS}$. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
EXP_{OUT}	Expandor error at –10dB output level	Input level = –5dB	–1.0		1.0	dB
EXP_{OUT}	Expandor error at 0dB output level	Input level = 0dB	–1.5	–0.18	1.5	dB
EXP_{OUT}	Expandor error at +10dB output level	Input level = +5dB	–1.0		1.0	dB
EXP_{OUT}	Expandor error at +24.6dB output level[2]	Input level = +12.3dB	–1.5		1.5	dB
EXP_{OUT}	Expandor V_{OS}	No signal	–50.0		50.0	mV
EXP_{OUT}	Expandor output DC shift	No signal to 0dB	–100		100	mV
	Timing capacitors compandor			2.2		µF
THD	Total harmonic distortion					
	Compressor	1kHz, 0dB		0.09	1	%
	Expandor	1kHz, 0dB		0.09	1	%
	$NCAN_{OUT}$	1kHz. Pin 2 open output level = 0dB		0.18	1	%
		1kHz, Pin 2 open output level = +25dB		0.13	1	%
	Speaker amplifier Drive capability				40	mA_{P-P}
	Output swing (<1% THD)	50Ω load	2	3.2		V_{P-P}
		100Ω load	3	4.1		V_{P-P}
		No load	4	4.9		V_{P-P}
	Ear amplifier Drive capability				10	mA_{P-P}
	Output swing (<1% THD)	300Ω load	3	4.3		V_{P-P}
		2000Ω load	4	4.9		V_{P-P}
		No load	4	4.9		V_{P-P}
VOX_{OUT}	Sink current				0.5	mA
	Low level High level	Open collector $I_L = 0.5mA$	 4	0.07 5	0.4	V V
VOX_{CTL}	Input current Low		–50	–21	0	µA
	High		–10		+10	µA
	Input level Low High		0 3.5		1.5 5	V V
H_{PDN}	Input current Low		–10		+10	µA
	High		–10		+10	µA
	Input level Low High		0 3.5		1.5 5	V V
	Reference filter capacitor			10		µF

NOTE:
1. Measurements are relative to 0dB output.
2. Measurement is absolute and indicative of the output dynamic range capability.

Audio processor – companding and amplifier section NE/SA5750

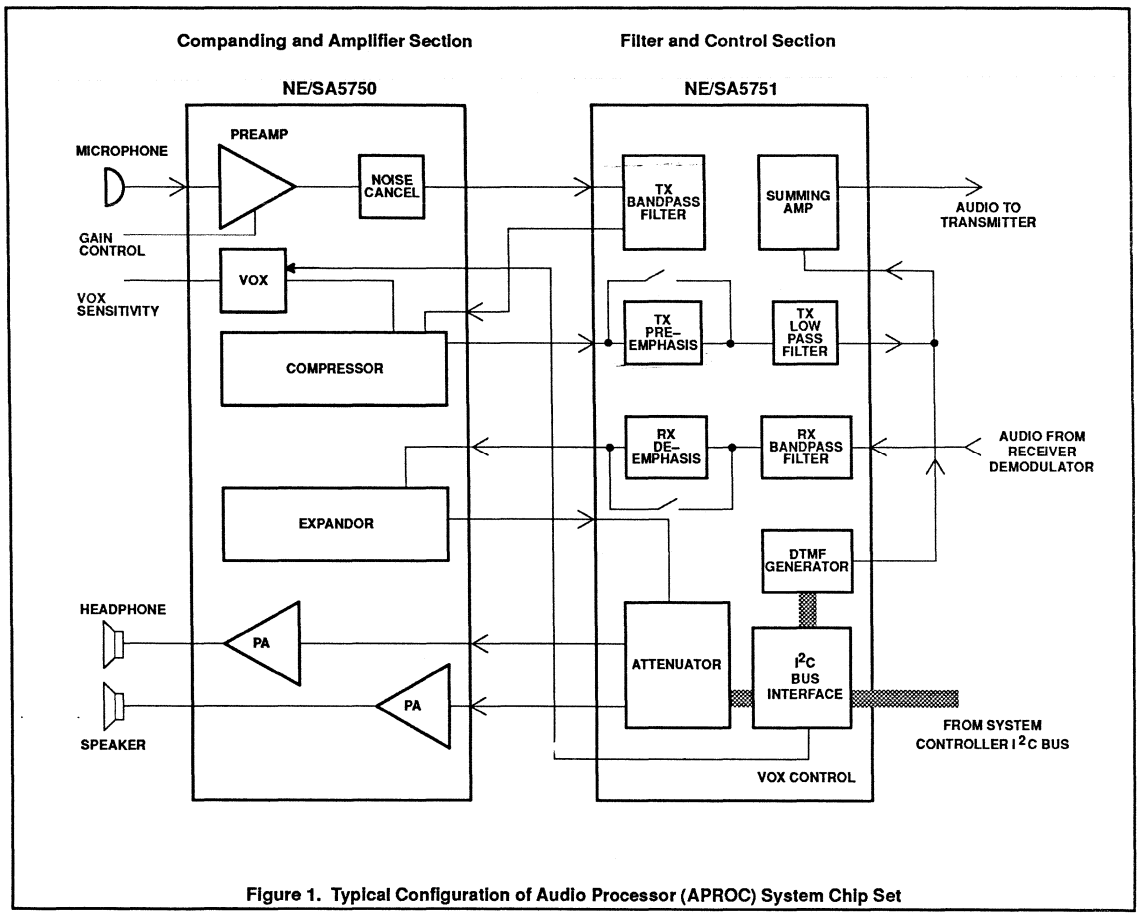


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

Audio processor – companding and amplifier section NE/SA5750

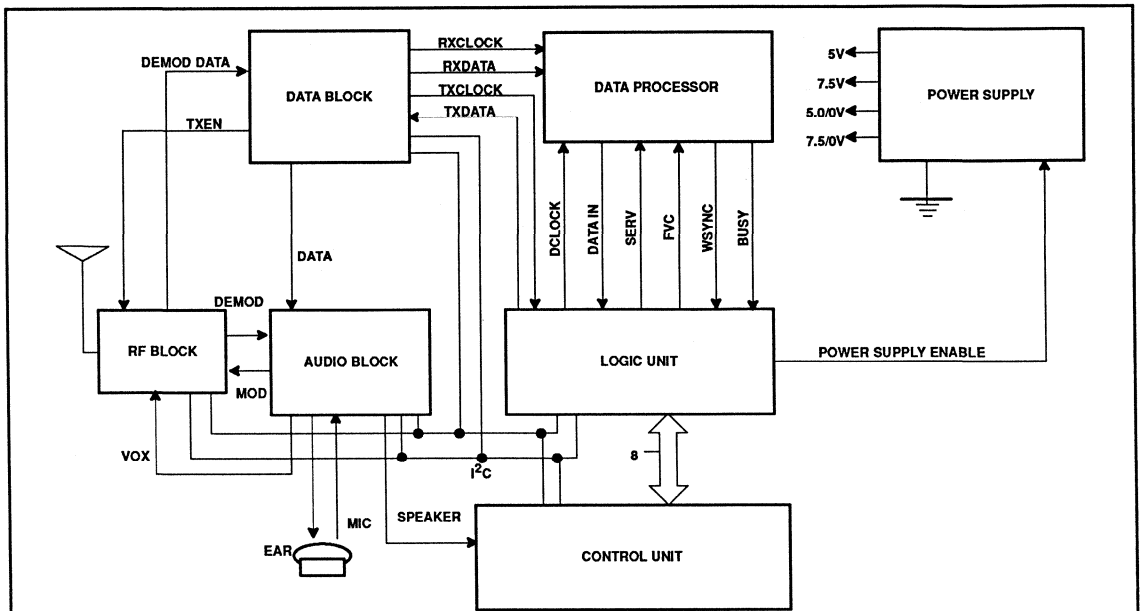


Figure 2. Cellular Radio System

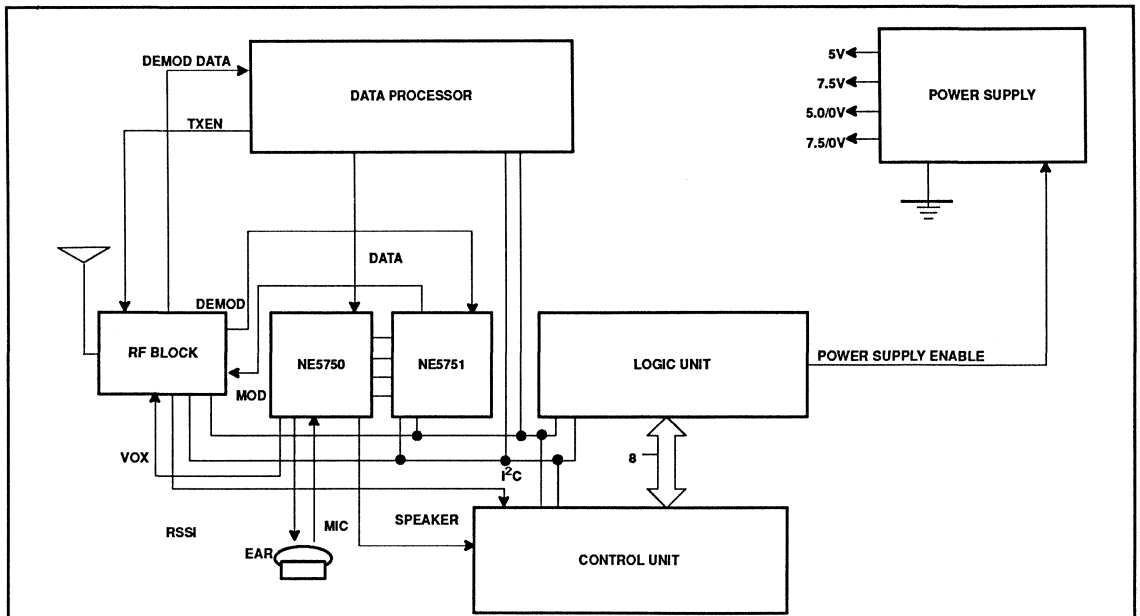


Figure 3. APROC Application Diagram

Audio processor – companding and amplifier section NE/SA5750

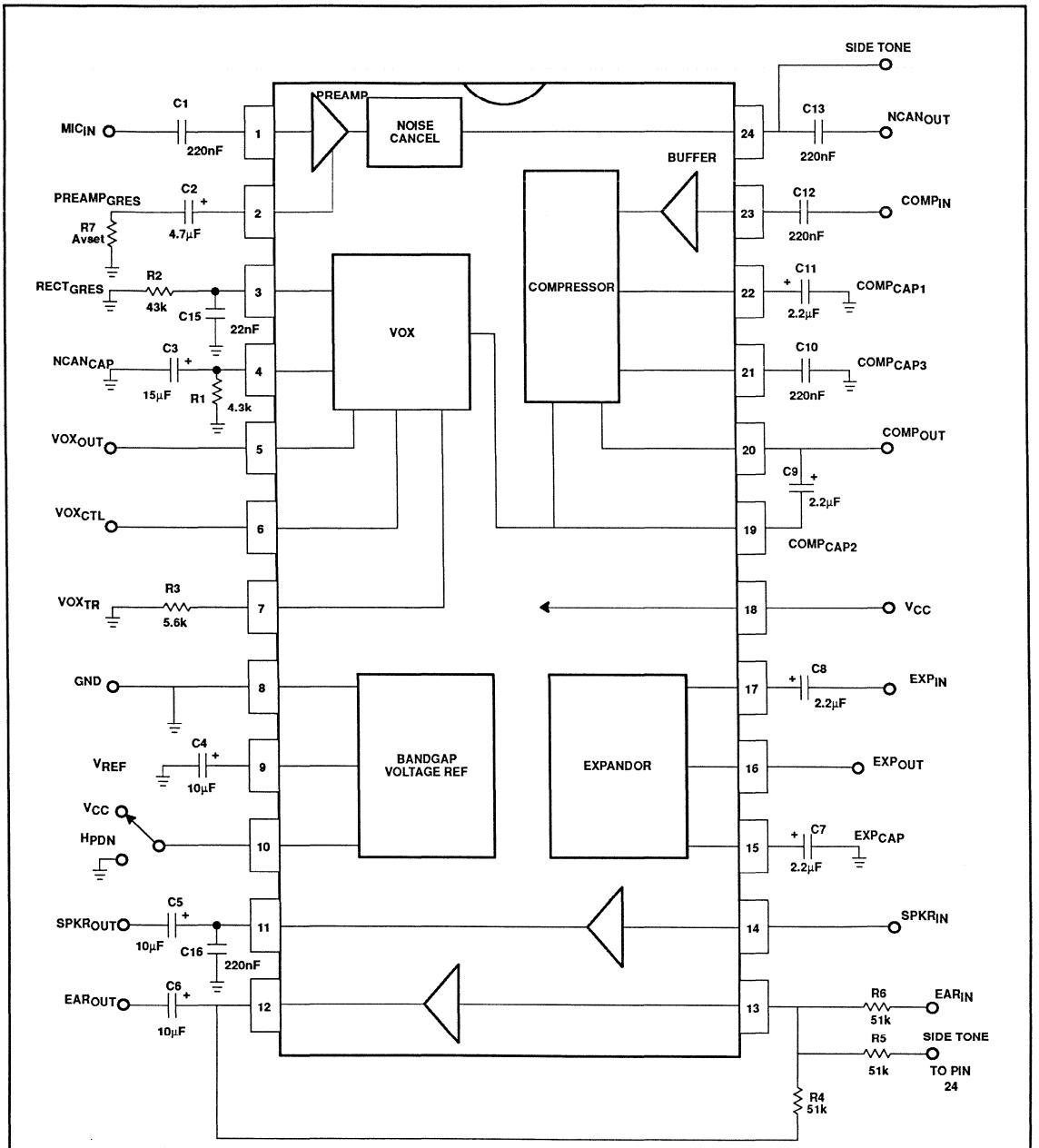


Figure 4. NE/SA5750 Test and Application Circuit

Philips Components

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Status	Product Specification
RF Communications	

NE/SA5751

Audio processor – filter and control section

special components for cellular radio

DESCRIPTION

The NE/SA5751 is a high performance low power CMOS audio signal processing system. The NE/SA5751 subsystems include complementary transmit/receive voice band (300–3000Hz), switched capacitor bandpass filters with pre-emphasis and de-emphasis respectively, a transmit low pass filter, peak deviation limiter for transmit, a digitally controlled volume control with 30dB range (in 2dB steps), audio path mute switches, a programmable DTMF generator, power-down circuitry for low current standby, power-on reset capability, and an I^2C interface. When the SA5751 is used with an SA5750 (companding function), the complete audio processing system of an AMPs or TACs cellular telephone is easily implemented.

FEATURES

- Low power
- High performance
- 5V supply
- Built-in programmable DTMF generator
- Built-in digitally controlled volume control
- Built-in peak-deviation limit
- I^2C Bus controlled
- Power-on reset
- Power-down capability

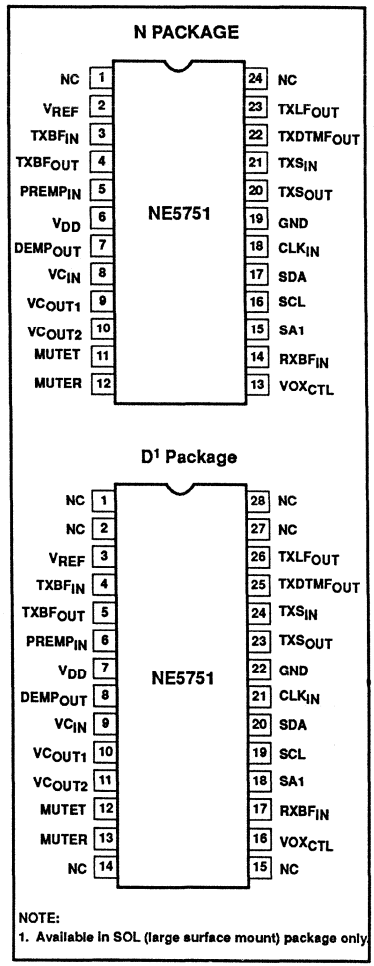
BENEFITS

- Very compact application
- Long battery life in portable equipment
- Complete cellular audio function with the SA5750

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION



NOTE:
1. Available in SOL (large surface mount) package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	0 to +70°C	NE5751N
28-Pin Plastic SOL	0 to +70°C	NE5751D
24-Pin Plastic DIP	–40 to +85°C	SA5751N
28-Pin Plastic SOL	–40 to +85°C	SA5751D

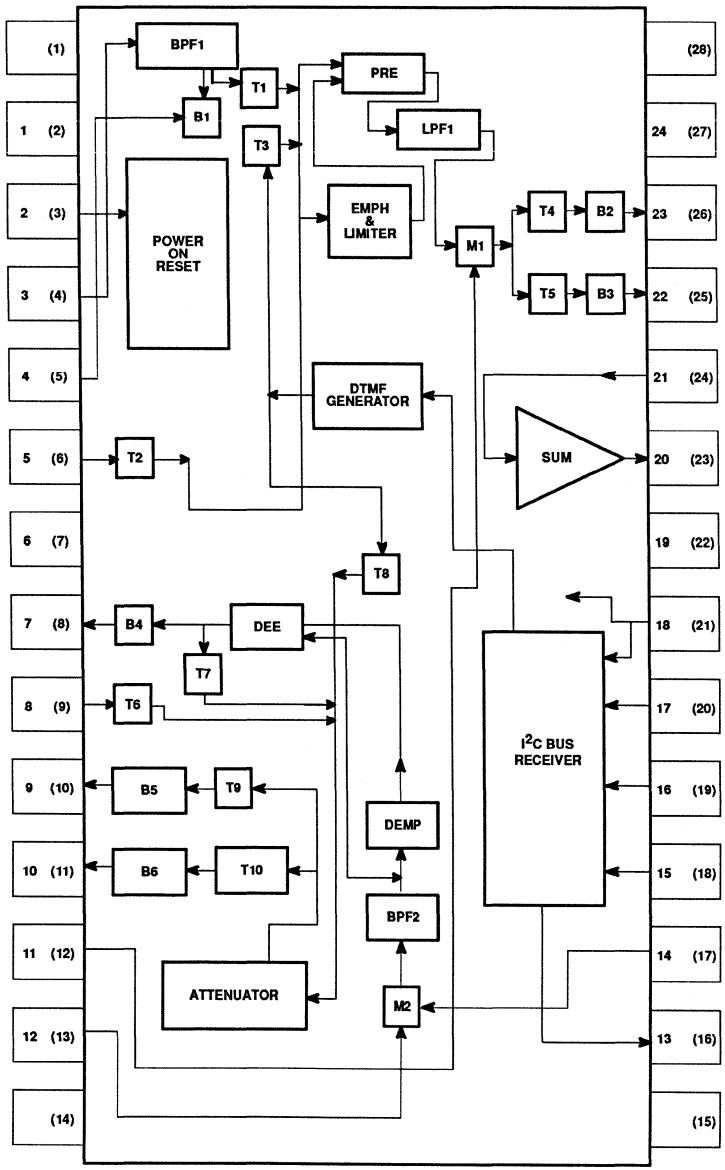
PIN DESCRIPTIONS

PIN NO.		SYMBOL	DESCRIPTION
	(1)	NC	Not connected
1	(2)	NC	Not connected
2	(3)	V_{REF}	Reference voltage
3	(4)	$TXBF_{IN}$	Transmit bandpass filter input
4	(5)	$TXBF_{OUT}$	Transmit bandpass filter output
5	(6)	$PREMP_{IN}$	Pre–emphasis input
6	(7)	V_{DD}	Positive supply
7	(8)	$DEMP_{OUT}$	De–emphasis output
8	(9)	VC_{IN}	Volume control input
9	(10)	VC_{OUT1}	Volume control output 1
10	(11)	VC_{OUT2}	Volume control output 2
11	(12)	MUTET	TX analog voice path mute input
12	(13)	MUTER	RX analog voice path mute input
	(14)	NC	Not connected
	(15)	NC	Not connected
13	(16)	VOX_{CTL}	Vox control output
14	(17)	$RXBF_{IN}$	Receive bandpass filter input
15	(18)	SA1	Serial bus address
16	(19)	SCL	Serial clock line
17	(20)	SDA	Serial data line
18	(21)	CLK_{IN}	Clock input
19	(22)	GND	Ground
20	(23)	TXS_{OUT}	Transmit summer output
21	(24)	TXS_{IN}	Transmit summer input
22	(25)	$TXDTMF_{OUT}$	Transmit DTMF output
23	(26)	$TXLF_{OUT}$	Transmit low–pass filter output
24	(27)	NC	Not connected
	(28)	NC	Not connected

NOTE:
1. Callouts are for N package; those in parentheses are for the D (SOL) package.

Audio processor – filter and control section NE/SA5751

BLOCK DIAGRAM



NOTES:
1. T1 to T10 represent the signal path switches.
2. M1 and M2 represent the mute switches.
3. PRE and DEE represent the bypass switches for pre–emphasis and de–emphasis, respectively.
4. B1 to B6 represent the output buffers.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Power supply voltage[1]	6	V
T_{STG}	Storage temperature	–65 to +150	°C
T_A	Ambient operating temperature NE5751	0 to 70	°C
	SA5751	–40 to +85	°C

NOTE:
1. Voltage applied to any pin –0.3 to V_{DD} +0.3V

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V, unless otherwise specified. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	Power supply voltage range		4.75	5.0	5.25	V
I_{DD}	Supply current	Operating Standby		2.7 0.9	5.0 2.0	mA mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V. See test circuit, Figure 4. Clock frequency = 1.2MHz; test level = 0dBV = 77.5mV_{RMS} = –20dBm, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	RX BPF anti alias rejection			40		dB
	RX BPF input impedance	f= 1kHz		500		kΩ
	RX BPF gain with de–emphasis	f = 1kHz	–0.5	0	0.5	dB
	RX BPF gain with de–emphasis	f = 100Hz		–31	–29	dBm0
	RX BPF gain with de–emphasis	f = 300Hz	9.0	9.6	11.0	dBm0
	RX BPF gain with de–emphasis	f = 3kHz	–11.0	–10.0	–9.0	dBm0
	RX BPF gain with de–emphasis	f = 5.9kHz		–68	–50	dBm0
	RX BPF noise with de–emphasis	300Hz–3kHz		170		μV_{RMS}
	RX dynamic range	with deemphasis		80		dB
	$DEMP_{OUT}$ output impedance	f = 1kHz		40		Ω
	$DEMP_{OUT}$ output swing (1%)	2.3kΩ to V_{REF}; f = 1kHz	V_{DD} –3	3.5		V_{P-P}
	VC_{OUT1} ouput swing (1%)	50kΩ toV_{REF}; f = 1kHz	V_{DD} –1	4.5		V_{P-P}
	VC_{OUT2} output swing (1%)	50kΩ to V_{REF}; f = 1kHz	V_{DD} –1	4.5		V_{P-P}
	VC_{OUT1} noise	VC_{IN} grounded C – message		25		μV_{RMS}
	VC_{OUT2} noise	VC_{IN} grounded C – message		25		μV_{RMS}
	Mute threshold off		0		0.8	V
	Mute threshold on		2.0		5.0	V
	CLK1, 2 high		4.0		5.0	V
	CLK1, 2 low		0		1.0	V
	TX BPF anti alias rejection			40		dB
	TX BPF input impedance	f = 3kHz		500		KΩ

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	TX BPF noise	300 – 3000kHz		90		μV_{RMS}
	TX LPF gain	f = 5.9kHz		–39	–36	dB
	TX LPF gain with pre–emphasis	f = 1kHz, 20dBV		12.06		dB
	TX LPF gain with pre–emphasis	f = 100Hz		–19		dBm0
	TX LPF gain with pre–emphasis	f = 300Hz		–10.45		dBm0
	TX LPF gain with pre–emphasis	f = 3kHz		9.14		dBm0
	TX LPF gain with pre–emphasis	f = 5900Hz		–39		dBm0
	TX LPF gain with pre–emphasis	f = 9kHz		–51		dBm0
	TX overall gain	1kHz	11.3	11.8	12.5	dB
	TX overall gain	100Hz		–47	–45	dBm0
	TX overall gain	300Hz	–11	–10.4	–9	dBm0
	TX overall gain	3kHz	8	9	9.6	dBm0
	TX overall gain	5.9kHz		–52	–45	dBm0
	TX BPF output impedance	f = 1kHz		360		Ω
	TX BPF output swing (1%THD)	50kΩ to V_{REF} f = 1kHz		4.5		V_{P-P}
	TX BPF dynamic range			90		dB
	$PREMP_{IN}$ input impedance	f = 3kHz		500		kΩ
	Summing op amp					
	Slew rate	C_L = 15pF		0.75		V/μs
	Output impedance	Unity gain; f = 3kHz		40		Ω
	Output swing (1% THD)	1kHz, 5kΩ load (25°C)		4.3		V_{P-P}
	Volume control accuracy	–30dB to 0dB	–1	0	+1	dB
	Analog switches					
	Insertion loss			60		dB
	On time transition	MUTET, MUTER 0.8V –>2.0V		3		μs
	Off time transition	MUTET, MUTER 2.0V –>0.8V		0.25		μs

I²C CHARACTERISTICS

The I²C bus is for 2–way, 2–line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull–up resistor. When the bus is free, both lines are high. Data transfer may be initiated only when the bus is not busy.

The output devices, or stages, connected to the bus must have an open drain or open collector output in order to perform the wired–AND function.

Data at the I²C bus can be transferred at a rate up to 100kbits/s. The number of devices connected to the bus is solely dependent on the maximum allowed bus capacitance of 400pF.

Due to the variety of different devices which can be connected to the I²C bus, the levels of the logical "0" and "1" are not fixed and depend on the appropriate level of V_{DD}. For the typical supply voltage of 5V which is chosen here, logical "1" and logical "0" are, however, fixed respectively on maximum input LOW voltage, 1.5V and minimum input HIGH voltage, 3.0V.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock's cycle. If it does not remain HIGH, it may be interrupted as a control signal.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH to LOW transition of the data line while the clock line is HIGH is defined as a start condition S. A LOW to HIGH transition of the data line while the clock is HIGH is defined as a stop condition.

SYSTEM CONFIGURATIONS

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master"; and devices which are controlled by the master are the "slaves".

ACKNOWLEDGE

The number of data bytes transferred between the start and the stop condition from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set up and hold times must be taken into account.

I²C BUS DATA CONFIGURATIONS

The NE5751 is always a slave receiver in the I²C bus configuration (R/W bit–0). The slave address consists of seven bits in the serial mode where the least significant bit is selectable by hardware on input A0 and the other more significant bits are internally fixed.

POWER ON RESET

In order to avoid undefined states of the NE5751 when the power is switched on, a power on reset is supplied. The reset is active when Pin V_{REF} is held below 0.8V. The reset is off when Pin V_{REF} is above 2.0V. Pin V_{REF} is normally at 2.5V generated by a resistive divider from V_{DD}. Nominal impedance is 20kΩ. In a typical application a capacitor is connected to Pin V_{REF} to improve power supply rejection. The time delay of the network resets the internal registers when power is first applied. The signal paths are off in the reset condition. The NE5751 must be programmed via the I²C bus for normal operation. The Power Down mode is defined only when all register values are zero.

CONTROL REGISTERS

Register Map

The address register is as follows:

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	SA1	0

SA1 is controlled by serial bus address pin.

Signal Path Register

MSB							LSB
T10	T9	T8	T6	VOX_{EN}	T4	T3T5	T2

T2 is the transmission gate between Pin $PREEMP_{IN}$ and the emphasis input.

T3T5 connects the output of the DTMF generator to the emphasis input and connects the output of the XMT LPF to Pin $TXDTMF_{OUT}$.

T4 connects the output of the XMT LPF to Pin $TXLF_{OUT}$.

VOX_{EN} enables the VOX function of NE5750.

T6 connects Pin VC_{IN} to the volume control.

T8 connects the output of the DTMF generator to the volume control.

T9 enables VC_{OUT1}.

T10 enables VC_{OUT2}.

Volume Control and Test Register

MSB							LSB
PDW	T1T7	DEE	PRE	V1	V2	V3	V4

V4 is volume control bit 4. This is the MSB. A zero is 16dB attenuation.

V3 is volume control bit 3. A zero is 8dB attenuation.

V2 is volume control bit 2. A zero is 4dB attenuation.

V1 is volume control bit 1. A zero is 2dB attenuation.

PRE is the bypass for the pre–emphasis.

DEE is the bypass for the de–emphasis.

T1T7 is the bypass for the compressor and expandor.

PDW is the control for power down mode.

This mode is defined only when all register values are reset to zero.

High Tone DTMF Register

MSB							LSB
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

The eight bits determine the output frequency by the following formula.:

High Frequency = 1200kHz/6/HD
where HD is the value of the register.

Low Tone DTMF Register

MSB							LSB
LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0

The eight bits determine the output frequency by the following formula.:

Low Frequency = 1200kHz/12/LD
where LD is the value of the register.

The operation of the 96ms DTMF timer is initiated by the loading of the low tone DTMF register. This timer terminates transmission of the tones as the generated tones cross the reference level after 96ms. The on time of the tones can thus vary by up to one cycle of the tones.

Continuous tones can be obtained by again loading the two DTMF registers before 96ms have elapsed.

Single tones can be obtained by loading 0, 1 or 2 into one of the registers to silence it.

Phase continuous frequency modulation can be produced by loading a new value into a DTMF register during operation.

Audio processor – filter and control section NE/SA5751

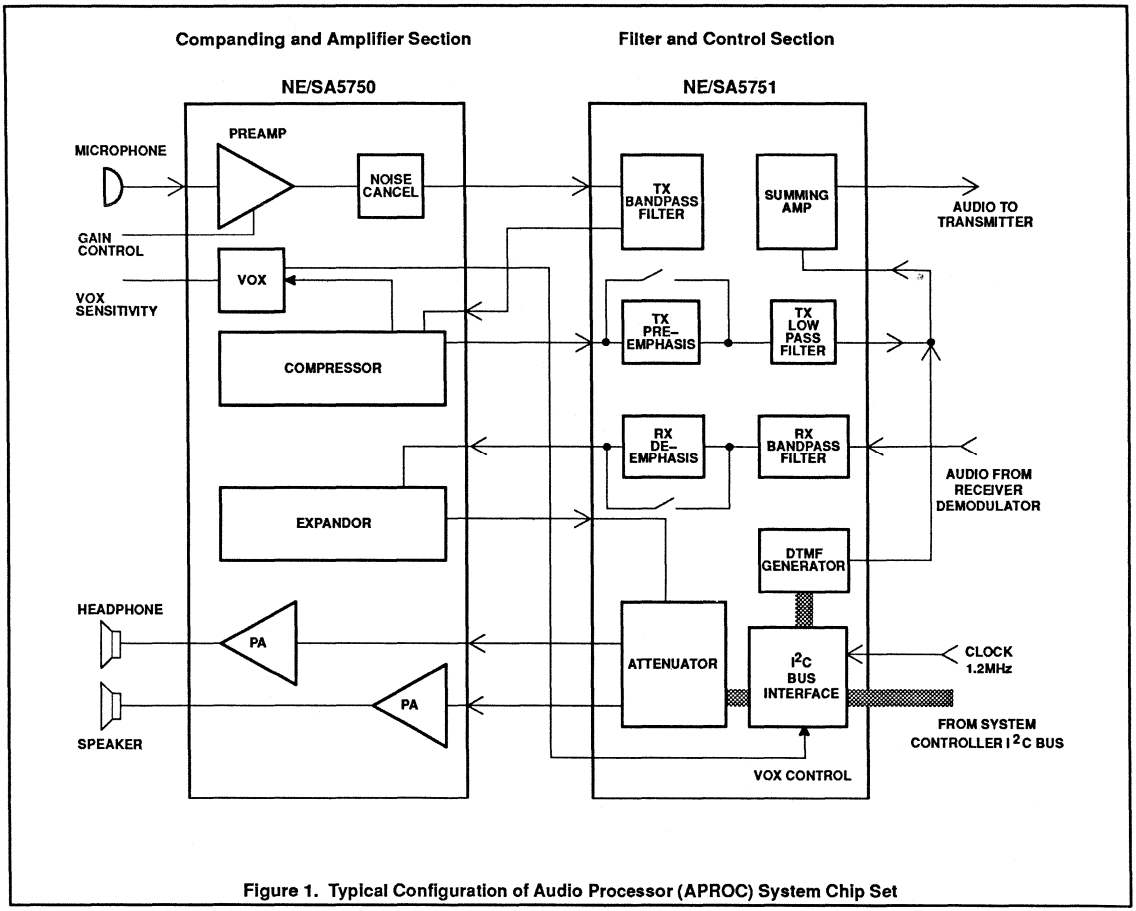


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

Audio processor – filter and control section NE/SA5751

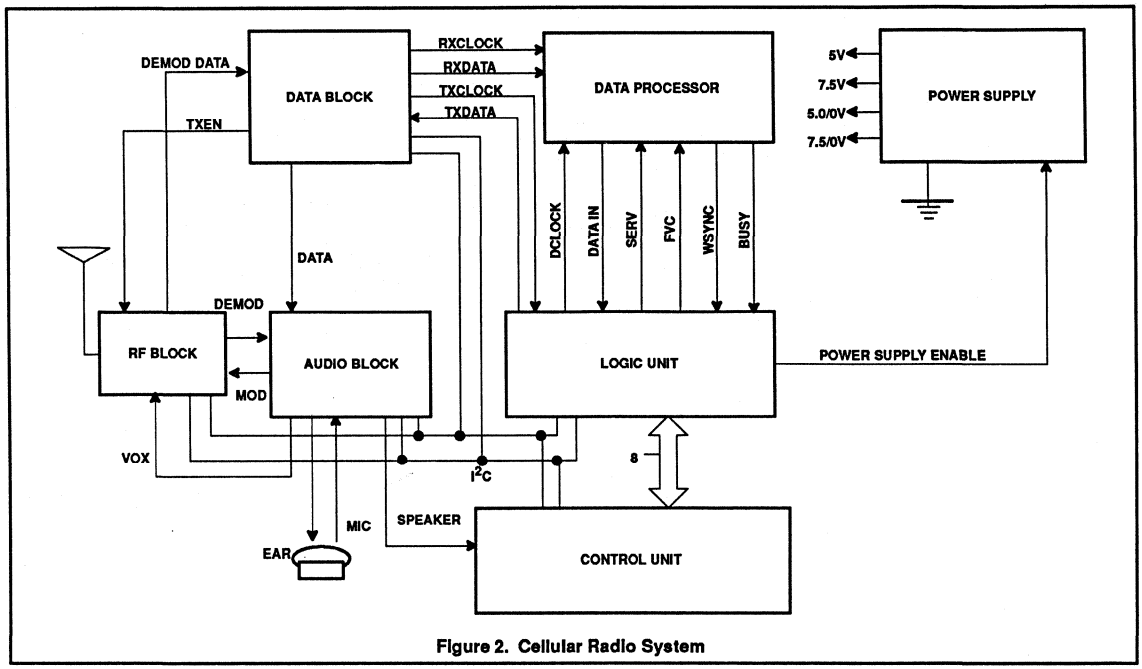


Figure 2. Cellular Radio System

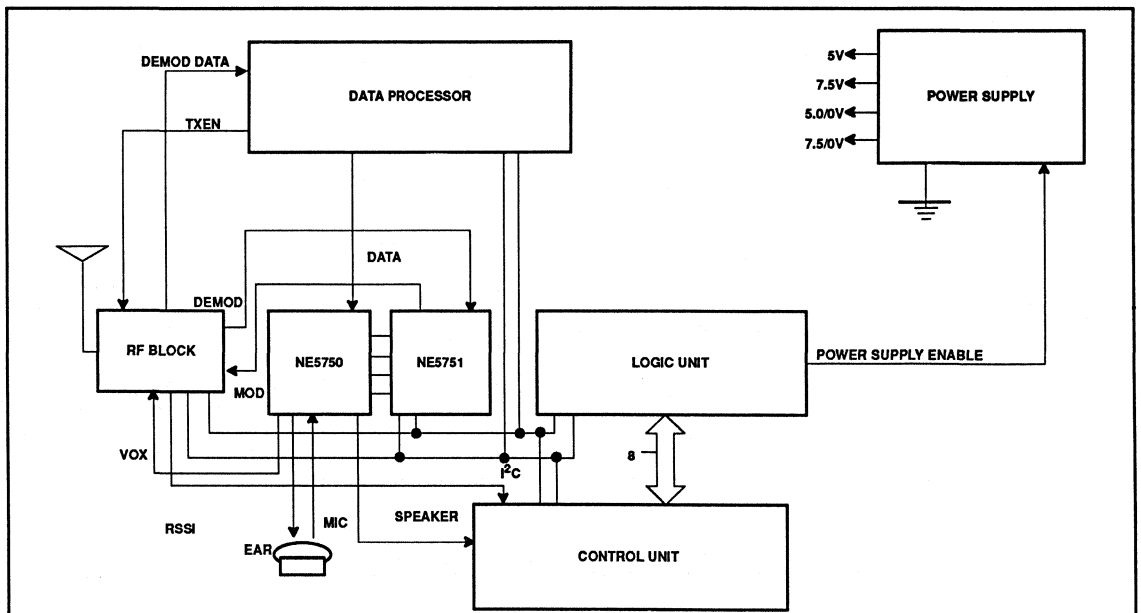


Figure 3. APROC Application Diagram

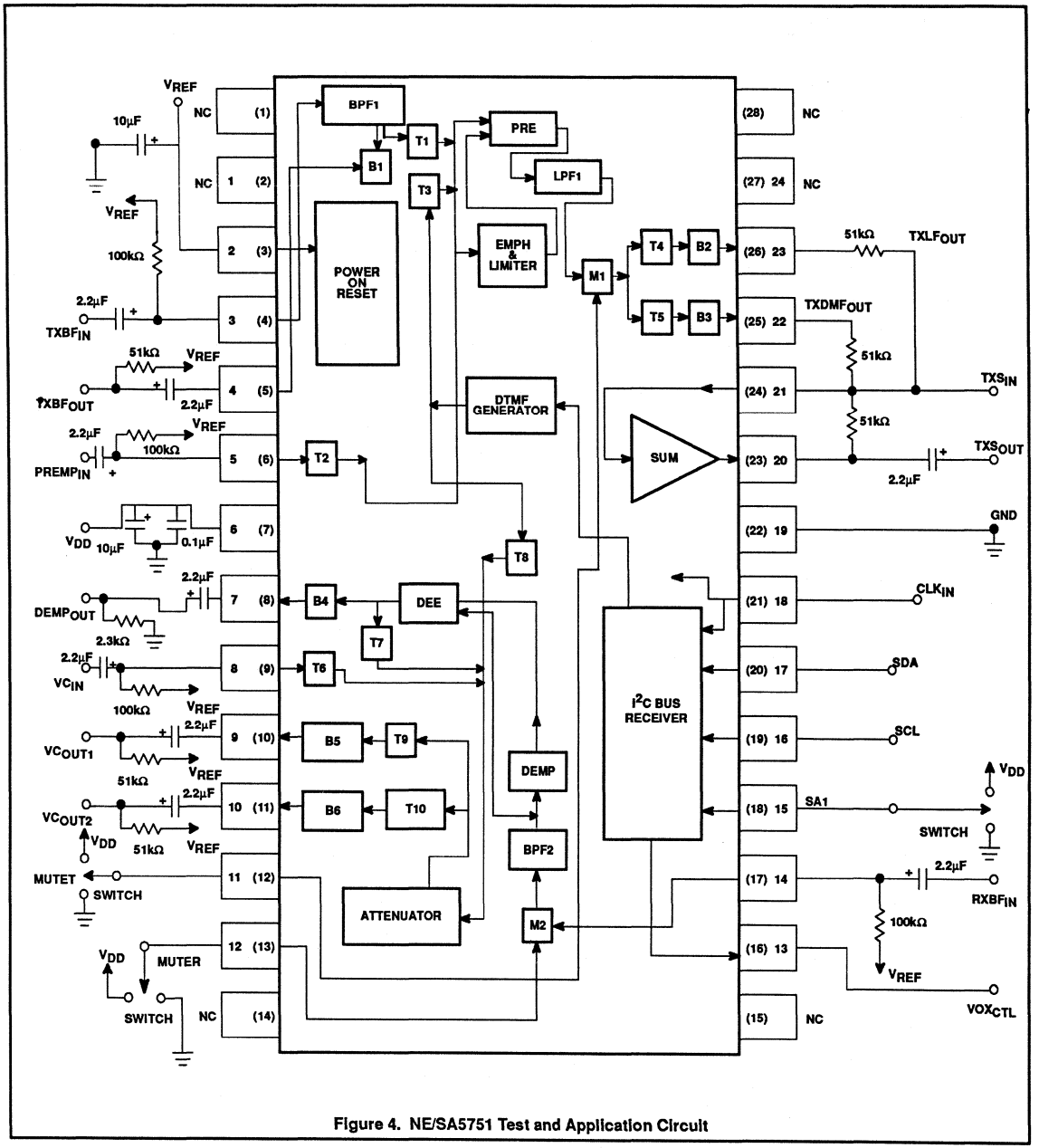
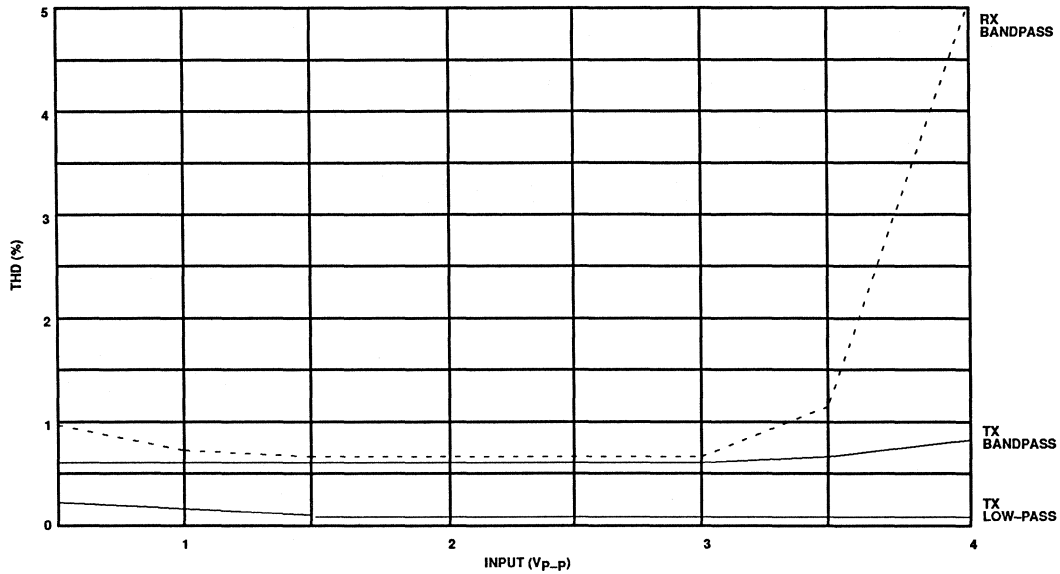


Figure 4. NE/SA5751 Test and Application Circuit

PERFORMANCE CHARACTERISTIC

THD (%) vs INPUT SIGNAL VOLTAGE (1kHz)
FOR THE RX BANDPASS, TX BANDPASS, AND TX LOW–PASS FILTERS



NE5900
Call Progress Decoder

Product Specification

DESCRIPTION

The NE5900 call progress decoder (CPD) is a low cost, low power CMOS integrated circuit designed to interface with a microprocessor-controlled smart telephone capable of making preprogrammed telephone calls. The call progress decoder provides information to permit microprocessor decisions whether to initiate, continue, or terminate calls. A tri-state, 3-bit output code indicates the presence of dial tone, audible ringback, busy signal, or reorder tones.

A front-end bandpass filter is accomplished with switched capacitors. The bandshaped signal is detected and the cadence is measured prior to output decoding. In addition to the three data bits, a buffered bandpass output and envelope output are available. All logic inputs and outputs can interface with LSTTL, CMOS, and NMOS.

Circuit features include low power consumption and easy application. Few and inexpensive external components are required. A typical application requires a 3.58MHz crystal or clock, 470kΩ resistor, and two bypass capacitors. The NE5900 is effective where traditional call progress tones, PBX tones, and precision call progress tones must be correctly interpreted with a single circuit.

FEATURES

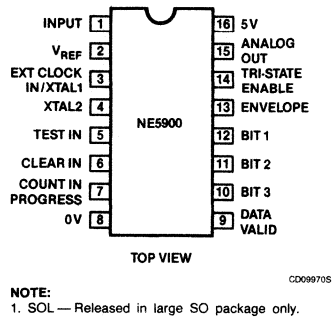
- **Fully decoded tri-state call progress status output**
- **Works with traditional, precision, or PBX call progress tones**
- **Low power consumption**
- **Low cost 3.58MHz crystal or clock**
- **No calibration or adjustment**
- **Interfaces with LSTTL, CMOS, NMOS**
- **Easy application**

APPLICATIONS

- **Modems**
- **PBXs**
- **Security equipment**
- **Auto dialers**
- **Answering machines**
- **Remote diagnostics**
- **Pay telephones**

PIN CONFIGURATION

D[1] and N Packages

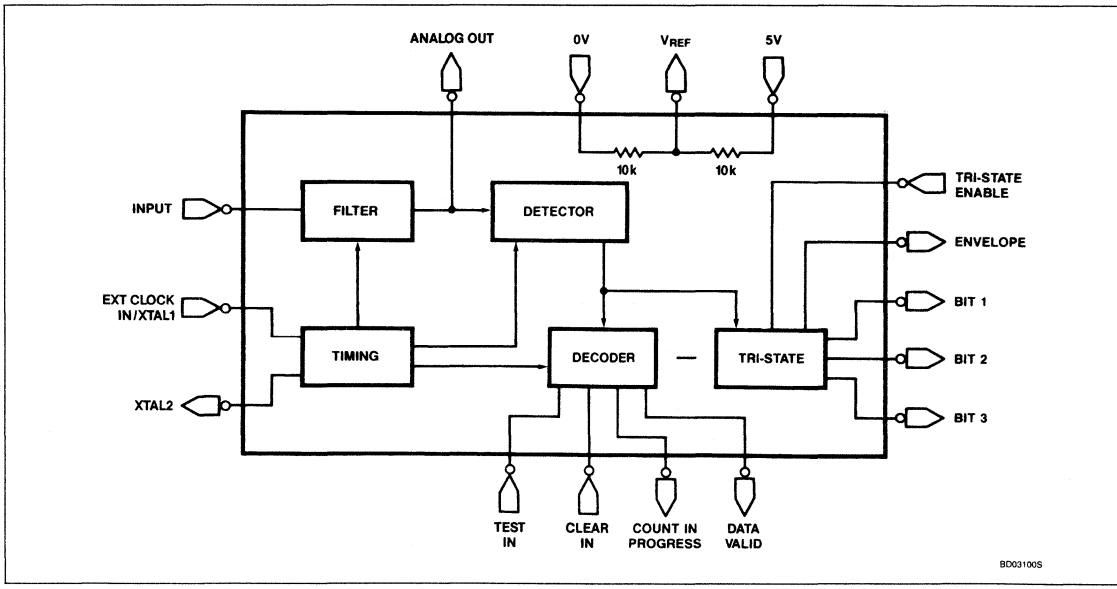


TOP VIEW

CD09970S

NOTE:
1. SOL — Released in large SO package only.

BLOCK DIAGRAM CPD



ORDERING INFORMATION

DESCRIPTION	AMBIENT TEMPERATURE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE5900D
16-Pin Plastic DIP	0 to +70°C	NE5900N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Power supply voltage	9	V
V_{IN}	Logic control input voltages	−0.3 to +16	V
V_{IN}	All other input voltages[1]	−0.3 to V_{CC} +0.3	V
V_{OUT}	Output voltages	−0.3 to V_{CC} +0.3	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating temperature range	0 to +70	°C
T_{SOLD}	Lead soldering temperature (10s)	+300	°C
T_J	Junction temperature	+150	°C

NOTE:
1. Includes Pin 3 — Ext Clock In

DC ELECTRICAL CHARACTERISTICS Unless otherwise stated, V_{DD} = +5.0V; Pin 3 f_{OSC} = 3.58MHz; Ambient Temperature = 0 to +70°C. Pin 5 = 0V, Pin 14 = V_{DD}.

SYMBOL	PARAMETER	TEST CONDITONS	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Power supply voltage	Pin 16 Pin 14 = V_{DD} Pins 5, 6 = 0V	4.5	5.0	5.5	V
	Quiescent current	As above with no output loads.		2.0	4.0	mA
	Input threshold	Pin 1 level, frequency = 460Hz, V_{DC} = V_{REF} Output Pin 13 = V_{DD}		-39	-35	dB[1]
	Signal rejection	Pin 1 level, 300Hz frequency, V_{DC}=V_{REF} Output Pin 13 = 0V			-50	dB[1]
	Low frequency[2] rejection	Pin 1 frequency, 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V			180	Hz
	High frequency[2] rejection	Pin 1 frequency 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V	800			Hz
V_{IH}	Logic 1 input voltage	Pins 6, 14	2.0		15	V
V_{IL}	Logic 0 input voltage	Pins 6, 14	0		0.8	V
I_{HL}	Logic 1 input current	Pins 3, 6, 14 = V_{DD}	-1.0		1.0	μA
I_{IL}	Logic 0 input current	Pins 3, 6, 14 = 0V	-1.0		1.0	μA
V_{IH}	Logic 1 input voltage	Pin 3 External Clock In/XTAL	V_{DD} - 1		V_{DD}	V
V_{IL}	Logic 0 input voltage	Pin 3 External Clock In/XTAL	0		1.0	V
V_{OL}	Logic 0 output voltage	I_{SINK} = 1.6mA Pins 7, 9, 10, 11, 12, 13	0		0.4	V
V_{OH}	Logic 1 output voltage	I_{SOURCE} = 0.5mA Pins 7, 9, 10, 11, 12, 13	V_{DD} - 0.4		V_{DD}	V
I_{OZ}	Tri-state leakage	V_{OUT} = V_{DD} or 0V Pins 10, 11, 12, 13 Pin 14 = 0V	-3.0		3.0	μA
	Filter output gain	Input Pin 1, 460Hz - 20dB, V_{DC} = V_{REF} Output Pin 15, R_{LOAD} = 1MΩ	6.5	8.5	10.5	dB
	Filter frequency response	As above from 300Hz to 630Hz, referenced to 460Hz	-1.0		1.0	dBmo
	Input impedance[2]	Pin 1, frequency = 460Hz	1			MΩ
V_{REF}	Reference voltage	Pin 2, V_{DD} = 5V	2.4	2.5	2.6	V
R_{REF}	Reference resistance	Pin 2		5		Ω
	Envelope response time	Time from removal or application of 460Hz - 20dB (V_{DC} = V_{REF} on Pin 1) to response of Pin 13		38		ms

NOTES:
1. 0dB = 0.775V_{RMS}.
2. By design; not tested.

Call Progress Decoder

NE5900

The NE5900 uses the signal in the call progress tone passband and the cadence or interrupt rate of the signal to determine which call progress tone is present.

Figure 1 shows a detailed block diagram of the NE5900.

The signal input from the phone line is coupled through a 470kΩ resistor which, together with two internal capacitors and an internal resistor, form an anti-aliasing filter. This passive low pass filter strongly rejects AM radio interference. Insertion loss is typically 1.5dB at 460Hz. The 470kΩ resistor also provides protection from line transients. The input (Pin 1) DC voltage can be derived from V_{REF} (Pin 2) or allowed to self-bias through a series coupling capacitor (10nF minimum).

Following this is a switched capacitor bandpass filter which accepts call progress tones and inhibits tones not in the call progress band of 300Hz to 630Hz. The bandpass limits are determined by the input clock frequency of 3.58MHz. An on-board inverter between Pins 3 and 4 can be used either as a crystal oscillator or as a buffer for an external 3.58MHz clock signal. The switched capacitor filters provide typical rejection of greater than 40dB for frequencies below 120Hz and above 1.6kHz.

The decoder responds to signals between 300Hz and 630Hz with a threshold of −39dB typical (0dB = 0.775V_{RMS}). The decoder will not respond to any signals below −50dB or to tones up to 0dB which are below 180Hz or above 800Hz. Dropouts of 20ms or bursts of only 20ms duration are ignored. A gap of 40ms or a valid tone of 40ms is detected.

The buffered output of the switched capacitor filter is available at the analog output, Pin 15. A logic output representing the detected envelope of this signal is available at the envelope output, Pin 13.

At the start of an in-band tone (envelope output goes high), a 2.3-second interval is timed out. Transitions of the envelope during this interval are counted to determine the signal present. At 2.3 seconds, the three bits of data representing this decision are stored in the latch and appear at the outputs. A data valid signal goes high at this time, signaling that the data bits, Pins 10 − 12, can be read.

The output code is as follows:

	PIN 12	PIN 11	PIN 10
DIAL TONE	0	0	0
RINGING SIGNAL	1	0	0
BUSY SIGNAL	0	1	0
REORDER TONE	0	0	1
OVERFLOW	1	1	1

The overflow condition occurs in the event that too many transitions occur during the 2.3-second interval. This can result from noise, voice, or other line disturbances not normally present during the post-dialing interval. Note that the end of dial tone is interpreted as a valid ringing signal.

The clear input resets all internal registers and the output latch, and is to be set low after the completion of dialing. The clear input should be pulsed high for proper operation. Recommended pulse width is between 0.2μs and 20ms. If clear is held high when envelope is high, a false output pulse (Pin 13) can result when clear is returned low.

For applications where dialing is done by a person rather than by a microprocessor, an uncertainty exists about the number of digits to be dialed (local vs long distance). In such situations it is possible to clear the NE5900 by application of the DTMF signal or dial pulses to the clear pin (Pin 6). When dialing is complete, the device is cleared and ready to respond to the next call progress unit.

Enable is held at 5V to enable Pins 10, 11, 12, and 13. When enable is brought low, data valid is also set low. Enable must remain high while the data is being read. The test pin is for production test only and must be kept low in all user applications.

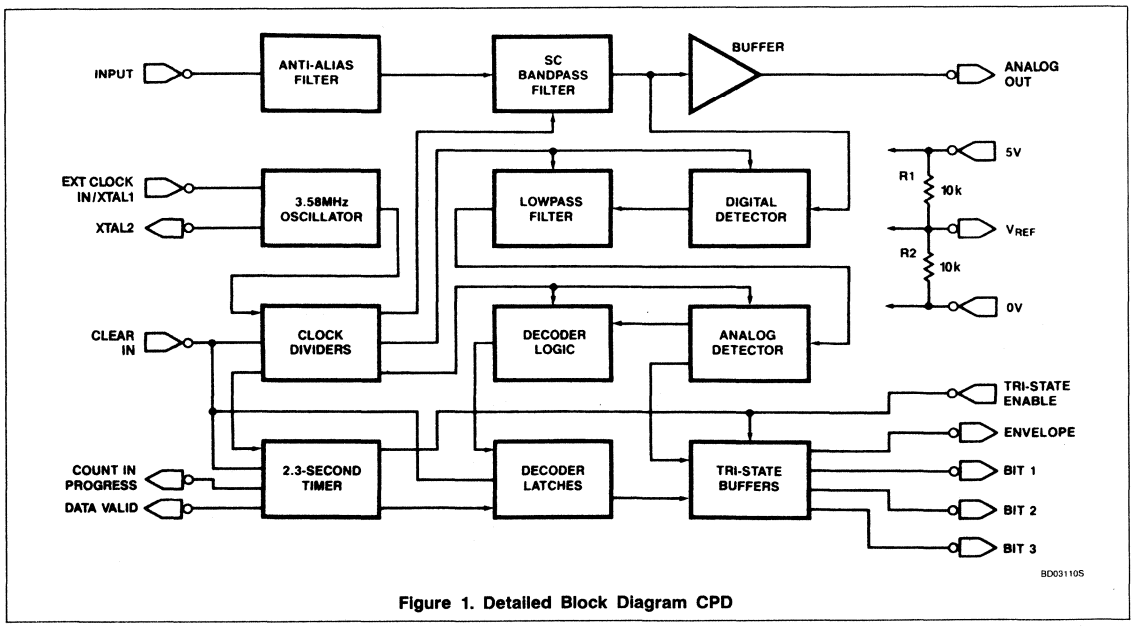


Figure 1. Detailed Block Diagram CPD

Call Progress Decoder

NE5900

Figure 2 shows a typical application of the call progress decoder.

In this application only one external component is needed and no microprocessor activity other than clear is required.

Figure 3 shows the recommended direct interface to the telephone line. Bus connection is possible by utilizing tri-state, and internal timing is accomplished with a 3.58MHz crystal.

The designer can utilize the input signal, clock, bus, or microprocessor interface which best serves the application. Figure 4 gives a typical timing diagram for the application of Figures 2 and 3.

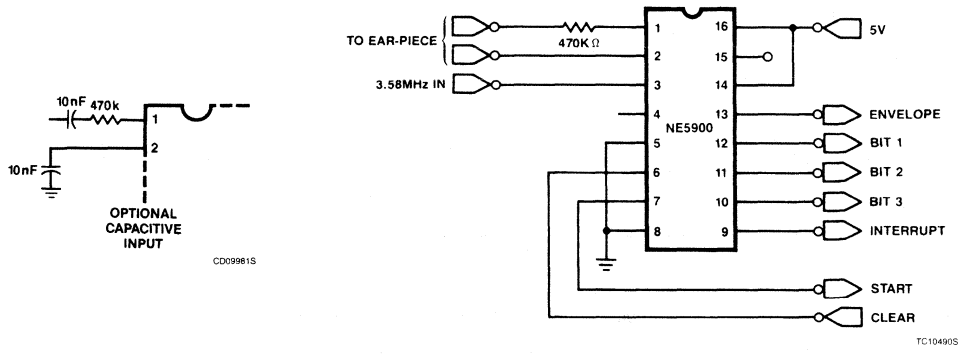


Figure 2. Typical Application

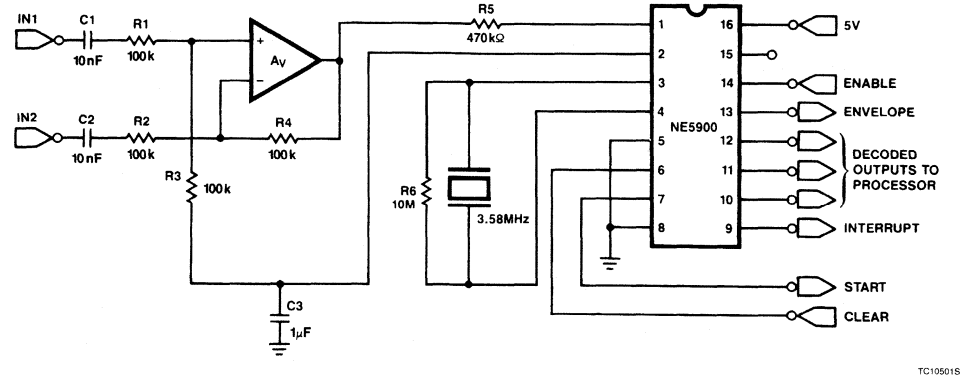


Figure 3. Typical Two-Wire Application

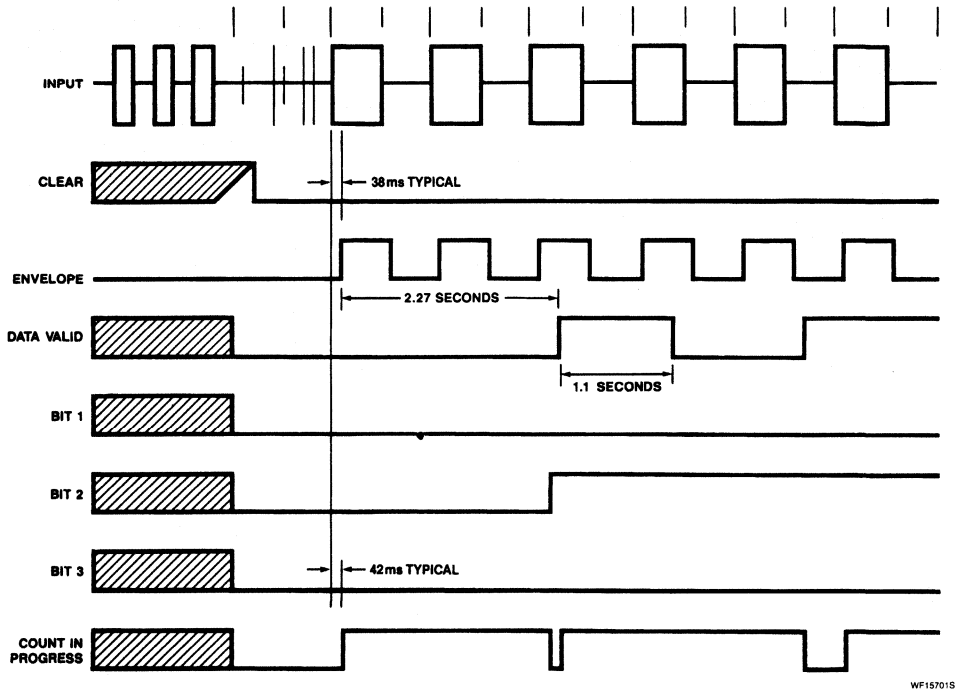
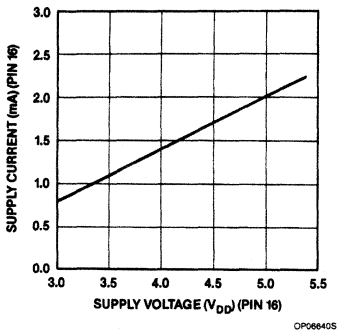

INPUT
CLEAR
38ms TYPICAL
ENVELOPE
2.27 SECONDS
DATA VALID
1.1 SECONDS
BIT 1
BIT 2
BIT 3
42ms TYPICAL
COUNT IN PROGRESS
WF15701S

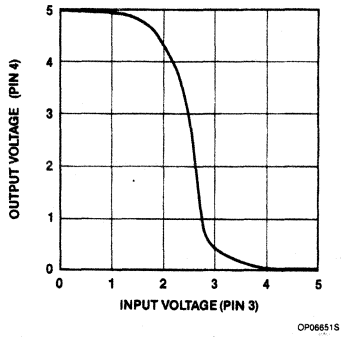
Figure 4

TYPICAL PERFORMANCE CHARACTERISTICS

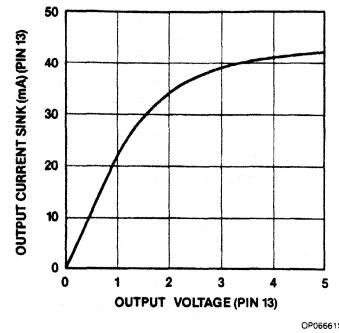
Power Supply Current vs V_{DD}



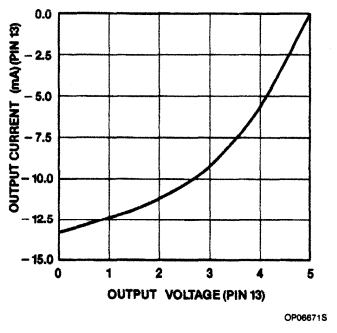
Voltage Transfer Curve



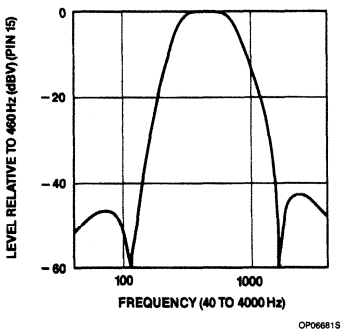
Output Voltage Current Curve Digital Output Low



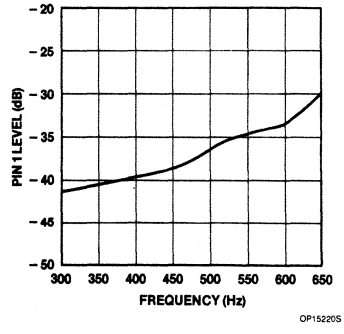
Output Voltage Current Curve Digital Output High



Filter Frequency Response



Typical Threshold



PULSE DIALLER WITH REDIAL

The OM1036C is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The OM1036C can regenerate access pauses during redial. During the original entry, access pauses are stored via the keyboard. A regenerated access pause can be terminated during redial in two ways: via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems.

The circuit has the following features:

- Operation from 2,0 V to 6 V supply.
- Static standby operation down to 1,5 V.
- Low current consumption; typ. 20 μA.
- Low static standby current; typ. 0,65 μA.
- Low-cost RC oscillator; 13,8 kHz.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz and 20 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; $>$ 160 ms (10 Hz dialling pulse frequency).
- Access pause generation via the keyboard.
- Access pause reset:
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE and RC1).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINE

OM1036CP: 18-lead DIL; plastic (SOT102G,N,PE).

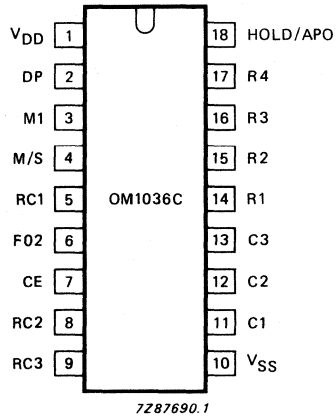


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

4	M/S	controls the mark-to-space ratio of the line pulses
6	F02	the dialling pulse frequency is defined by the logic state of this input
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	C1	column keyboard inputs with pull-up on chip
12	C2	
13	C3	
14	R1	row keyboard outputs with pull-down on chip
15	R2	
16	R3	
17	R4	

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence

Input/output

18	HOLD/APO	This pin will go HIGH when an access pause code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

5	RC1	input/output of the RC on-chip oscillator
8	RC2	
9	RC3	

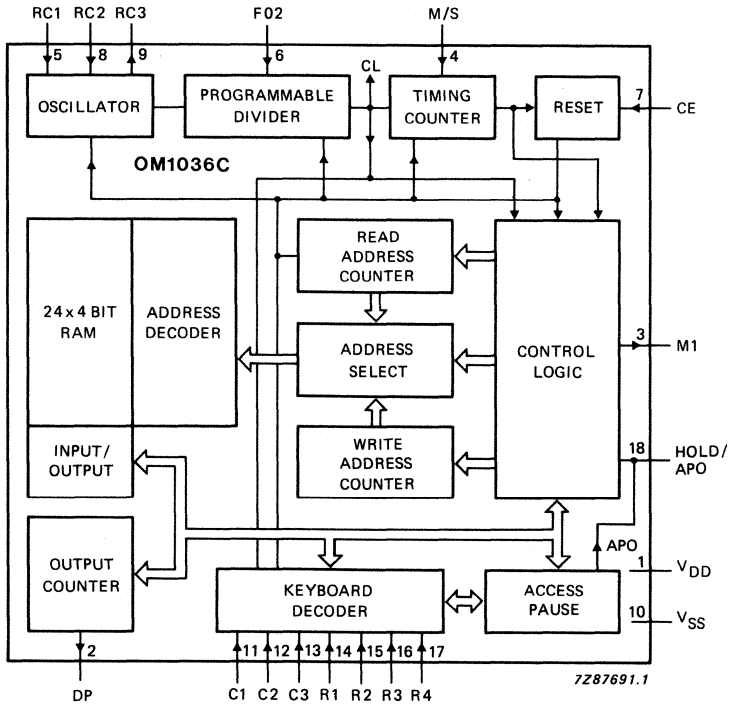


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (RC1, RC2, RC3)

The time base for the OM1036C is an RC controlled on-chip oscillator which is completed by connecting two resistors and a capacitor between the RC1, RC2 and RC3 pins (see Fig. 5). The oscillator is followed by a frequency divider of which the division ratio can be externally set (F02) to provide one of two chip system clocks (10 Hz or 20 Hz pulse frequencies).

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 6 and 7 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

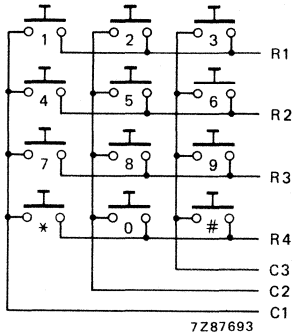
Debouncing keyboard entries (C1 to C3; R1 to R4)

The column keyboard inputs to the integrated circuits (C_n) and the row keyboard outputs (R_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig.3, or to a double contact keyboard with a common left open contact (see Fig.4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input. Any other input combinations are not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig.6. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for five or six clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been left open for four or five clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the leading edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the OM1036C. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

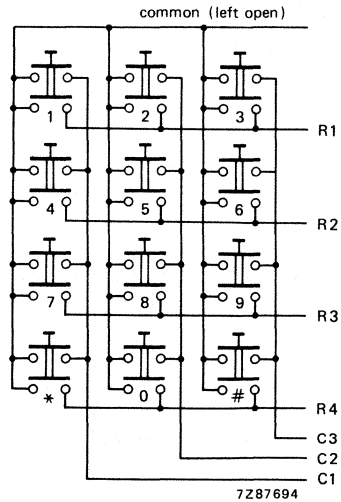


Fig. 4 Double contact keyboard.

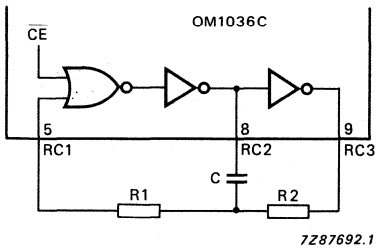


Fig. 5 Oscillator configuration.

$$f_{osc} \approx \frac{1}{2{,}7 \times R2 \times C} \text{ for } R1 \gg R2$$

with:

R1 = 560 kΩ
R2 = 220 kΩ
C = 120 pF
} f_{osc} = 13,8 kHz

C = ceramic capacitor (type NP0)

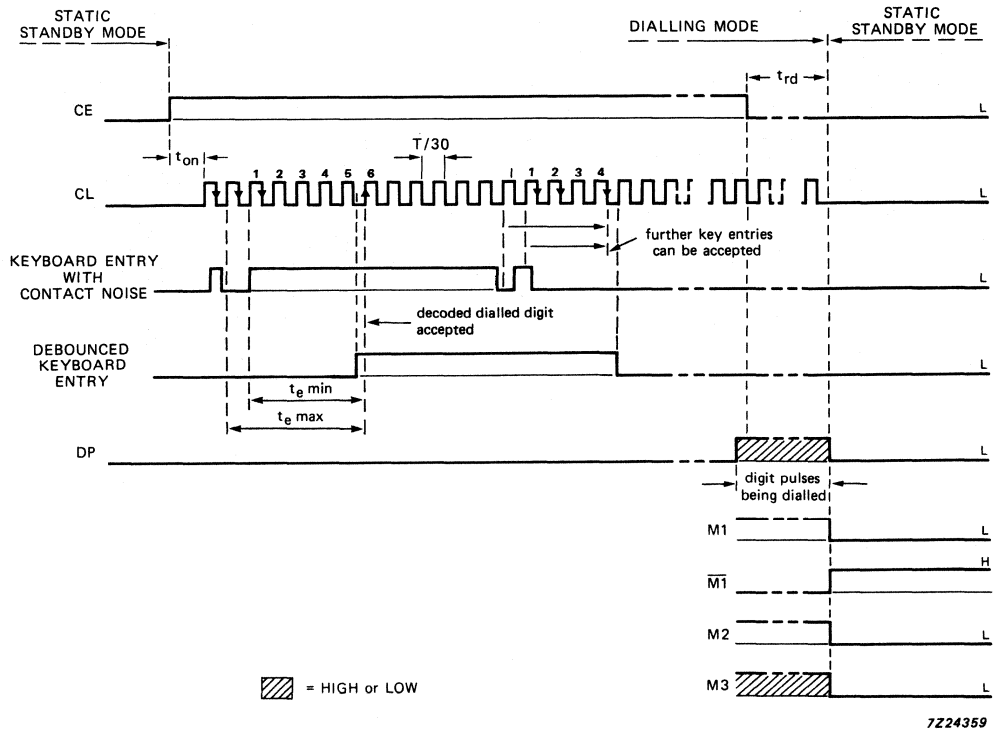


Fig.6 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL is an internal signal.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 7.

Ten clock pulse periods (t_d) after CE goes HIGH, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 8).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. After CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the push-button can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 7. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,5 V.

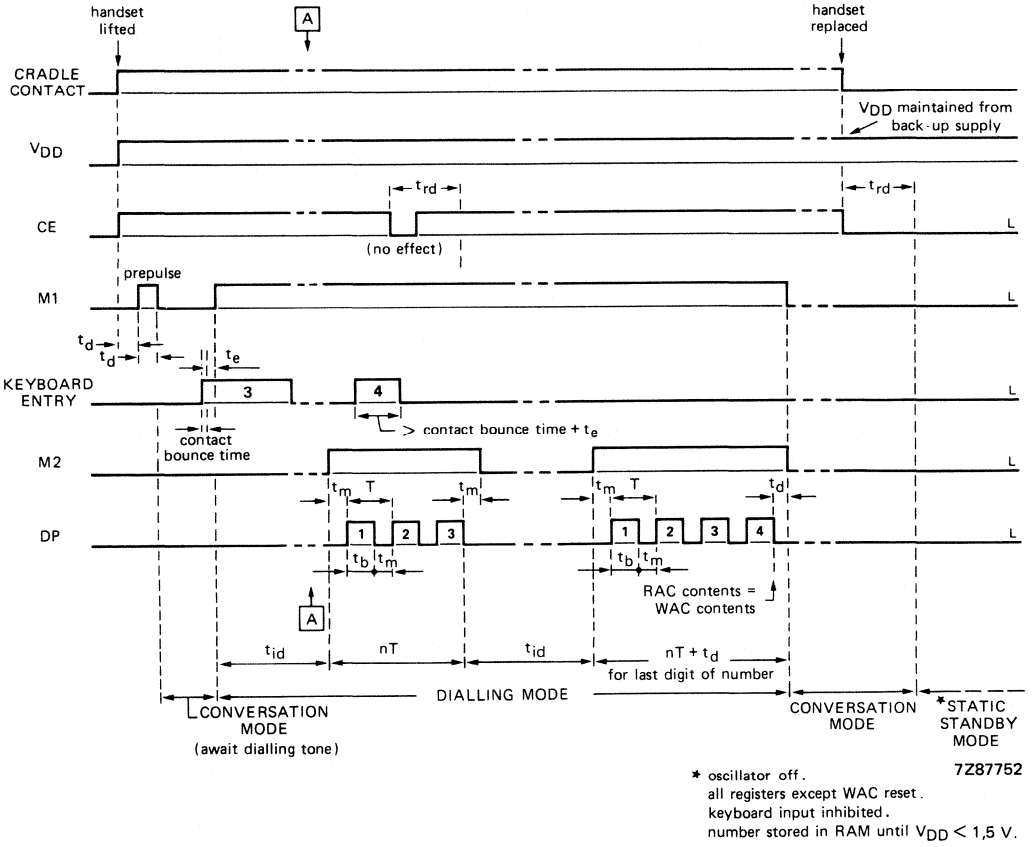


Fig. 7 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

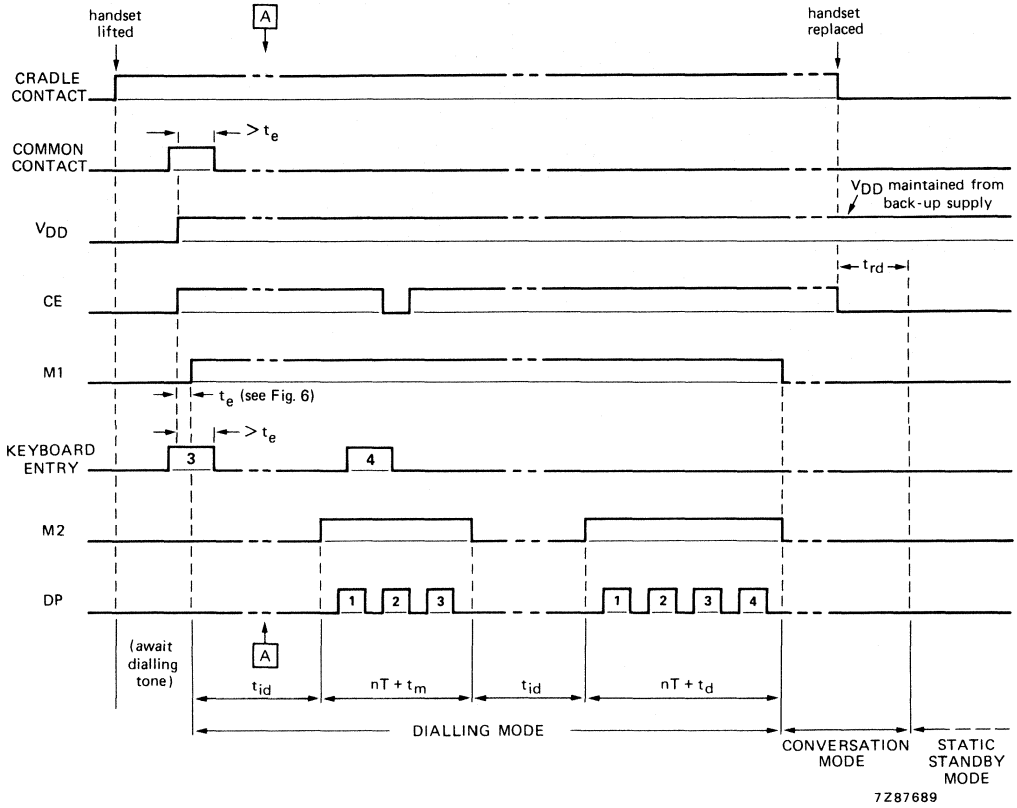


Fig. 8 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 7 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 9, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

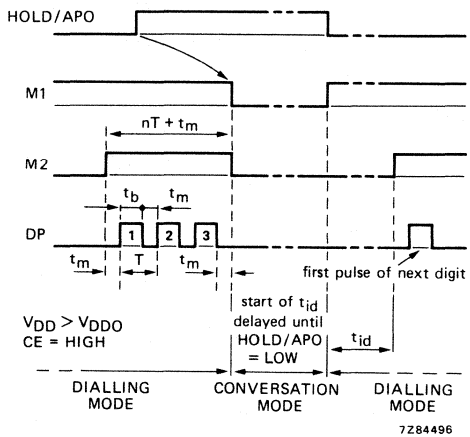


Fig. 9 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

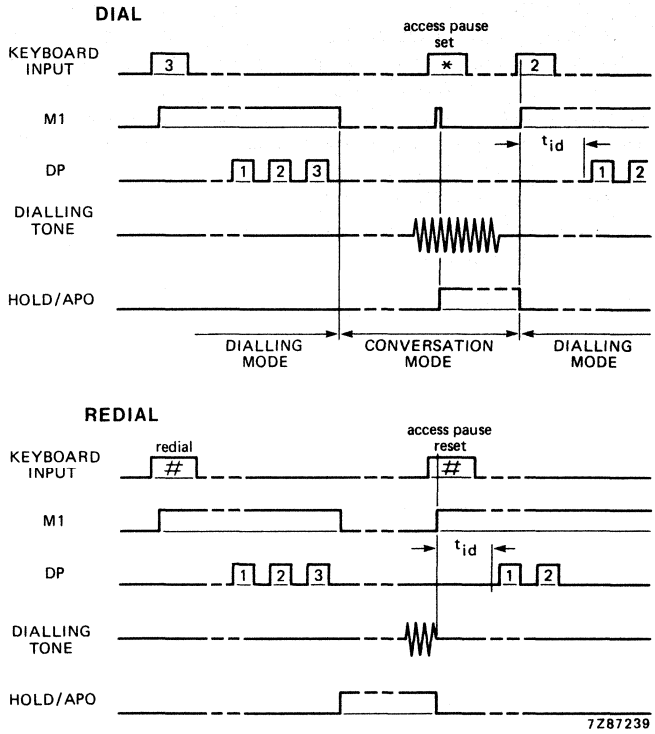


Fig. 10 Dialling sequence showing how an access pause code is stored in the RAM (DIAL) and how the access pause code is reset during the REDIAL.

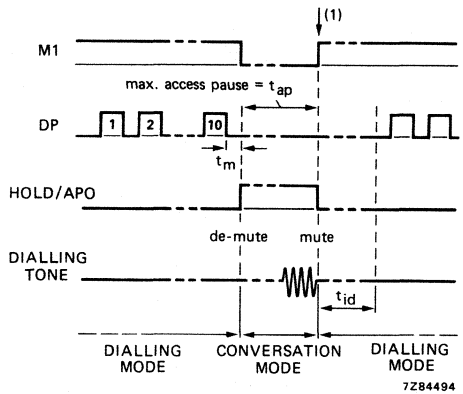
Note: access pause can be reset by pressing any key.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO) will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is stored in the RAM during original entry by pressing the access pause key (*) between entering the trunk exchange code and the subscriber code, or at any other moment an access pause is required. The number of access pauses that can be inserted in this manner is only limited by the capacity of the RAM (digits + access pauses $\leqslant$ 23).

During redial, access pauses will be automatically regenerated.
Two methods of terminating an access pause:

1. Manually, by pressing the redial key (#)
2. With an external tone recogniser, by forcing HOLD/APO to LOW.



(1) a. Access pause reset by pressing redial key (#).
b. HOLD/APO controlled by tone recogniser: HOLD/APO forced to LOW.

Fig. 11 Timing diagram showing Access Pause Reset, during redial.

Note: access pause can be reset by pressing any key.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,5 to 8 V
Voltage on any pin	V_I	V_{SS} −0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; f_{osc} = 13,8 kHz (R1, R2 and C see Fig. 5); T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit	conditions
Operating supply voltage	V_{DD}	2,0	3	6	V	T_{amb} = −25 to +70 °C
Standby supply voltage (note 1)	V_{DDO}	1,5	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	20	40	µA	CE = V_{DD}; note 2
	I_{DD}	–	75	150	µA	CE = V_{DD}; V_{DD} = 6 V; note 2
Standby supply current	I_{DDO}	–	0,65	2,0	µA	CE = V_{SS}; note 2
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE LOW	$-I_{IL}$	–	–	50	nA	CE = V_{SS}
HIGH	I_{IH}	–	–	50	nA	CE = V_{DD}
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current F02	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	30	–	µA	X connected to Y, CE = V_{DD}
Keyboard 'ON' resistance	R_{KON}	–	–	2	kΩ	contact ON; note 3
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 3
Outputs R1 to R4						
sink current	I_{OL}	–	3	–	µA	V_{OL} = 0,5 V
source current	$-I_{OH}$	–	40	–	µA	V_{OH} = 2,5 V

Notes

1. V_{DDO} = 1,5 V only for redial.
2. All other inputs and outputs open.
3. Guarantees correct keyboard operation.

parameter	symbol	min.	typ.	max.	unit	conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	2,0	4,0	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,8	3,6	mA	V_{OH} = 2,5 V
Latch output HOLD/APO						
source current	$-I_{OH}$	0,7	2,0	4,0	mA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 13,8 kHz

input levels of F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F02}	LOW	HIGH		conditions (note 3)
		symbol			unit	
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10	19,2	Hz	
Dialling pulse period	$1/f_{DP}$	T_{DP}	100	52,2	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	300	575	Hz	
Break time (note 1)	$3/5 \times T_{DP}$	t_b	60	31,3	ms	M/S = H; n.c.
Make time (note 1)	$2/5 \times T_{DP}$	t_m	40	20,9	ms	M/S = H; n.c.
Break time (note 2)	$2/3 \times T_{DP}$	t_b	66,6	34,8	ms	M/S = L
Make time (note 2)	$1/3 \times T_{DP}$	t_m	33,3	17,4	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	800	417	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	160	83,5	ms	
Prepulse duration	$1/3 \times T_{DP}$	t_d	33,3	17,4	ms	
Debounce time						
min.	$5/30 \times T_{DP}$	$t_{e\ min}$	16,66	8,7	ms	
max.	$6/30 \times T_{DP}$	$t_{e\ max}$	20,0	10,44	ms	

parameter	symbol	min.	typ.	max.	unit	conditions
Frequency stability for f_{DP} = 10 Hz						see Fig. 12
V_{DD} = 2 to 6 V	Δf_{DP}	–	0,52	–	Hz	T_{amb} = 25 °C
V_{DD} = 3 V	Δf_{DP}	–	–0,144	–	Hz	T_{amb} = -40 to +85 °C

Notes

1. Mark-to-space ratio: 3:2.
2. Mark-to-space ratio: 2:1.
3. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.

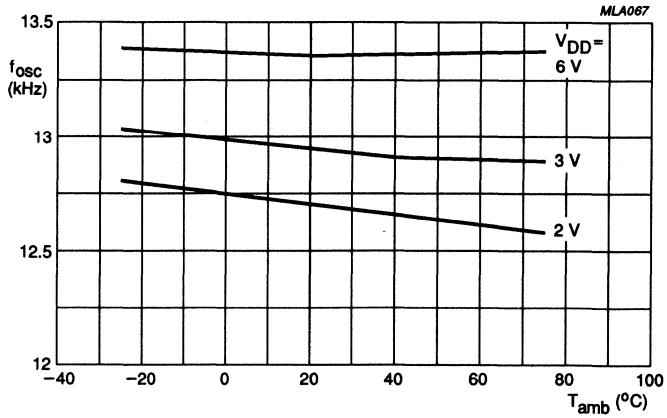


Fig. 12 RC oscillator frequency as a function of ambient temperature (T_{amb}) and supply voltage (V_{DD}).

Table 1 Dialling pulse frequency variation (T_{amb} = −40 to + 85 °C)

V_{DD} (V)	Δf_{DP} (Hz)
6,0	−0,007
3,0	−0,144
2,0	−0,217

Maximum frequency variation (Δf_{DP}):

$\Delta f_{DP} = f_{DP}$ (6 V, −40 °C) − f_{DP} (2 V, + 85 °C) = 0,637 Hz.

LOW COST SPEECH DEMONSTRATION BOARD

GENERAL DESCRIPTION

The low cost speech demonstration board is designed to add voice output to existing card based electronic equipment with the minimum of additional effort and components. The majority of components used are of the CMOS type with low power consumption making the board suitable for battery operation.

Applications include speech evaluation and speech demonstration.

FEATURES

- PCF8200 speech synthesizer
  - Male and female speech of very high quality
  - CMOS technology
  - Extended operating temperature range
  - Programmable speaking speed
- Low current consumption
  - All major components use CMOS technology (PCF8200, 80C39 and 27C64)
- Very large vocabulary up to 12 minutes
  - 4 EPROM sockets
  - EPROM selection for 27C16 to 27C256
  - Low data rates for synthesizer (average 1500 bits per second)
- Easy interfacing
  - 8-bit parallel data bus/key switch input
  - Volume control, speaker connection
  - Control signals (e.g. RESET, BUSY etc etc)
- Simple operating modes
  - ROM selection
  - Word sequence within a ROM
  - Repeat last utterence
  - Control software is readily customizeable
  - To implement parameter download from external source
- Single Eurocard size PC board
- Single +5 V supply
- Low cost

APPLICATIONS

- OEM design-in
- May be simply used with many card systems for speech evaluation
- Speech demonstration
  - Particularly simple when used with the OM8201 (Speech Demonstration Box)

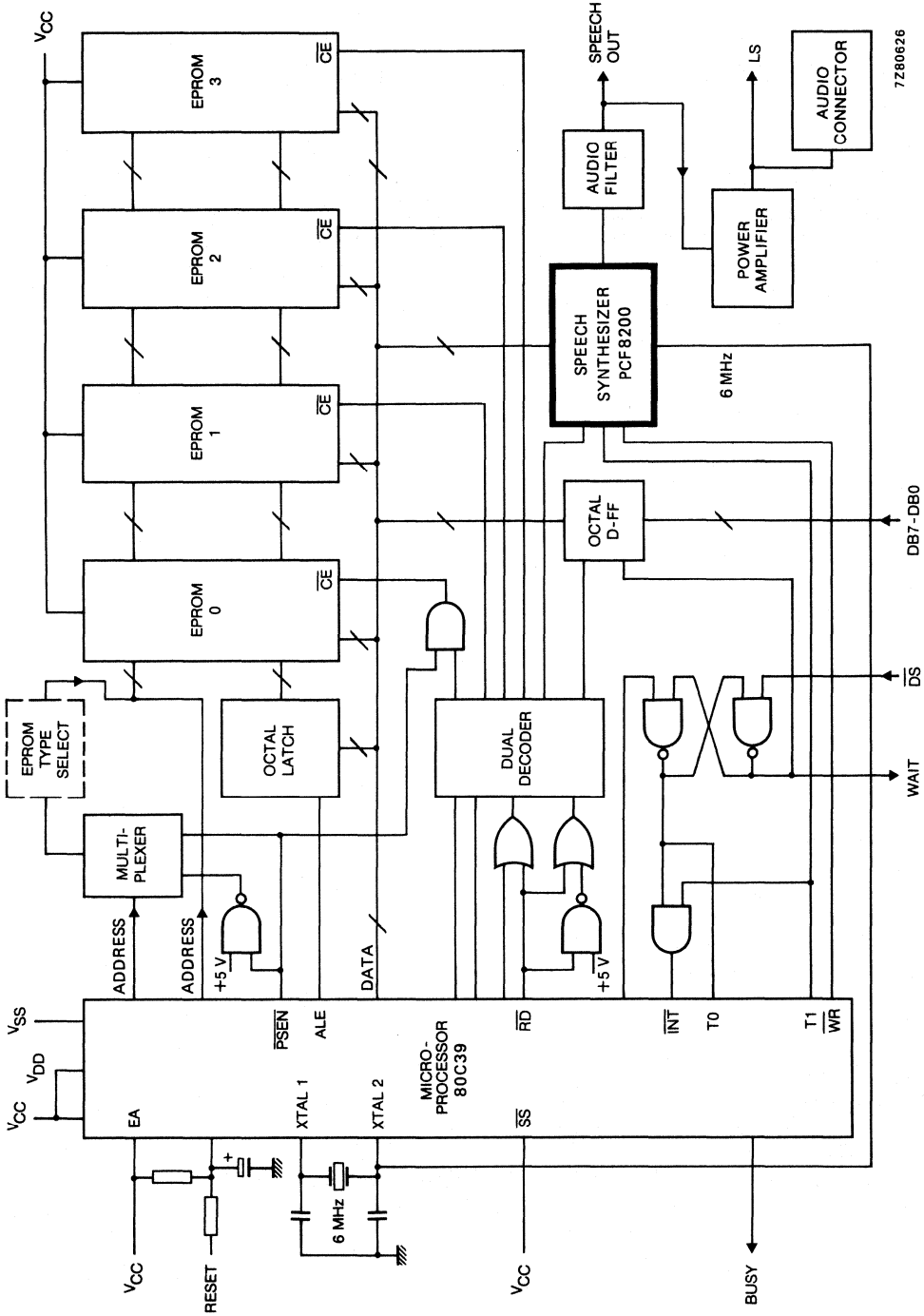


Fig. 1 Block diagram.

OPERATION

HARDWARE DESCRIPTION

The main controlling microprocessor is an 80C39 running at 6 MHz. This device supplies all of the main controlling signals for the board operation and the interfacing to any external system.
Four sockets are provided for EPROMS which contain speech coding. These may be 27C16 types, through to 27C256 types; the sockets will be a low insertion force type to allow for easy customizing.
The board will be supplied with one socket occupied by a 27C64 which will contain the control program and some speech examples. All four EPROM sockets must contain the same EPROM type.

The speech synthesizer PCF8200 converts the coding into a speech output. This synthesizer has been designed to simulate the human vocal tract using five formants for male and four formants for female speech. Periodic updating of the parameters for these formants can produce very high quality speech.

The output of the synthesizer can be fed into an audio amplifier, TDA7050, via a resistor-capacitor filter network which provides a frequency cut-off above 5 kHz of about 25 dB. The configuration of the audio amplifier used on this board gives an output of 140 mW peak power into a 25 Ω speaker from a 5 V supply.

Connections are made to the board via a standard DIN/IEC connector. This allows access to the 8-bit parallel data bus so that speech coding from an external source may be used, if implemented, and allows the selection of speech phrases by an external system, such as a microcomputer or even a bank of switches. The same connector also permits the addition of a volume control, loudspeaker, a high impedance audio output, and power supply. The control signals RESET, BUSY, WAIT and DS are also taken to the outside of the board. There is also a loudspeaker plug on the board.

All components are contained on a standard single Eurocard, and therefore suitable for rack mounted equipment.

SOFTWARE DESCRIPTION

All the software required to operate the board is contained in the only EPROM supplied. The software is written in modular from so that it is possible for a customer to alter or add to any particular function which suits his applications. An industrial standard microprocessor was chosen so that readily available development systems could be used to facilitate this modification.

There are four main modes of operation:

- ROM Selection
- Word Sequence
- Repeat Word
- Speaking Speed Selection

These modes are all controlled by software.

ROM Selection mode permits access to an individual EPROM and pronounces the first utterence from that EPROM.

Word Sequence gives the next word (activated by repeated access to the same EPROM) and if continually exercised will keep looping on the words in that EPROM.

The Repeat Word command allows indefinate repetition of the last utterance pronounced.

The Speaking Speed Selection allows the utterence to be pronounced at a different speed.

The software also controls the address sequencing within the utterance and ensures that the required data is supplied to the synthesizer.

There are also some examples of words/utterences encoded in the remainder of the supplied EPROM. These words are intended for demonstration purposes and will show the features of the synthesizer when selected. The main features being illustrated are:

- Male speech in several languages
- Female speech in several languages
- Programmable speaking speed

ORDERING INFORMATION

Product name: Low Cost Speech Demonstration Board

Type number: OM8200

Ordering code: 9337 541 30000

Orders should be placed with your local Philips/Signetics agency.

SPEECH DEMONSTRATION BOX

GENERAL DESCRIPTION

Speech demonstration box OM8201 is designed to be used in conjunction with the low cost speech demonstration board OM8200. The box contains all the necessary components to drive the board. The combination of these two components make an extremely attractive demonstration unit.

FEATURES

- Low cost
- Can use unmodified OM8200 board which allows access to all features of the OM8200
- Single + 9 V supply
  - Low power consumption therefore permits battery operation
  - External power supplies may also be used
  - Voltage is regulated and dropped to a standard + 5 V for the OM8200 board
- Simple mechanical construction
  - Allows easy access to the OM8200 for changing EPROMS
- Contains all peripherals needed to drive the OM8200

HARDWARE DESCRIPTION

The box contains a set of eight keypad switches which are connected to the data bus. Four switches can select which EPROM your speech data is derived from. Repeated pressing of an EPROM switch increments the expression number which will be uttered. To repeat the last expression, a separate switch must be activated.

It is possible in the PCF8200 to change the rate of speaking to 73%, 123% or 145% of the normal speed. A switch has been included on the box which will sequence through the speed options making the same utterance every time.

One of the two remaining switches is the master reset for the program and the other is for future enhancements of the box.

Included in the box are, the volume control for the amplifier, the loudspeaker, and a high impedance audio output.

The final piece of electronics is the power supply. This can be supplied from a + 9 V internal battery or from a + 9 V external supply. The + 9 V is regulated to a + 5 V supply which is then fed to other parts of the box and to the OM8200.

The box is of simple construction and allows easy access to the OM8200 for changing of EPROMS.

SOFTWARE DESCRIPTION

There is no software in the OM8201. The software of the OM8200 may be used in an unmodified form without any problems. However, if changes have been made to the control program of the OM8200 then different functions for the switches of the box can be achieved.

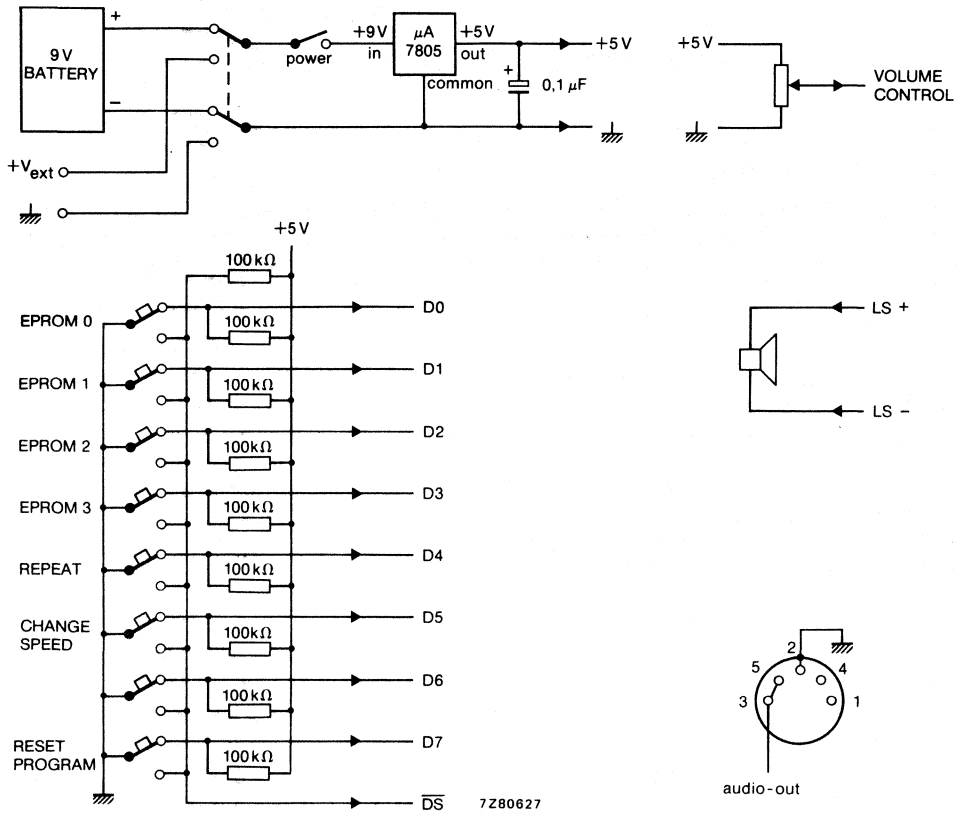


Fig. 1 Schematic diagram.

ORDERING INFORMATION

Product name: Speech Demonstration Box

Type number: OM8201

Ordering code: 9337 541 40000

N.B. OM8200 must be ordered as well if this box is to be used in demonstration mode. The order number for the OM8200 is 9337 541 30000.

Orders should be placed with your local Philips/Signetics agent.

UPDATE PACKAGE FOR EXISTING OM8010 SPEECH EDITING SYSTEM

GENERAL DESCRIPTION

This package, OM8209, is an updating package which allows the users of our already existing editing system for the MEA8000 also to generate the parameters and codes necessary for our new CMOS voice synthesizer, PCF8200.

FEATURES

- Hardware updates for the synthesizer board to permit output via the PCF8200 and the MEA8000
- Software update to generate parameters and codes for the PCF8200
- Gives all the features of the OM8210 to those who have the OM8010 (used for generating first generation synthesizer codes)

Hardware

The only hardware changes are to the synthesizer card. This card is completely replaced by a new synthesizer card. This card contains the new PCF8200 voice synthesizer, the MEA8000 voice synthesizer and the necessary components required to interface the synthesizers to their environment.

Software

The software package is exactly the same as in the OM8210, for fuller information consult the data for that device.

ORDERING INFORMATION

Product name: Update package for existing OM8010 Speech Editing System using the HP9816S

Type number: OM8209

Ordering number: 9337 564 50000

Orders should be placed with your local Philips/Signetics agent.

SPEECH ANALYSIS/EDITING SYSTEM

GENERAL DESCRIPTION

The OM8210 is a speech analysing/editing system, and comprises of a speech adapter box and associated software. The system uses either the HP9816S or IBM-PC personal computer.
The OM8210 and the computer function together to produce speech coding for the PCF8200.
The system has many commands available, mostly single key operations, which gives it flexability.

FEATURES

- Input sampling of analogue speech signals
- Speech analysis
- Graphic parameter representation
- Parameter editing screen
- Conversion of parameters to PCF8200 synthesizer
- EPROM programming
- Parameter storage on floppy disc
- Speech output via PCF8200 voice synthesizer

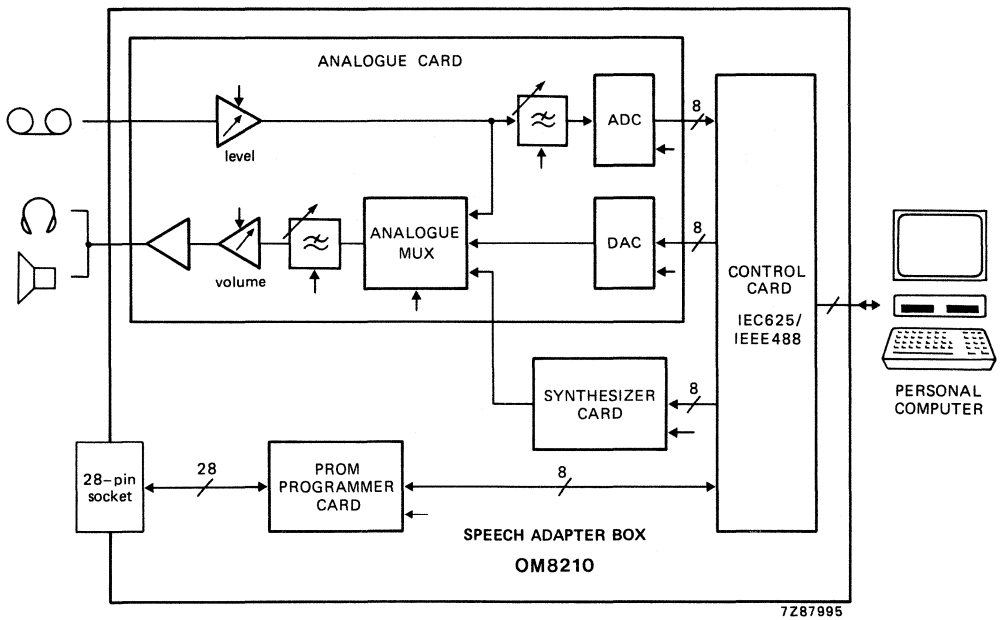


Fig. 1 Block diagram.

HARDWARE DESCRIPTION

The hardware for the OM8210 is contained in an attractive box with access to all the interconnections (IEC 625, interface loudspeaker, headphones, tape input, and EPROM socket), from the front panel. There are four single Eurocards and a power supply forming the speech adapter box.
These cards are:

- Analogue Card
- Synthesizer Card
- EPROM Card
- Control Card

Analogue Card

On this card, the level of the recorded audio input signal is adjusted by an electronic potentiometer. Before the audio is sampled, frequencies higher than half the sampling frequency are removed by a switched capacitor filter of the type normally used for codecs. A 12-bit analogue-to-digital converter (ADC) produces the digital samples that are sent to the control card. An 8-bit digital-to-analogue converter (DAC) on the analogue card allows the sampled speech to be output. The audio input signal, the sampled speech and the synthesized speech are selected by an analogue multiplexer, filtered, and adjusted for volume before reproduction by a loudspeaker.

The use of integrated electronic potentiometers and codec filters substantially reduces the number of components required while maintaining high performance.

Synthesizer Card

This card accommodates the PCF8200 voice synthesizer and a small amount of peripheral components and a socket for the MEA8000 voice synthesizer.

EPROM Programmer Card

This card allows four different types of EPROM (2716, 2732, 2732A and 2764) to be programmed under software control. All the hardware to generate the programming voltages and the programming waveforms are on this card.

Control Card

This card performs three functions:

- IEC 625/IEEE 488 interface
- Control sequencer
- Clock generator

The IEC/IEEE interface is a simple talker/listener implementation with a HEF4738 circuit.

An FPLA control sequencer provides the handshake signals for IEC/IEEE interface and the chip enable signals for the rest of the system (the ADC, the DAC, the synthesizer and control circuits).

The filter sampling frequency is generated with a software programmable PLL frequency synthesizer. The speech sampling frequency is derived from the filter sampling frequency by frequency division. Hence, the filter frequency cut-off and the sample rate of the ADC and the DAC are automatically linked.

The hardware includes all the necessary cables, adapter plug, loudspeaker, headphone and power supply.

SOFTWARE DESCRIPTION

The software for this speech coding system has been developed and arranged for optimum user convenience. There are eight modes available.

Each mode and each command in the mode is selected by single key entries. Commands that can destroy data have to be confirmed before they are executed. More than 100 commands are available. The modes are:

Sample Mode	Samples and digitizes the recorded speech, the amplitude can be checked and speech segments selected. The sampled speech is stored in a memory and can be displayed or made audible.
Analysis Mode	Generates speech parameters from samples. The analysis selects the voiced/unvoiced sections, extracts the formants (5 for male and 4 for female), amplitude, and the pitch, and quantisizes the speech parameters.
Parameter Edit Mode	Speech parameters are displayed graphically on the VDU and can be edited to correct errors in the analysis, improve speech quality by altering contours, or amplitudes, concatenate sounds and optimize data rate by editing the frame duration.
Code Mode	Generates PCF8200 code and permits the arrangement of utterences in the optimum order of application. This mode also generates the address map at the head of the EPROM.
EPROM Mode	Used to program/read EPROMS with data for the code memory also possible is a new check, bit check and verification commands.
File Mode	Stores speech parameters or codes on disc, can also assemble code speech segment from an already existing library.
Media Mode	For diskette initialization and making back-up copies.
Option Mode	Allows the system configuration to be read or changed.

The software is supplied on two diskettes, one labelled 'BOOT' which wakes up the system and also contains the system library routines. The other diskette labelled 'SPEECH' contains the speech program, the disc initialization and the file handler programs. The 'BOOT' disc is not required during operation, giving a free disc drive with the system for a diskette to store speech parameter files.

Computer System

The following equipment is required to make a complete Hewlett Packard based editing system:
- HP9816S-630 (optimum computer type) or HP9817
- HP9121D (dual floppy disc)
- Additional memory card for the HP9816S (512 K bytes total required)

The following equipment is required to make a complete IBM based editing system:
- IBM-PC or PC-XT or Philips P3100
- Additional memory (512 K recommended)
- Display graphics card (Hercules monochrome)
- IEEE488 card (Tecmar Rev. D.)

ORDERING INFORMATION

Product name:	Speech Analysis/Editing System
Type number:	OM8210
Ordering code:	9337 561 50112

The computer system should be purchased from your local agents.
The OM8210 should be ordered through your local Philips/Signetics agent.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	December 1990

PC.8582 Family
256 x 8-BIT CMOS EEPROMS with I²C-BUS interface

GENERAL DESCRIPTION

The 2 Kbit (256 x 8-bit) CMOS EEPROMS are floating gate electrically erasable programmable read only memories.

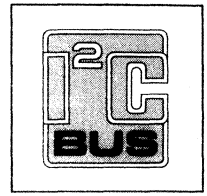
Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient.

Chip select is accomplished by the three address inputs, which also allows up to eight devices to be connected to the I²C-bus.

Features

- Non-volatile storage of 2 Kbits organized as 256 x 8-bits
- Only one power supply required
- On chip voltage multiplier
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- Power-on reset
- 10 years non-volatile data retention time
- Pin and address compatible to PCF8570, PCF8571, and PCF8581
- Mini-pack package for SMD technology.



QUICK SELECTION GUIDE

TYPE	PCF8582A	PCA8582B	PCF8582C	PCD8582D	PCF8582E
extended temperature range	•	•	•	–	•
extended voltage supply range	–	–	•	•	–
no external RC required	–	–	•	•	•
single bit error correction for extended number of erase/write cycles	–	•	•	•	•

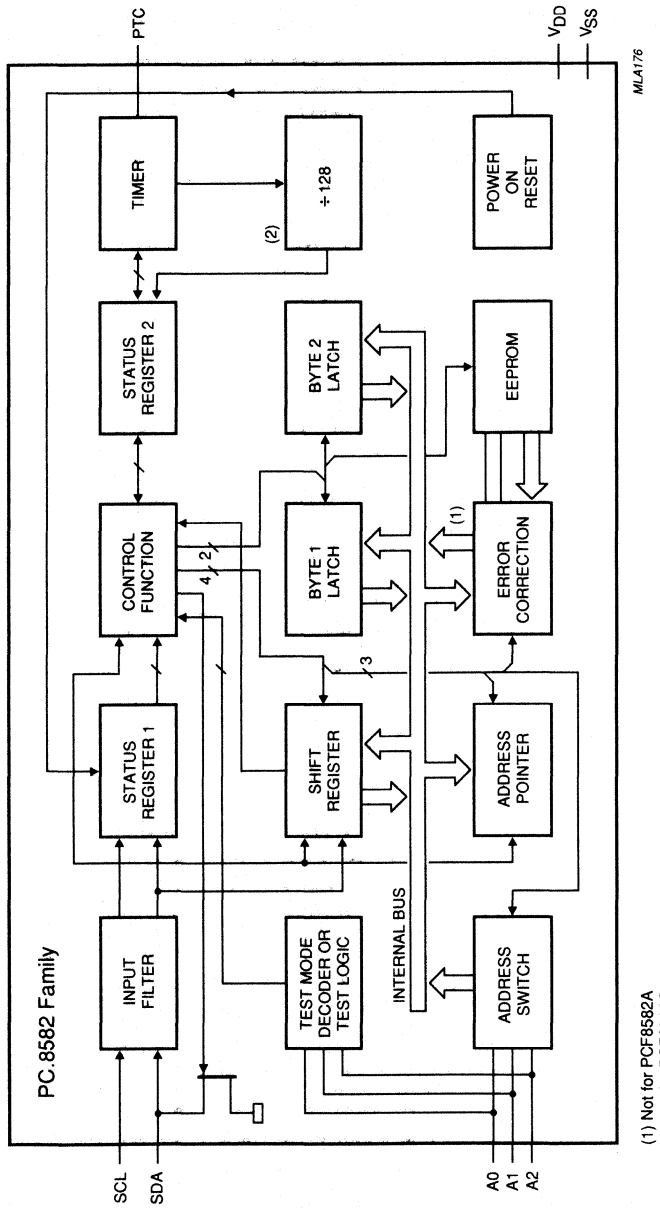


Fig.1 Block diagram.

(1) Not for PCF8582A.

(2) Not for PCF8582C, PCD8582D or PCF8582E.

256 x 8-BIT CMOS EEPROMS with I²C-BUS interface

PC.8582 Family

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA8582BP	8	DIL	plastic	SOT97
PCA8582BT	16	SO16L	plastic	SOT162A
PCD8582DP	8	DIL	plastic	SOT97
PCD8582DT	8	SO8	plastic	SOT96A
PCF8582AP	8	DIL	plastic	SOT97
PCF8582AT	16	SO16L	plastic	SOT162A
PCF8582CP	8	DIL	plastic	SOT97
PCF8582CT	16	SO16L	plastic	SOT162A
PCF8582EP	8	DIL	plastic	SOT97
PCF8582ET	8	SO8	plastic	SOT96A

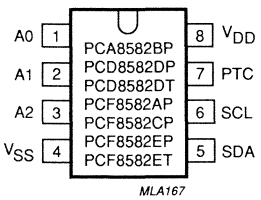


Fig.2 Pin configuration (SOT96A and SOT97).

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	address input
A1	2	address input
A2	3	address input
V_{SS}	4	ground
SDA	5	serial data
SCL	6	serial clock
PTC	7	can be connected to V_{DD} or left open-circuit
V_{DD}	8	positive supply voltage

FUNCTIONAL DESCRIPTION

Characteristics of the I²C-bus

The I²C-bus is a bidirectional, 2-line communication between different ICs or modules. The two lines are for serial data (SDA) and serial clock (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- data transfer may be initiated only when the bus is not busy.
- during data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy: both data and clock lines remain HIGH.
Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH defines the start condition.

Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.

Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

256 x 8-BIT CMOS EEPROMS with I²C-BUS interface

PC.8582 Family

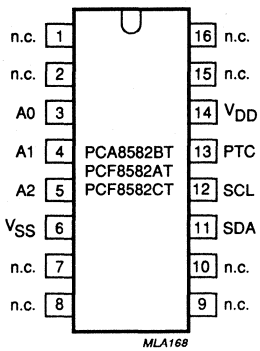


Fig.3 Pin configuration (SOT162A).

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
A0	3	address input
A1	4	address input
A2	5	address input
V_{SS}	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
SDA	11	serial data
SCL	12	serial clock
PTC	13	can be connected to V_{DD} or left open-circuit
V_{DD}	14	positive supply voltage
n.c.	15	not connected
n.c.	16	not connected

By definition a device that sends a signal is called a "transmitter" and the device which receives the signal is called a "receiver". The device which controls the signals is called the "master". The devices that are controlled by the master are called "slaves".

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse.

The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

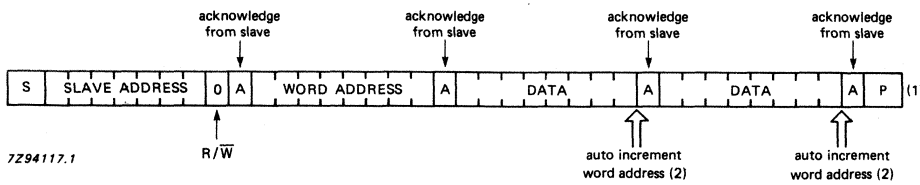
Set up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

(1)

(1) Detailed specifications of the I²C-bus are available on request.

I²C-bus protocol

The I²C-bus configuration for different READ and WRITE cycles of the EEPROM are shown in Figures 4, 5 and 6.



(1) After this stop condition the ERASE/WRITE cycle starts and the bus is free for another transmission. During the ERASE/WRITE cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

(2) The second data byte is voluntary. It is not allowed to ERASE/WRITE more than two bytes.

Fig.4 Master transmitter transmits to EEPROM slave receiver (ERASE/WRITE mode).

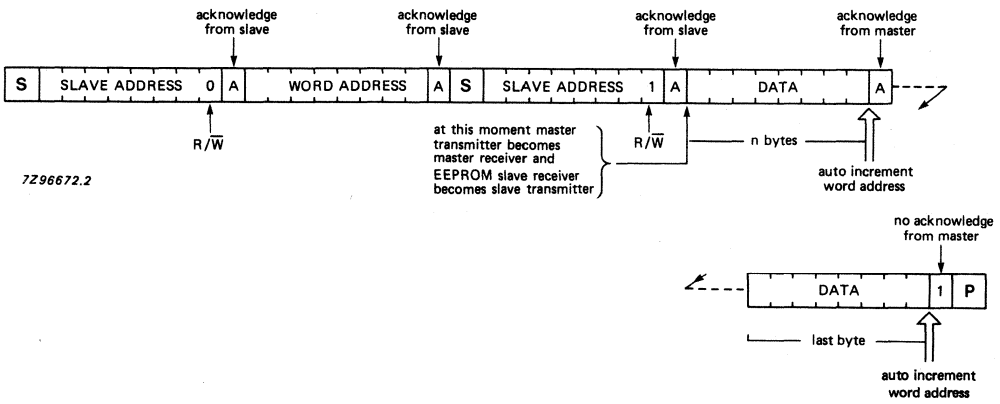


Fig.5 Master reads EEPROM slave after setting word address (write word address; READ data).

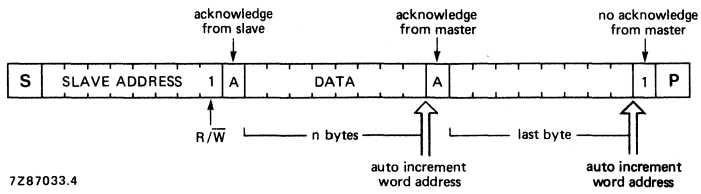


Fig.6 Master reads EEPROM slave immediately after first byte (READ mode). Write protection can be achieved by connecting pin PTC to V_{DD} (for PCF8582A and PCA8582B only).

The slave address is defined in accordance with the I²C-bus specification as:

1	0	1	0	A2	A1	A0	R/W

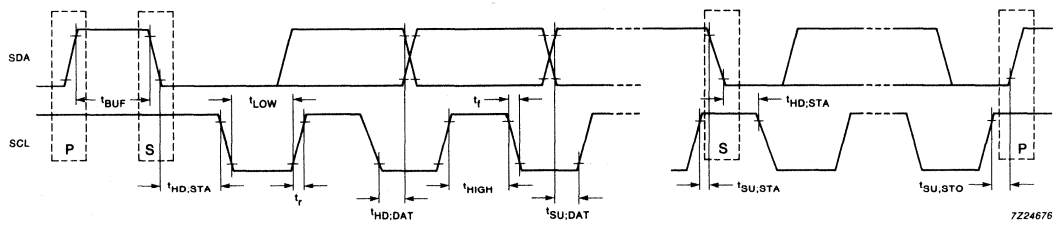


Fig.7 I²C-bus timing.

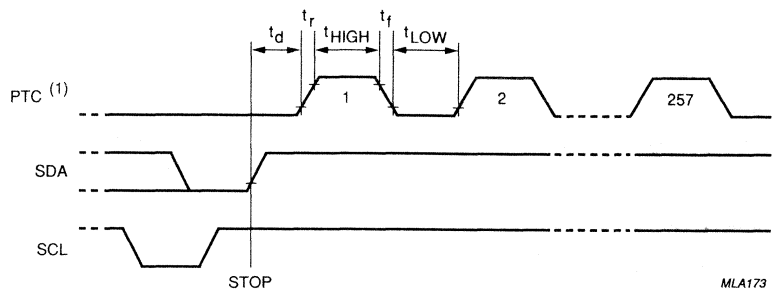


Fig.8 One byte ERASE/WRITE cycle.

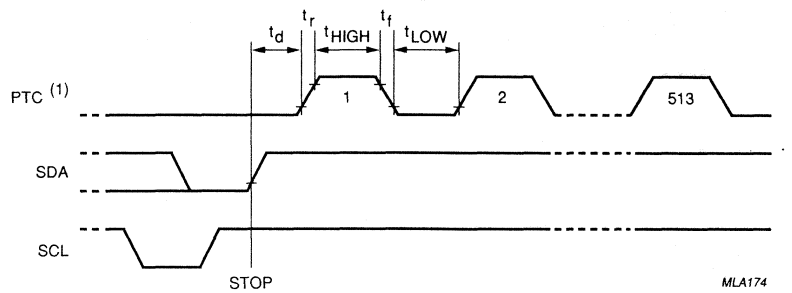
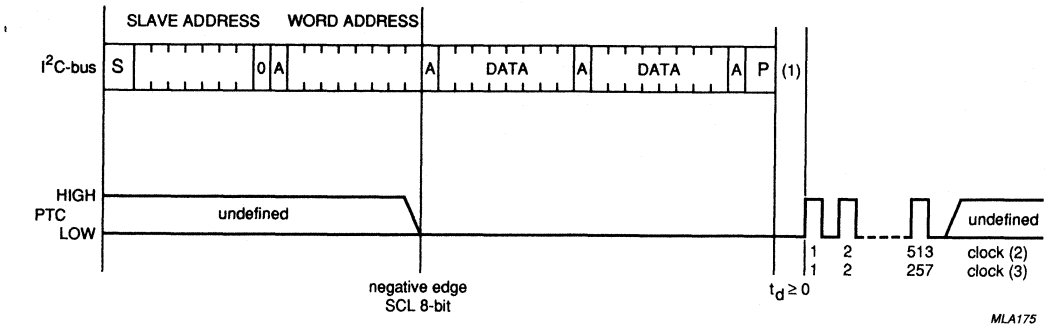


Fig.9 Two byte ERASE/WRITE cycles.



(1) If an external clock is chosen, this information is latched internally by leaving pin PTC LOW after transmission of the eigth bit of the word address (negative edge of SCL). The state of pin 7 then, may be previously undefined.

(2) 2 byte programming

(3) 1 byte programming

Fig.10 External clock.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+7.0	V
V_I	voltage on any input	$\|Z_I\| > 500\ \Omega$	V_{SS}−0.8	V_{DD} + 0.8	V
I_I	current on any input pin		-	1	mA
I_O	output current		-	10	mA
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	operating ambient temperature range				
	PCF8582A/C/E		−40	+85	°C
	PCA8582B		−40	+125	°C
	PCD8582D		−25	+70	°C

CHARACTERISTICS

PCF8582A; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C
PCA8582B; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +125 °C
PCF8582C; V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C
PCD8582D; V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C
PCF8582E; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage					
	PCF8582A/E, PCA8582B		4.5	-	5.5	V
	PCF8582C		2.5	-	6.0	V
	PCD8582D		3	-	6	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz				
	PCF8582A	$V_{DD(max)}$	–	–	0.4	mA
	PCA8582B	$V_{DD(max)}$	–	–	0.8	mA
	PCF8582C/PCD8582D	V_{DD} = 3 V	–	–	0.25	mA
		V_{DD} = 6 V	–	–	1.6	mA
	PCF8582E	$V_{DD(max)}$	–	–	1.6	mA
$I_{DDE/W}$	supply current ERASE/WRITE	f_{SCL} = 100 kHz				
	PCF8582A/PCA8582B	$V_{DD(max)}$	–	–	2	mA
	PCF8582C/PCD8582D	V_{DD} = 3 V	–	–	0.35	mA
		V_{DD} = 6 V	–	–	2.5	mA
	PCF8582E	$V_{DD(max)}$	–	–	2.5	mA
I_{stb}	supply current STANDBY					
	PCF8582A	$V_{DD(max)}$	–	–	10	µA
	PCA8582B	$V_{DD(max)}$	–	–	20	µA
	PCF8582C/PCD8582D	V_{DD} = 3 V	–	–	3.5	µA
		V_{DD} = 6 V	–	–	10	µA
	PCF8582E	$V_{DD(max)}$	–	–	10	µA
PTC input (PCF8582A/PCA8582B)						
V_{IH}	input voltage HIGH		V_{DD}−0.3	–	V_{DD} + 0.8	V
V_{IL}	input voltage LOW		−0.8	–	V_{SS} + 0.3	V
PTC input (PCF8582C/PCD8582D/PCF8582E)						
V_{IH}	input voltage HIGH		0.9 V_{DD}	–	V_{DD} + 0.8	V
V_{IL}	input voltage LOW		−0.8	–	0.1 V_{DD}	V
SCL input						
V_{IH}	input voltage HIGH					
	PCF8582A/PCA8582B		3	–	V_{DD} + 0.8	V
	PCF8582C/PCD8582D/PCF8582E		0.7 V_{DD}	–	V_{DD} + 0.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDA input/output						
V_{IL}	input voltage LOW					
	PCF8582A/PCA8582B		−0.3	–	1.5	V
	PCF8582C/PCD8582D/PCF8582E		−0.8 V_{DD}	–	0.3 V_{DD}	V
V_{OL}	output voltage LOW	I_{OL} = 3 mA				
	PCF8582A/PCA8582B	V_{DD} = 4.5 V	–	–	0.4	V
	PCF8582C	V_{DD} = 2.5 V	–	–	0.4	V
	PCD8582D	V_{DD} = 3 V	–	–	0.4	V
	PCF8582E	$V_{DD(min)}$	–	–	0.4	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	–	–	1	µA
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	–	1	µA
Data retention time						
t_S	data retention time	T_{amb} = 55 °C	10	–	–	yrs

WRITE CYCLE LIMITS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
t_{EW}	ERASE/WRITE cycle time				
	PCF8582A/PCA8582B		5	40	ms
	PCF8582C/PCD8582D/PCF8582E		5	25	ms
Endurance					
N_{EW}	ERASE/WRITE cycles per byte				
	PCF8582A		–	10000	
	PCA8582B	T_{amb} = 125 °C;			
		t_{EW} = 5 to 40 ms	–	50000	
		T_{amb} = 85 °C;			
		t_{EW} = 5 to 40 ms	–	100000	
		T_{amb} = 33 °C;			
		t_{EW} = 10 ms	-	500000	
	PCF8582C	T_{amb} = 85 °C;			
		t_{EW} = 5 to 25 ms	–	100000	
		T_{amb} = 33 °C;			
		t_{EW} = 10 ms	–	500000	
	PCD8582D	T_{amb} = −25 to +70 °C;			
		t_{EW} = 5 to 25 ms	–	10000	
		T_{amb} = 0 to +40 °C;			
		t_{EW} = 10 ms	–	100000	
	PCF8582E	T_{amb} = −40 to +85 °C;			
		t_{EW} = 5 to 25 ms	–	100000	

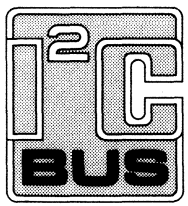
I²C-BUS CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{SCL}	clock frequency		0	-	100	kHz
C_I	input capacitance (SDA; SCL)	$V_I = V_{SS}$	-	-	7	pF
t_{BUF}	time the bus must be free before new transmission can start		4.7	-	-	µs
$t_{HD;STA}$	start condition hold time after which first clock pulse is generated		4	-	-	µs
t_{LOW}	clock period LOW		4.7	-	-	µs
t_{HIGH}	clock period HIGH		4	-	-	µs
$t_{SU;STA}$	set up time for start condition	repeated start	4.7	-	-	µs
$t_{HD;DAT}$	data hold time for bus compatible masters		5	-	-	µs
$t_{HD;DAT}$	data hold time for bus devices	note 1	0	-	-	ns
$t_{SU;DAT}$	data set up time		250	-	-	ns
t_r	SDA and SCL rise time		-	-	1	µs
t_f	SDA and SCL fall time		-	-	300	ns
$t_{SU;STO}$	set up time for stop condition		4.7	-	-	µs

Note

1. The hold time required to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter. It is not greater than 300 ns.

I²C



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specification defined by Philips.

E/W programming time control

Using external resistor R_{EW} and capacitor C_{EW} (see Table 1).

Table 1 Recommended R_{EW} and C_{EW} combinations (PCF8582A/PCA8582B only).

R_{EW} (kΩ)	C_{EW} (nF)	T_{EW} (typ.) (ms)
56	3.3	34
56	2.2	21
22	3.3	13
22	2.2	7.5

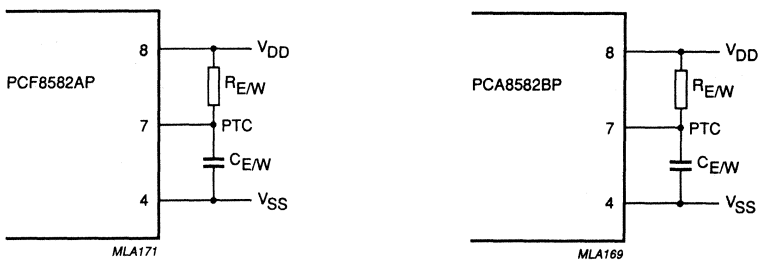


Fig.11 PTC circuit connections to PCF8582AP/PCA8582BP when using the internal oscillator.

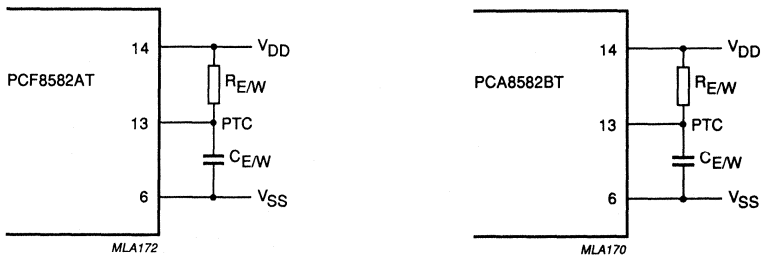


Fig.12 PTC circuit connections to PCF8582AT/PCA8582BT when using the internal oscillator.

Using external clock (see Table 2 and Figs 8, 9 and 10).

Table 2 E/W programming time control using an external clock.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
f_{CLK}	frequency	10	50	kHz
t_{LOW}	clock period LOW	10	-	µs
t_{HIGH}	clock period HIGH	10	-	µs
t_r	rise time	-	300	ns
t_f	fall time	-	300	ns
t_d	delay time	0	t_{LOW}	µs

USING AN INTERNAL OSCILLATOR

When using an internal oscillator t_{EW} has a minimum value of 5 ms and a maximum value of 25 ms; a typical value is 10 ms.

PAGING DECODER

GENERAL DESCRIPTION

The PCA5000AT is a fully integrated decoder for the CCIR Radio Paging Code number 1 (POCSAG-code). It supports two basic modes of operation:

Alert-Only-Pager. This is a stand-alone mode in which the PCA5000AT scans inputs from three external switches that relate to the states ON, OFF and SILENT. Only a few external components are required to build an Alert-Only pager.

Display-Pager. In this mode, received calls and messages are transferred via the IC's serial communication interface to an external microcontroller. A built-in voltage converter can double the supply voltage output and perform level shifting on the interface signals.

Call-alert cadences are generated when valid calls and messages are received, and status cadences to indicate the present state of the decoder are generated following a status interrogation. An on-chip 5 x 9-bit static RAM with battery back-up is provided for programming two user-addresses and for special functions. Synchronization of the input data stream is achieved by the built-in ACCESS algorithm which allows data to be synchronized without preamble detection and minimizes battery power consumption by receiver-enable control. One of three error correction algorithms is applied to received code words to optimize the call success rate.

The PCA5000AT is fabricated in SACMOS-technology to ensure low power consumption at low supply voltages. Typical applications are alert-only pagers, numeric/alphanumeric display pagers, cellular radio and data/telemetry decoders.

Features

- Wide operating supply voltage range (1.7 to 6.0 V)
- Very low supply current (15 μA typ.)
- Decodes CCIR Radio Paging Code number 1
- Data rate: 512 bits/s
- Powerful 'ACCESS' synchronisation algorithm
- Supports two user addresses
- Four cadences per user address
- Silent call storage, up to four different calls
- Interfaces directly to the UAA2033 digital paging receiver
- Directly drives a 2 kHz bleeper
- High-level alert facility requires only a single external transistor
- Receiver-enable control for battery economy
- On-chip static RAM, non-volatile with battery back-up
- On-chip voltage converter
- Level-shifted microcontroller interface
- Battery-low alert
- Out-of-range indication (optional)

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A.)

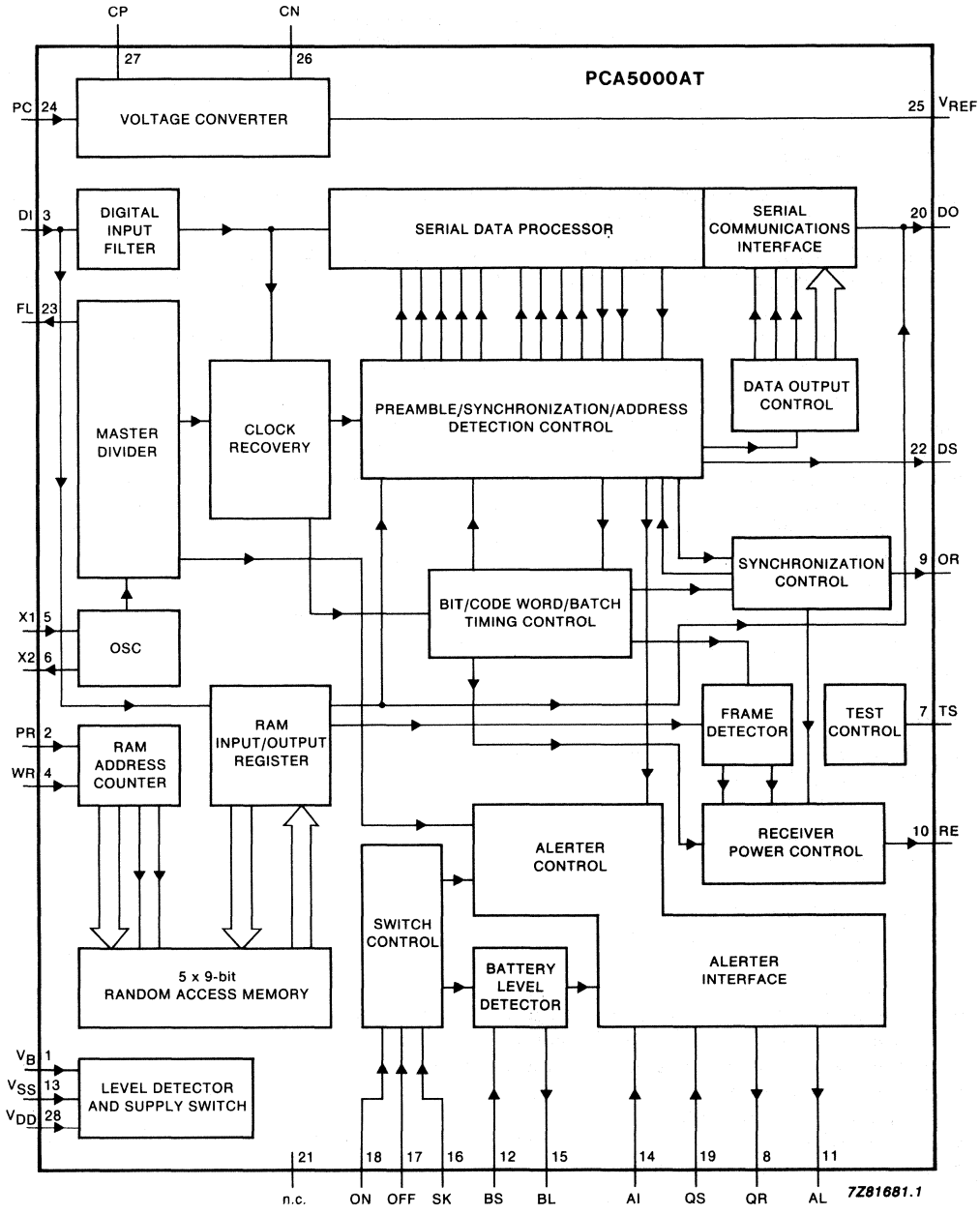


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

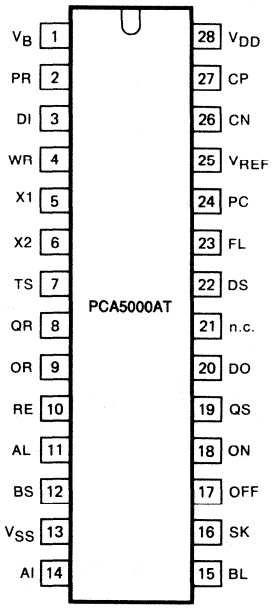


Fig. 2 Pinning diagram.

pin	mnemonic	description
1	V_B	RAM back-up negative supply voltage
2	PR	programming enable input
3	DI	serial data input
4	WR	programming WRITE input
5	X1	oscillator input
6	X2	oscillator output
7	TS	test mode enable input
8	QR	alert high-level output/vibrator output
9	OR	out-of-range output
10	RE	receiver enable output
11	AL	alert low-level output
12	BS	battery sense input
13	V_{SS}	negative supply voltage
14	AI	alarm input
15	BL	battery-low output
16	SK	silent key/mute input
17	OFF	off key/reset input
18	ON	on key/on-off input
19	QS	vibrator enable input
20	DO	received data output
21	n.c.	not connected
22	DS	received data strobe output
23	FL	frequency reference output
24	PC	power control input to voltage converter
25	V_{REF}	microcontroller interface negative reference voltage
26	CN	voltage converter external capacitor (negative)
27	CP	voltage converter external capacitor (positive)
28	V_{DD}	positive supply voltage (common)

FUNCTIONAL DESCRIPTION

Operating modes

The decoder has two basic operating modes; alert-only-pager and display-pager. There is also a programming mode in which the contents of the internal RAM are programmed or verified. The RAM holds two user-addresses and special function bits.

Alert-Only-Pager

No external microcontroller is required in this mode.

Tone-alert cadences are generated when valid calls are received. Four different alert cadences are available and are called by combinations of the function bits. The voltage doubler is disabled in this mode.

The decoder continually scans the inputs ON, OFF and SK from the external switches ON, OFF and SILENT that determine the internal operating status. Operating one of the switches first causes the cadence of the existing internal status to be generated and then, after 1.5 s switch operation, generation of a cadence to indicate the new internal status of the decoder.

Display-Pager

In this mode the decoder receives calls/messages and directs those addressed to one of the two stored user addresses to an external microcontroller for post-processing and display. Tone-alert cadences are generated when valid calls are received.

The decoder provides a doubled supply voltage output to the microcontroller and associated hardware, and the interface signals are level-shifted to allow direct coupling to the microcontroller.

The internal state of the decoder is determined by the logic levels on the static inputs ON and SK.

Internal states

If the decoder is in one of the two operating modes, its internal status is always one of the following:

OFF state. This is the power-saving inactive state in which no decoding takes place and the paging receiver is disabled. Scanning of the ON, OFF and SK inputs is maintained to allow state-changes to be effected.

ON state. This is the normal active state of the decoder. Received calls and messages are compared with the two user addresses stored in the RAM. When the validity of incoming calls is confirmed, appropriate cadences are generated and data is shifted out via the serial microcontroller interface.

SILENT state. This is the same as the ON state except that alert cadences are not generated following valid calls. Instead, if programmed as an alert-only pager, the decoder stores up to four different calls. The appropriate alert cadences are generated after the decoder has been returned to the ON-state. However, special silent override calls will cause generation of alert cadences.

DEVELOPMENT DATA

POCSAG code structure

A transmission using the CCIR Radio Paging Code No. 1 (POCSAG code) is structured according to the following rules (see Fig. 3)

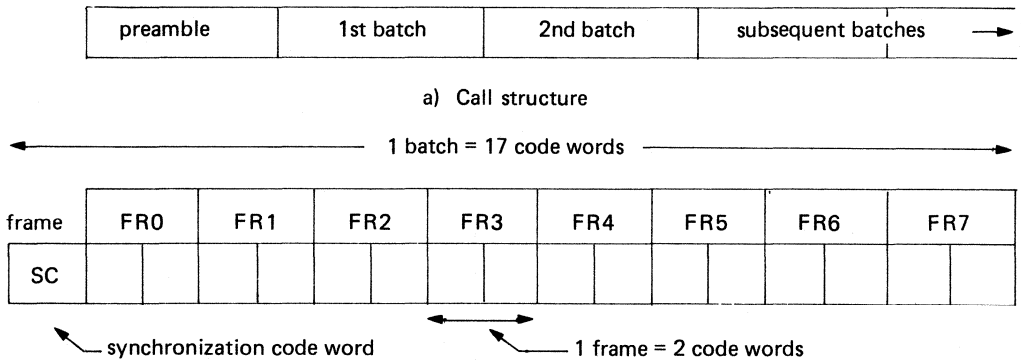
The transmission is started by sending a preamble which is a sequence of at least 576 continually alternating bits (01010101 . . .). The preamble precedes a number of batch blocks. The transmission is terminated after the last batch.

Every batch comprises a synchronisation code word with a fixed 32-bit pattern followed by eight frames (numbered 0 to 7). Only complete batches are transmitted.

A frame comprises two code words, each 32 bits long. A code word is either an address, message or an idle code word. Idle code words are transmitted to fill empty batches or to separate messages.

An address code word is coded as shown in Fig. 3; 18 bits of the 21-bit user address are coded in the code word and are protected against transmission errors by a CRC check word (bits 22 to 31). The other three bits of the user address are coded in the number of the frame in which the address code word is transmitted. Two function bits (bits 20 and 21) allow distinction between four different calls to one user address.

A message code word contains 20 bits of any information, these are also protected by a check word.



a) Call structure

b) Batch structure

bit	1	2 to 19	20	21	22 to 31	32
	0	user address	FC	FC	parity check	

c) Address code word structure (FC are function code bits)

bit	1	2 to 21	22 to 31	32
	1	message	parity check	

d) Message code word structure

Fig. 3 POCSAG coding structure.

FUNCTIONAL DESCRIPTION (continued)

Decoding

The POCSAG-coded input data is first noise-filtered by a digital filter. A sampling clock, synchronous to the 512 bits/s data rate, is derived from the filtered data.

Synchronization is performed on the POCSAG code structure using the ACCESS algorithm, which is a five-stage state mechanism.

The decoder first searches the data stream for preamble or synchronization code word patterns. Before synchronism can be achieved, the decoder must ascertain that synchronization code words are correctly positioned at the beginning of each batch. When the correct structure is detected, the decoder switches to the 'receive mode'. (The receiver enable output (RE) is active before input data is required.) Error correction algorithms are applied to the data.
If synchronization is lost (i.e. no synchronization code word found at the beginning of the next batch) the decoder enters a two-step recovery mechanism. In the first step, over the next 15 batches, the decoder attempts to resynchronize by bit-wise shifting its frame window. A 'carrier off' state is entered in the second step, in this the data stream is tested convolutionally for a preamble or synchronization code word at every effective bit position within a continuous stream of at least 17 batches. When synchronization is regained, the decoder returns to the 'receive mode'.

In the 'receive mode', the input data stream is sampled at the frame position pointed to by the RAM program and the sampled code words are error-corrected. If they are address code words, they are compared with the two user addresses from the RAM. If the result of this comparison is 'true', the following actions take place:

- a store is set for a call-alert cadence. The cadence will relate to the combination of the function bits in the accepted code word but will not be generated until the call has been terminated;
- the receiver enable output (RE) is held active so that reception of the call can continue. This condition remains until
  - another address code word or an IDLE instruction is received
  - the error-correction algorithm fails to generate a code word
  - synchronisation is lost;
- message code words attached to the validated address code word are transferred via the serial communication interface to the external microcontroller.

Programming

The on-chip RAM is organized in five 9-bit words (Fig. 4). It is used to store two user addresses (receiver identification codes) and six programmed special function bits. A lithium back-up battery maintains data retention when the main power supply is removed.

	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
word 0	A08	A07	A06	A05	A04	A03	A02	A01	A00
word 1	A17	A16	A15	A14	A13	A12	A11	A10	A09
word 2	B08	B07	B06	B05	B04	B03	B02	B01	B00
word 3	B17	B16	B15	B14	B13	B12	B11	B10	B09
word 4	FR2	FR1	FR0	SP6	SP5	SP4	SP3	SP2	SP1

where:

AXX are 18 bits of user address 'A'
BXX are 18 bits of user address 'B'
FR2 to FR0 are frame number bits common to both addresses 'A' and 'B'
SP6 to SP1 are special function bits.

Fig. 4 RAM organization.

A user address in POCSAG code comprises 21 bits, three of which are coded in the frame number. In the PCA5000AT the frame number is common to both user addresses.

The special function bits are programmable to select from the following:

bit SP1: 0 alert-only-pager mode; silent override enabled on address 'B'
1 display-pager mode

SP2: 0 enable voltage converter (SP1 = 1)
1 disable voltage converter (SP1 = 1); cadence 1 also for FC = 11

SP3: 0 1-bit error-correction on message code words
1 4-bit burst error-correction on message code words on address 'B' (FC = 00 or 11)

SP4: free for user-application

SP5: 0 silent override enabled on address 'B' (FC = 01 or 10)
1 silent override enabled on address 'B' (FC = 00 or 11)

SP6: 0 silent override disabled on address 'A' (FC = 10)
1 silent override enabled on address 'A' (FC = 10)

The programming mode is entered by holding input PR at V_{DD} during power-on; exit from the programming mode is made by removing the main power supply. The back-up battery must remain connected to the PCA5000AT to keep the RAM contents when the main power supply is removed. During programming, inputs ON, OFF and SK must not all be '1' at the same time.

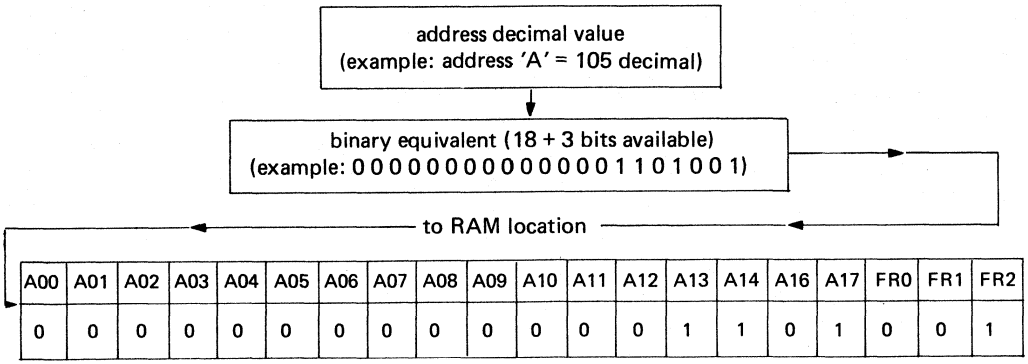
Programming of the RAM and verifying its contents is performed in a sequence starting with word 0, bit 0 and progressing through each of the five words in turn. Input and output is a serial operation; X1 is the shift clock input and DI, DO are respectively the data input and output.

During the RAM programming operation, a negative-going pulse first on WR and then on PR copies the 9 bits just shifted in into the RAM and switches to the next word (see Fig. 10).

During the RAM verify operation, reading the first word is triggered by a negative-going pulse on PR, which also switches to the next word in the sequence after 9 bits have been read (see Fig. 11).

Exit from the programming mode should be made after programming or verification of the RAM contents has been performed on all five words.

FUNCTIONAL DESCRIPTION (continued)



A00	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A16	A17	FR0	FR1	FR2
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1

Fig. 5 Example of bit conversion in user address programming.

Generation of output signals

Alerter interface

The alerter interface provides for the acoustic signalling of calls received (Fig. 8) and of changes of pager status (Fig. 9).

When valid calls are received and the pager is in the ON state, the decoder generates 2 kHz squarewave output signals to produce tone alert cadences via a magnetic or piezoceramic 2 kHz bleeper. The cadence signals differ in modulation according to the two function bits FC in the address code word (Fig. 6b). The PCA5000AT supports two levels of alerter loudness: during the first four seconds, cadences are generated at low intensity (output AL active, output QR inactive); during the following twelve seconds, the intensity is increased (outputs AL and QR both active).

The alert tone generation is automatically terminated after sixteen seconds. Alert cadences are also terminated by an ON, OFF or SILENT input when in alert-only-pager mode, or by pulsing the status/reset input in display-pager mode.

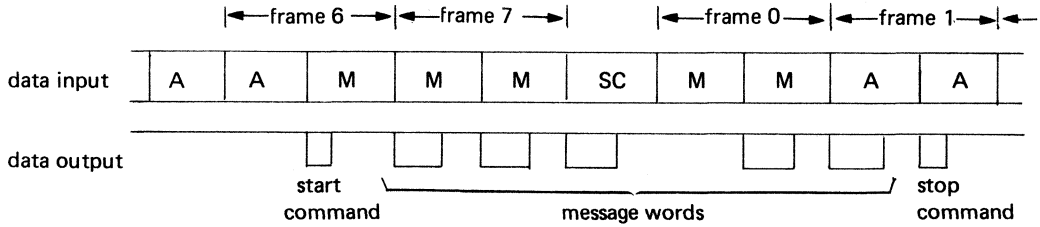
If the call is a message with subsequent message code words, alert cadence generation begins after the message has been terminated.

The alerter generates cadences to indicate the present internal status when interrogated and, when the main supply is low, gives a battery-low indicator output and generates an alarm tone.

Serial communication interface

This interface facilitates communication with an external microcontroller. Data is transmitted serially in the format shown in Fig. 6.

After receiving a valid address code word, transmission commences by sending a start command. The start command contains function data from the RAM, user address called (A or B) and function control bits FC from the address code word. The transmission continues with message words that contain the data from the received message code words. The end of a message transfer is marked by the sending of a stop command or another start command. In a stop command, bit 2 indicates that the call was successfully terminated.



a) Message format

bit

0	1	2	3	4	5	6	7
0	1	SP3	SP6	SP5	user address A or B	address bit 20 (FC)	address bit 21 (FC)

b) Start command format

bit

0	1	2	3	4 to 23
1	1	1	1	message code word bits 2 to 21 as received

c) Message word format

bit

0	1	2	3	4	5	6	7
0	0	successful termination	$\overline{QS}$ input	SP4	SP2	not used	not used

d) Stop command format

Fig. 6 Serial communication interface.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
V_{DD} is referred to as 0 V (ground)

parameter	symbol	min.	max.	unit
Supply voltage	$V_{SS} = V_{13-28}$	+ 0.5	−7.0	V
RAM back-up supply voltage	V_B	V_{SS} + 0.8	−6.0	V
Input voltage on pins ON, OFF, SK, AI, PC, FL, BL, DS, DO	V_I	0.8	V_{REF}−0.8	V
Input voltage on any other pin	V_I	0.8	V_{SS}−0.8	V
Power dissipation per output	P_O	–	100	mW
Total power dissipation	P_{tot}	–	250	mW
Operating ambient temperature range	T_{amb}	−10	+ 60	°C
Storage temperature range	T_{stg}	−55	+ 125	°C

CHARACTERISTICS: Alert-Only-Pager (SP1 = 0)

V_{DD} = 0 V; V_{SS} = −2.7 V; V_{REF} = −2.7 V; V_B = −3.0 V; T_{amb} = 25 °C; quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 12) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	−1.7	−2.7	−6.0	V
Operating supply current	all outputs open; all inputs at V_{SS}; voltage converter off	I_{SS}	–	–	−22.0	μA
Level at which RAM switches to V_B		$V_{SS(sw)}$	−1.2	–	−1.7	V
Supply current; peak value	AL = LOW	I_{SSM}	–	–	−45.0	mA
Input voltage LOW PR, DI, BS, QS, WR, TS		V_{IL}	0.7 V_{SS}	–	–	V
AI, ON, OFF, SK, PC		V_{IL}	0.7 V_{REF}	–	–	V
Input voltage HIGH PR, DI, BS, QS, WR, TS		V_{IH}	–	–	0.3 V_{SS}	V
AI, ON, OFF, SK, PC		V_{IH}	–	–	0.3 V_{REF}	V

CHARACTERISTICS: Alert-Only-Pager (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Input current						
PR, TS, BS	$V_I = V_{DD}$	I_I	7.0	–	18.0	μA
WR	$V_I = V_{SS}$	I_I	−9.0	–	−28.0	μA
DI	$V_I = V_{DD}$; $V_{RE} = V_{SS}$	I_I	6	–	16	μA
PR, TS, BS, DI, QS, PC	$V_I = V_{SS}$	I_I	–	–	−0.1	μA
WR, QS, PC	$V_I = V_{DD}$	I_I	–	–	0.1	μA
AI, ON, OFF, SK,	$V_I = V_{DD}$	I_I	6.0	–	16.0	μA
AI, ON, OFF, SK	$V_I = V_{SS}$	I_I	–	–	−0.1	μA
Input capacitance						
BS, DI, PR, WR, QS, TS		C_I	–	–	5	pF
AI, ON, OFF, SK, PC		C_I	–	–	5	pF
X1		C_I	–	–	5	pF
Output current LOW						
RE, OR, QR	$V_{OL} = -1.35$ V	I_{OL}	10.0	–	–	μA
DO, DS, BL, FL	$V_{OL} = -1.35$ V	I_{OL}	10.0	–	–	μA
AL	$V_{OL} = -1.5$ V	I_{OL}	17.5	–	41.5	mA
Output current HIGH						
RE	$V_{OH} = -1.35$ V	$-I_{OH}$	10.0	–	–	μA
OR, QR	$V_{OH} = -1.35$ V	$-I_{OH}$	10.0	540	750	μA
DO, DS, BL, FL	$V_{OH} = -1.35$ V	$-I_{OH}$	10.0	–	–	μA
AL	AL = high impedance	$-I_{OH}$	–	–	0.2	μA
Output capacitance						
X2		C_O	19	–	23	pF
Power-on reset threshold		V_{POR}	−1.10	–	−1.4	V

CHARACTERISTICS: Display-pager; alphanumeric mode (SP1 = 1, SP2 = 1)

CN and CP open circuit;
$V_{DD} = 0$ V; $V_{SS} = -3.0$ V; $V_{REF} = -6.0$ V; $T_{amb} = 25$ °C; quartz crystal f = 32.768 kHz, $R_{Smax} = 40$ kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	−1.7	–	−3.0	V
Microcontroller interface negative reference		V_{REF}	V_{SS}	–	−6.0	V
Input current AI, ON, OFF, SK	$V_I = V_{REF}$ or V_{DD}	I_I	–	–	0.1	μA

DEVELOPMENT DATA

CHARACTERISTICS: Display-pager; numeric mode (SP1 = 1, SP2 = 0)

220 nF capacitor connected to CN, CP;
V_{DD} = 0 V; V_{SS} = −3.0 V; T_{amb} = 25 °C;
quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	−1.7	–	−3.0	V
Voltage converter V_{REF} output: output voltage	V_{SS} = −3.0 V; no load	V_{REF}	−5.95	–	−6.0	V
	V_{SS} = −2.0 V; I_{VREF} = 150 μA; PC = 0	V_{REF}	−2.7	–	–	V
	V_{SS} = −2.0 V; I_{VREF} = 45 μA; PC = 1	V_{REF}	−2.7	–	–	V
output current	V_{SS} = −2.0 V; PC = 0	I_{VREF}	−150	–	–	μA
	V_{SS} = −2.0 V; PC = 1	I_{VREF}	−45	–	–	μA
Input current AI, ON, OFF, SK	V_I = V_{REF} or V_{DD}	I_I	–	–	0.1	μA

TIMING: Display-pager (SP1 = 1)

V_{DD} = 0 V; V_{SS} = −2.7 V; T_{amb} = 25 °C;
quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator frequency		f_{osc}	–	32.768	–	kHz
Alerter frequency		f_{alert}	–	2048	–	Hz
Data input rate		f_{DI}	–	512	–	bits/s
Frequency reference FL output		f_{FL}	–	16.384	–	kHz
Data input transition time		t_{TDI}	–	–	100	μs
Preamble duration			1125	–	–	ms
Batch duration		t_{BAT}	–	1062.5	–	ms
Bit period		t_{BIT}	–	1.9531	–	ms
Data output rate		f_{DO}	–	512	–	bit/s
Data output transition time	C_L = 5 pF	t_{DTO}	–	–	100	ns
Data strobe clock period		t_{DS}	–	1.9531	–	ms
Data output set-up time		t_{DOS}	–	1.77	–	ms
Data strobe pulse width		t_{DSW}	61	122	–	μs
Data hold time		t_{DH}	30.5	61	–	μs
Call alert period		t_{ALT}	–	16	–	s
Call alert (low level) AL output only		t_{ALL}	–	4.0	–	s
Call alert (high level) QR and AL outputs		t_{ALH}	–	12.0	–	s

parameter	conditions	symbol	min.	typ.	max.	unit
Call alert cycle period		t_{ALC}	–	1.0	–	s
Call alert pulse period		t_{ALP}	–	125	–	ms
Status pulse set-up time		t_{STP}	10.0	330	–	μs
Status pulse duration		t_{STD}	10.0	330	–	μs
Status alert period		t_{STON}	–	62.5	–	ms
Status alert delay		t_{STOF}	–	62.5	–	ms
Receiver control RE transition time	C_L = 5 pF	t_{RXT}	–	–	100	ns
RE establishment time		t_{RXON}	–	31.2	–	ms
Programming:						
data clock period		t_{PDC}	–	100	–	μs
data settling time		t_{PDS}	20.0	–	–	μs
write set-up time		t_{WSU}	20.0	–	–	μs
write pulse width		t_{WP}	10.0	–	–	μs
program input pulse width		t_{PR}	10.0	–	–	μs
program input settling time		t_{PRS}	20	–	–	μs
Power-on reset pulse width		t_{POR}	7.5	–	–	μs
Program start delay time		t_{CSU}	20.0	–	–	μs
Program data hold time		t_{PDE}	10.0	–	–	μs
Data clock period LOW		t_{X1}	10.0	50.0	–	μs

DEVELOPMENT DATA

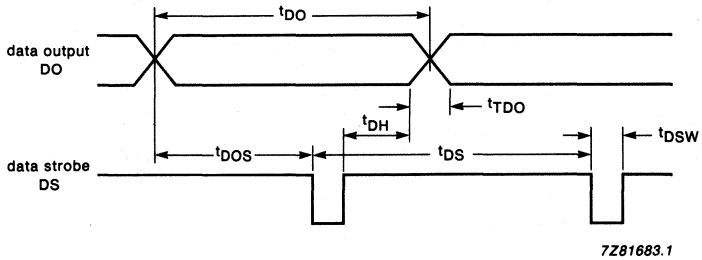


Fig. 7 Serial communications interface timing.

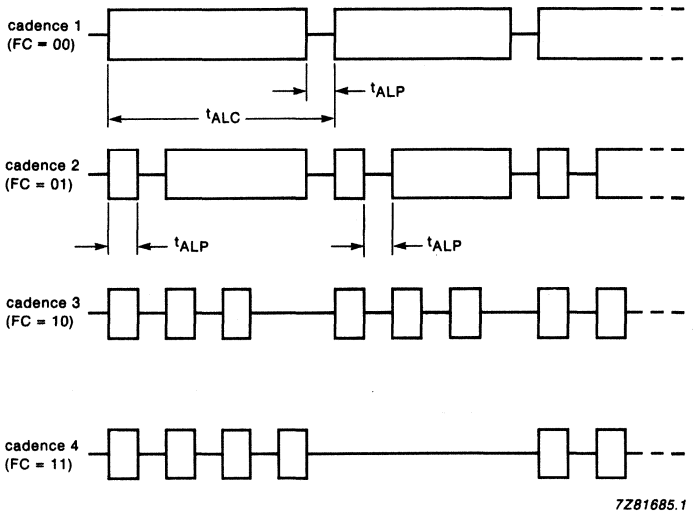


Fig. 8 Call alert cadences; FC refers to function control bits 20 and 21 in the address code word.

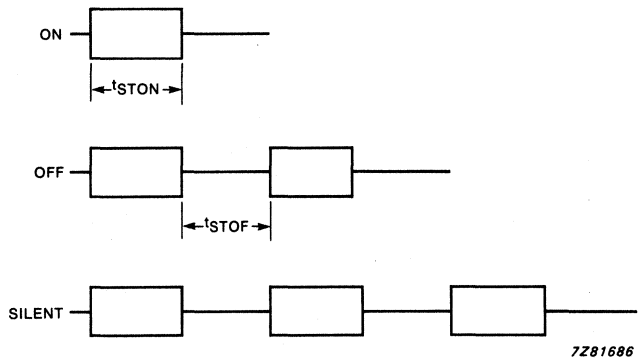


Fig. 9 Status indication cadences.

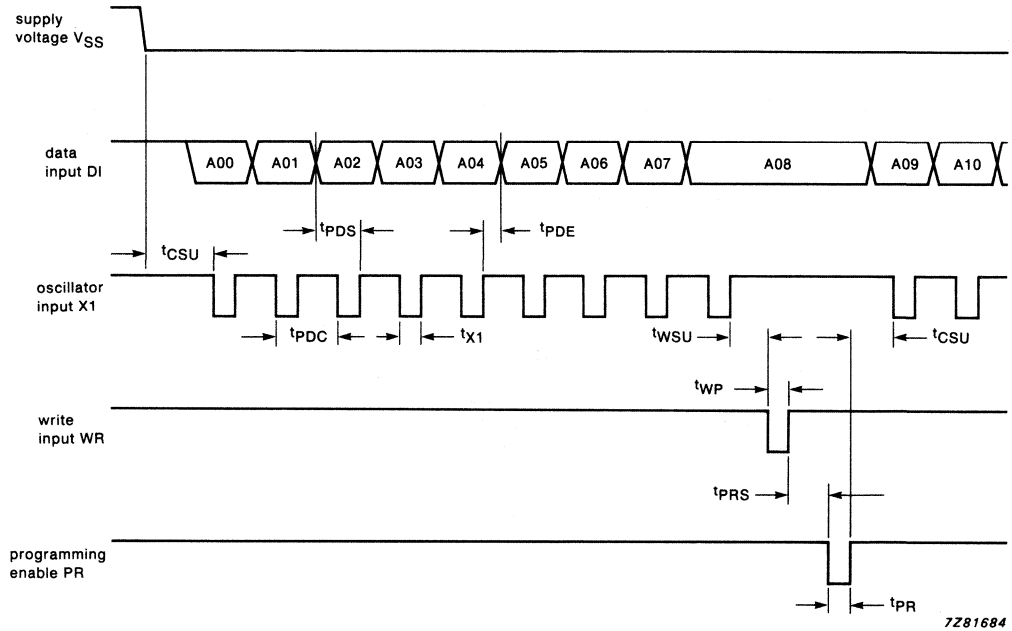


Fig. 10 Timing of RAM programming operation.

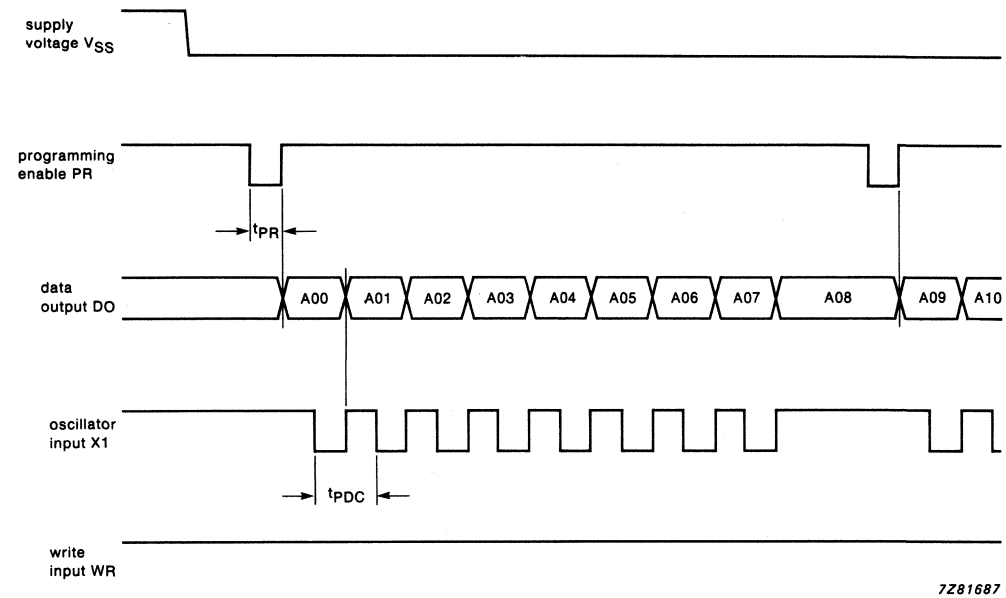


Fig. 11 Timing of RAM verify operation.

DEVELOPMENT DATA

APPLICATION INFORMATION

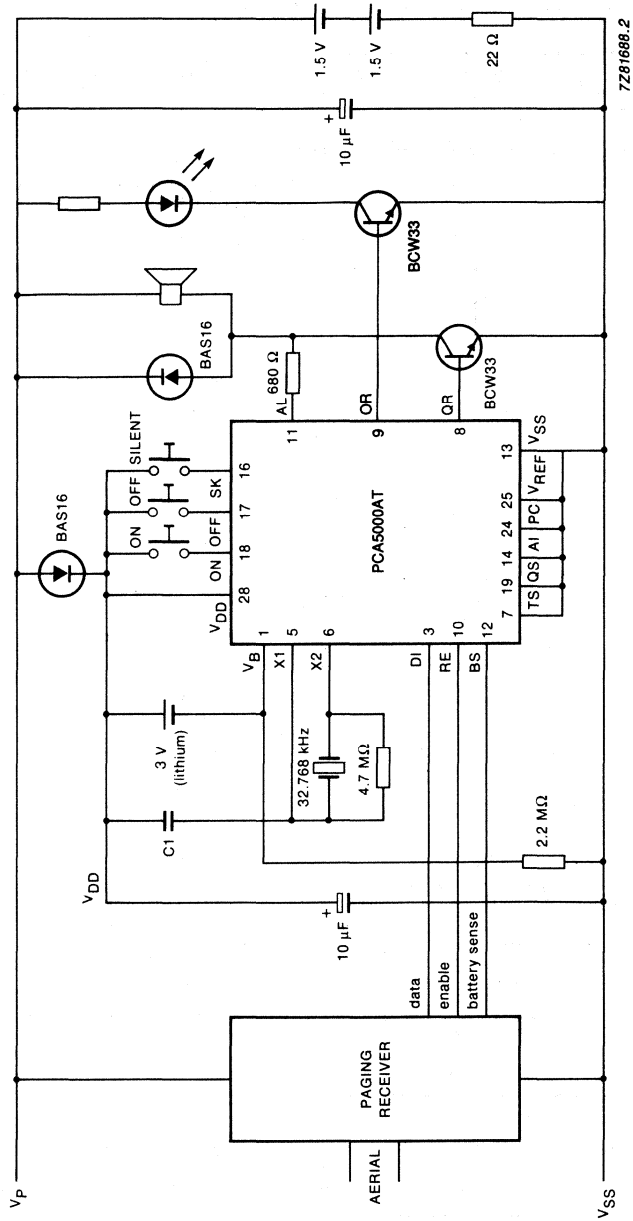


Fig. 12 Example of alert-only pager.

DEVELOPMENT DATA

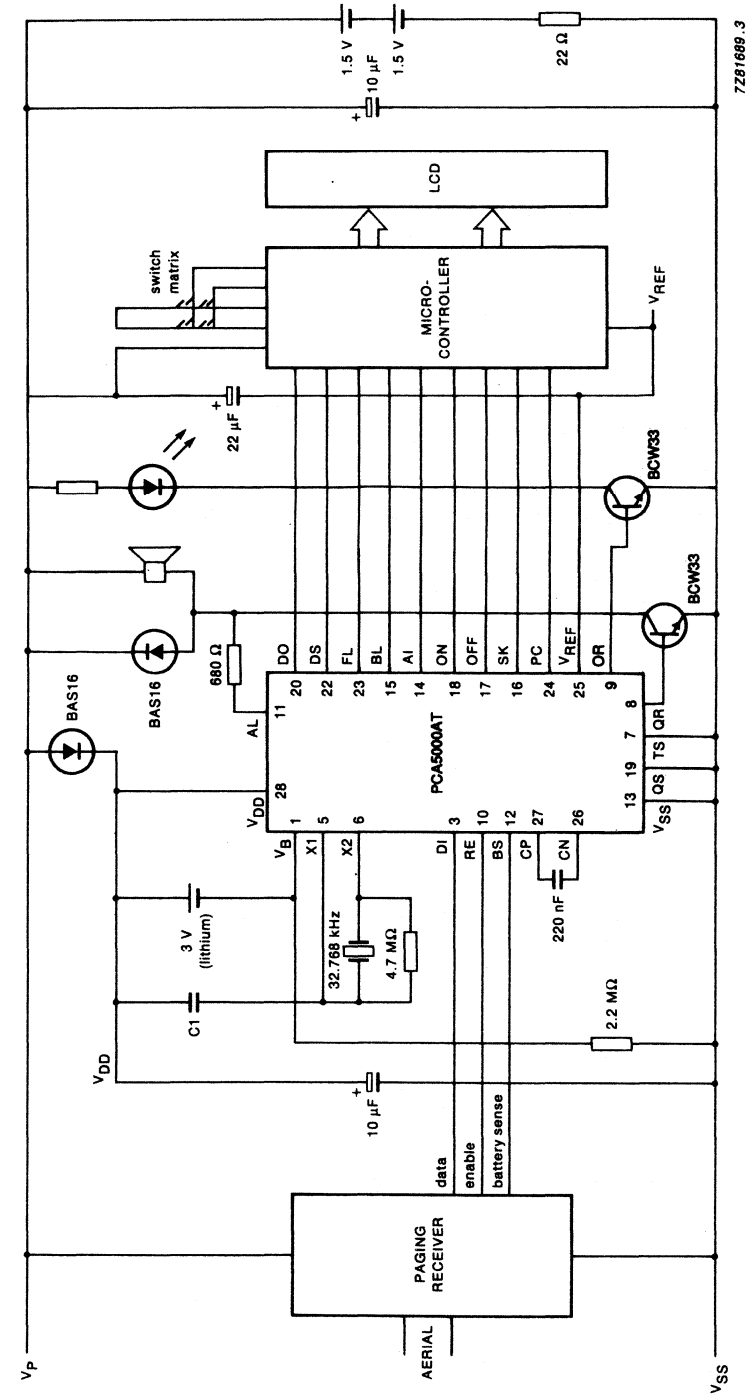


Fig. 13 Example of display-pager in alphanumeric mode with voltage converter enabled.

Application notes

Input pins

The programming control inputs have internal biasing resistors of sufficiently low impedance to provide safe operation even if the pins are left open circuit.

Pin 1 (V_B): RAM back-up battery negative supply. Connect this pin to the negative terminal of a lithium battery and connect the positive battery terminal to V_{DD}. This battery supply ensures data retention when the main supply voltage is removed.

Pin 2 (PR): programming enable, normally LOW. To enter the programming mode, pull this input HIGH when connecting the main supply voltage.

Pin 3 (DI): serial data input. During normal operation, POCSAG-coded data is received via this pin. When in programming mode, data to be stored in the internal RAM is read from this input whenever a pulse on X1 occurs.

Pin 4 (WR): programming write input, normally HIGH. A positive edge on this pin copies the preceding word shifted into the internal RAM. Keep this pin HIGH during RAM-read operations.

Pin 5 (X1): oscillator input. Connect a 32 kHz crystal to this pin during normal operation. When in programming write mode, a positive edge on X1 shifts the data present on DI to the internal register. When in programming read mode, a positive edge on X1 moves the next bit from the internal register to DO.

Pin 6 (X2): oscillator output. Return connection to the 32 kHz crystal.

Pin 7 (TS): test mode enable input, **always** LOW.

Pin 12 (BS): battery sense input. The decoder samples this input when it is in the ON state and the receiver is enabled. Every single sample is copied to the BL output. A continuous high-level alert tone is generated if four sequential samples are HIGH.

Pin 13 (V_{SS}): main negative supply voltage. Remove the voltage from this pin to leave the programming mode. The RC combination of 22 Ω and 10 μF (Figs 12 and 13) should remain connected; disconnect the battery only.

Pin 14 (AI): alarm input, normally LOW. A HIGH on this input causes a continuous high-level alert tone to be generated. The input may be pulsed to modulate the output tone.

Pin 16 (SK): silent key/mute input.
Alert-Only-Pager: push-button switch input, pushing the switch selects SILENT state.
Display-Pager: static input, when HIGH no calls are stored and no alert tones are generated for calls received.

Pin 17 (OFF): off key/reset input.
Alert-Only-Pager: push-button switch input, pushing the switch selects OFF state.
Display-Pager: static input, normally LOW. A positive-going pulse on this input causes (a) status indication cadences to be generated if the decoder is not alerting or (b) resetting an alert call or a battery-low alert if active.

Pin 18 (ON): on key/on-off input.
Alert-Only-Pager: push-button switch input. Pushing the switch selects ON state.
Display-pager: static input. LOW level selects OFF state, HIGH level selects ON state.

Pin 19 (QS): vibrator enable input, normally LOW. A HIGH level enables the vibrator output logic and switches QR to vibrator output.

Pin 24 (PC): voltage converter power control. The level on this pin determines the output impedance of the voltage converter. LOW selects low impedance, HIGH selects high impedance.

Pin 26 (CN): voltage converter external capacitor, negative connection.

Input pins (continued)

Pin 27 (CP): voltage converter external capacitor, positive connection.

Pin 28 (V_{DD}): main positive supply input. This pin is common to all supply voltages and is referred to as GROUND.

Output pins

Pin 8 (QR): alert high-level output/vibrator output. This output can directly drive an external bipolar transistor to control a vibrator-type alerter if QS is set HIGH, or supports high-level alerting in conjunction with AL.

Pin 9 (OR): out-of-range output, active HIGH. If the decoder detects 'carrier-off', an output is generated for the duration of the synchronization scan period. Connecting OR to QR provides alert tone generation during 'carrier-off'.

Pin 10 (RE): receiver enable output, active HIGH. Connect the radio paging receiver power control input to this pin to minimize power consumption. Whenever no input data is required, the PCA5000AT will disable the paging receiver to conserve power.

Pin 11 (AL): alert low-level output, active LOW. The low-level alert tone is generated via this output; the alert becomes high-level in conjunction with QR.

Pin 15 (BL): battery-low output, active HIGH. Every time the PCA5000AT samples the BS input, data sensed is output on this pin.

Pin 20 (DO): received data output. During normal operation, accepted calls and possibly subsequent message code words are output via this pin at a rate of 512 bits/s. When in programming read mode, data read from the internal RAM is presented bit-by-bit on this pin.

Pin 22 (DS): received data strobe output, active LOW. In normal operation, every time this output goes LOW, the next bit on the DO output is valid.

Pin 23 (FL): frequency reference output. If the decoder is programmed as a Display-Pager, a 16 kHz squarewave reference is output from this pin.

Pin 25 (V_{REF}): microcontroller interface negative reference voltage. The LOW level of pins FL, BL, DO, DS, AI, ON, OFF, SK and PC is related to the voltage on V_{REF}.
Alert-Only-Pager: Connect V_{REF} output to V_{SS}.
Display-Pager: The doubled negative supply voltage generated by the internal voltage converter is output from V_{REF}. The V_{REF} pin may also be driven from an external supply if the capacitor across CN/CP is removed and CN/CP are left open circuit.

DEVELOPMENT DATA

SINGLE-CHIP DIGITAL SIGNAL PROCESSOR

HOW TO USE THIS DATA SHEET

- **Section 1** contains ordering information and the main features of the PCB5010 and PCB5011.
- **Section 2** describes the signals of the PCB5010 and PCB5011, with block diagrams and full descriptions of what functions can be performed by each block.
- **Section 3** describes how the blocks are controlled by the instructions given by the programmer. This section is used during programming, it assumes however, a full knowledge of section 2.0. Programming can be simplified by using the software tools available.
- **Section 4** describes all the electrical characteristics.
- **Section 5** gives details of the PCB5010 and PCB5011 packages.

CONTENTS

1.0 INTRODUCTION

The PCB5010 and PCB5011 are part of our SP 50 family of digital signal processors that contains devices for various applications. These CMOS devices have a common processor structure and are accompanied by a common set of development tools.

The processor structure is characterized by two separate data buses, a two operand hardware multiply/accumulate unit and a two operand ALU to improve throughput. Powerful parallel and serial interfaces enable communication with external devices. Large on-chip data memories, each with its own programmable address computation unit (ACU), offer the possibility to make systems with only a few components.

The PCB5010 and PCB5011 are the optimal solutions for implementing DSP functions in telecommunications, and can also be used to advantage in speech processing, high-speed control, image processing and many other fields.

- PCB 5010: Version with on-chip ROM (mask programmable)
- PCB 5011: ROMless bond-out version, for use with external program/data memory

DEVELOPMENT DATA

ORDERING INFORMATION

order number	speed (MHz)	operating ambient temperature (°C)	package
PCB5010WP-8	8.2	0 to +70	68-pin PLCC
PCF5010WP-8*	8.2	−40 to +85	68-pin PLCC
PCB5011YC-8	8.2	0 to +70	144 PGA
PCF5011YC-8*	8.2	−40 to +85	144 PGA

* The PCF versions will be identical to the PCB versions except that they have an extended operating ambient temperature range. However, minor variations may occur in the AC/DC characteristics.

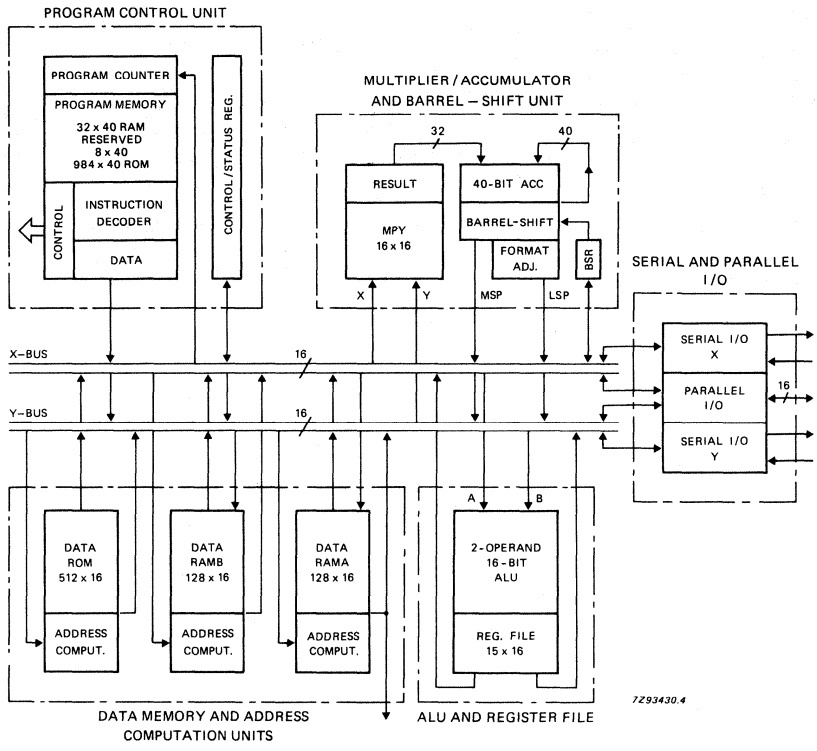


Fig. 1.0-1 Simplified block diagram of the PCB5010.

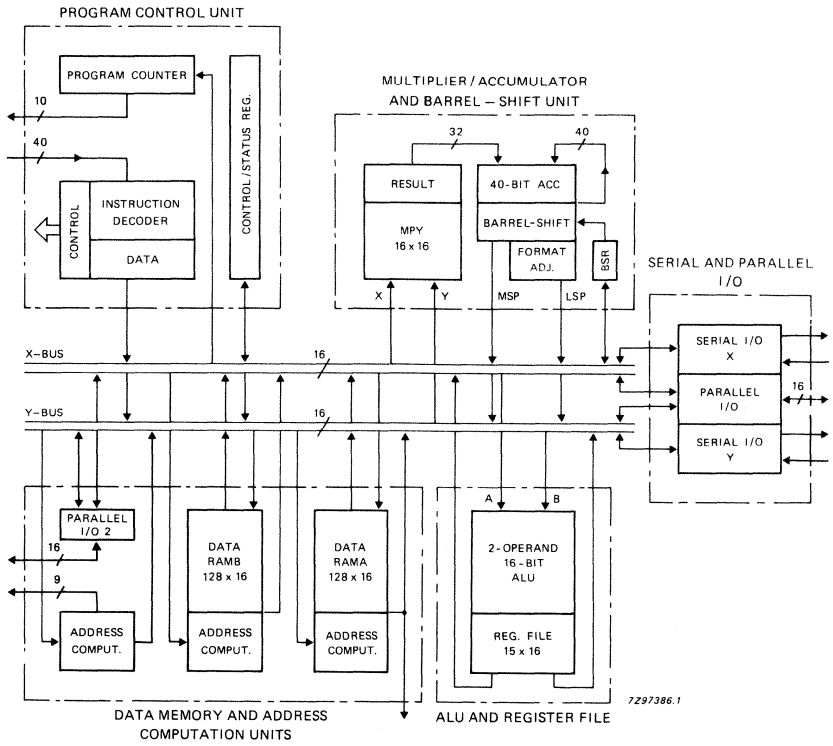


Fig. 1.0-2 Simplified block diagram of the PCB5011.

FEATURES

- Harvard architecture with two data buses of 16 bit width
- 4 instruction types:
  - multiply/accumulate operation + 2 data moves + 3 address calculations/ memory read accesses
  - alu operation + 2 data moves + 3 address calculations/ memory read accesses
  - load immediate data + 3 address calculations/ memory read accesses
  - branch + 3 address calculations/ memory read accesses

  Note: a high degree of parallel processing allows up to 6 basic operations to be performed simultaneously.
- Hardware two's complement 16 x 16 multiplier with 40-bit accumulator, full range barrel-shifter and format adjuster:
  - 45 different multiply/accumulate operations
  - multi-precision multiplication support
  - result bit-reversal possibility
  - 4 status flags
- 16-bit 2-operand ALU with:
  - 31 different operations
  - multi-precision operation support
  - 15 x 16-bit 3-port register-file
  - 5 status flags
- Program memory:
  PCB5010: 984 x 40-bit on-chip ROM (mask programmable)
  32 x 40-bit on-chip RAM (loaded via the X-bus)
  PCB5011: no on-chip program memory, but may be connected to a 1024 x 40-bit external memory
  (64K x 40-bit, by adding external logic circuitry)
- Data memory:
  PCB5010: 512 x 16 bit on-chip ROM (mask programmable)
  2 x (128 x 16) on-chip static RAM
  PCB5011: 512 x 16 bit external memory (read and write possible)
  2 x (128 x 16) on-chip static RAM
- 3 powerful programmable address computation units (ACU's) for the data ROM and both data RAMs and also for 16 pages of 4096 x 16 bit external data memory
  - each ACU has 8 different operations
  - 1 status flag for each ACU
- 5 level deep hardware stack (software extendable)
- 16-bit parallel I/O to access external data memory
  - 8.2 million words/s
  - WAIT facility so that "slow" peripherals can be connected
- 2 independent serial inputs and outputs (one pair for each data bus), with a maximum speed of 4.1 million bit/s under the control of external clocks
- 4 user input flags
- Maskable interrupt
- Possibility to repeat a single instruction
- Maximum clock rate 8.2 MHz
- Pipelined (P) and Non-pipelined (NP) modes under programmer control:
  P-mode: a new instruction can start every clock cycle
  NP-mode: a new instruction can start every two clock cycles
- Single 5 V power supply (±5%)
- All I/O are TTL compatible
- Operating ambient temperature range:
  PCB5010/11: 0 to +70 °C
  PCF5010/11: −40 to +85 °C

DEVELOPMENT DATA

2.0 FUNCTIONAL DESCRIPTION

2.1 GENERAL DESCRIPTION

The detailed block diagram of the PCB5010 and PCB5011 are shown in Fig. 2.1-1 and Fig. 2.1-2. The signals of the processors are described briefly in Table 2.1-1.

Table 2.1-1 Signal description

SIGNAL	I/O	DESCRIPTION
V_{DD}	I	Supply voltage: 5 V ± 5%
V_{SS}	—	Ground
CLK	I	Clock
$\overline{RST}$	I	Reset
D15 . . . D0	I/O	16-bit wide parallel I/O port
A15 . . . A0	O	16-bit wide address for 64K-words in external data memory
R/$\overline{W}$	O	Read/write signal for control of external memory
$\overline{DS}$	O	Data strobe
$\overline{WAIT}$	I	Wait signal for synchronization of parallel I/O
DIX	I	Serial data input for the X-bus
$\overline{SIXEN}$	I	Serial input enable for the X-bus
$\overline{SIXRQ}$	O	Serial input request for the X-bus
CIX	I	Serial input clock for the X-bus
DIY	I	Serial data input for the Y-bus
$\overline{SIYEN}$	I	Serial input enable for the Y-bus
$\overline{SIYRQ}$	O	Serial input request for the Y-bus
CIY	I	Serial input clock for the Y-bus
DOX	O	Serial data output for the X-bus
$\overline{SOXEN}$	I	Serial output enable for the X-bus
$\overline{SOXRQ}$	O	Serial output request for the X-bus
COX	I	Serial output clock for the X-bus
DOY	O	Serial data output for the Y-bus
$\overline{SOYEN}$	I	Serial output enable for the Y-bus
$\overline{SOYRQ}$	O	Serial output request for the Y-bus
COY	I	Serial output clock for the Y-bus
$\overline{INT}$	I	Maskable interrupt
$\overline{IACK}$	O	Interrupt acknowledge
SYNC	O	Synchronization signal; indicates where execution of a new instruction starts
IFA	I	User flag
IFB	I	User flag
IFC	I	User flag
IFD	I	User flag

(continued on next page)

Table 2.1-1 (continued)

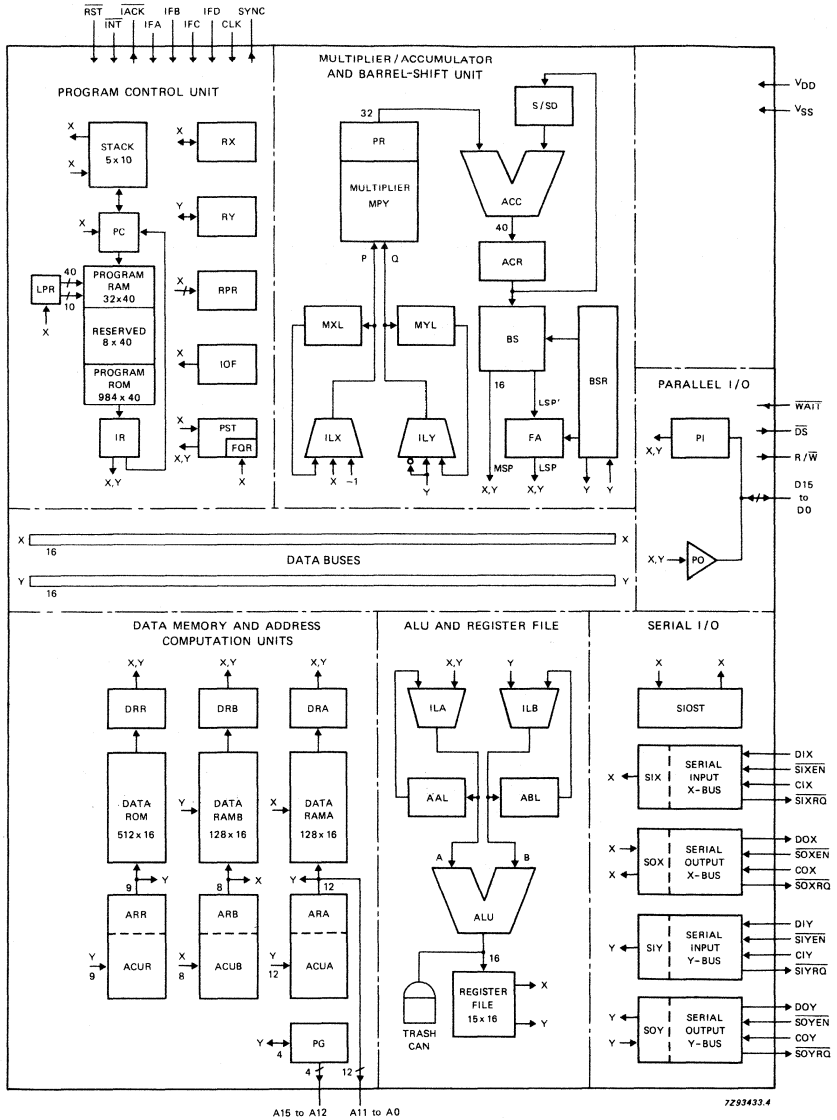
MNEMONIC	I/O	DESCRIPTION
PCB5011 only:		
PA9 . . . PA0	O	External program memory address
PD39 . . . PD0	I	External program word
ARR8 . . . ARR0	O	9-bit address for 512 words in external data memory
RD15 . . . RD0	I/O	Second 16-bit parallel I/O port
RR/$\overline{W}$	O	Read/write signal for second 16-bit parallel I/O port
$\overline{RDS}$	O	Data strobe for second 16-bit parallel I/O port

The main blocks of PCB5010/11 are:

- Program control unit with:
  - Program ROM (only for PCB5010)
  - IR (instruction register)
  - Sync pin
  - PC (program counter)
  - RPR (instruction repeat register)
  - Stack
  - PST (processor status register)
  - IOF (input/output status and user flag register)
  - User flag pins
  - $\overline{INT}$ pin and $\overline{IACK}$ pin
  - Bus-save registers RX and RY
  - $\overline{RST}$ pin
  - External program memory port (only PCB5011)
  - External program memory address port (only PCB5011)
- Data memory and address computation units with:
  - RAMA, ACUA (address computation unit A), DRA (data register A)
  - PG (page register)
  - RAMB, ACUB (address computation unit B), DRB (data register B)
  - ROM (only PCB5010), ACUR (address computation unit R), DRR (data register R)
  - External data word pins (only PCB5011)
  - External data memory address pins (only PCB5011)
- Multiplier/accumulator and barrel-shift unit with:
  - Input selectors ILX and ILY
  - Latches MXL and MYL
  - MPY (multiplier)
  - Accumulator with ACC (adder), ACR (multiplication/accumulation register) and S/SD (sign/scale-down block)
  - BS (barrel-shifter)
  - FA (format adjuster)
  - BSR (barrel-shift and format adjust control register)
- ALU and register file with:
  - Input selectors ILA and ILB
  - Latches AAL and ABL
  - ALU (arithmetic logic unit)
  - R1-R15 (register file)
  - Trash can
- Parallel I/O with:
  - PI (parallel data input latch)
  - PO (parallel data output buffer)
  - Parallel I/O data and control pins
- Serial I/O with:
  - SIX (serial input latch connected to X-bus)
  - SOX (serial output latch connected to X-bus)
  - SIY (serial input latch connected to Y-bus)
  - SOY (serial output latch connected to Y-bus)
  - SIOST (serial I/O control register)
  - Serial I/O data and control pins
- Data buses with:
  - 16 bits X-bus
  - 16 bits Y-bus

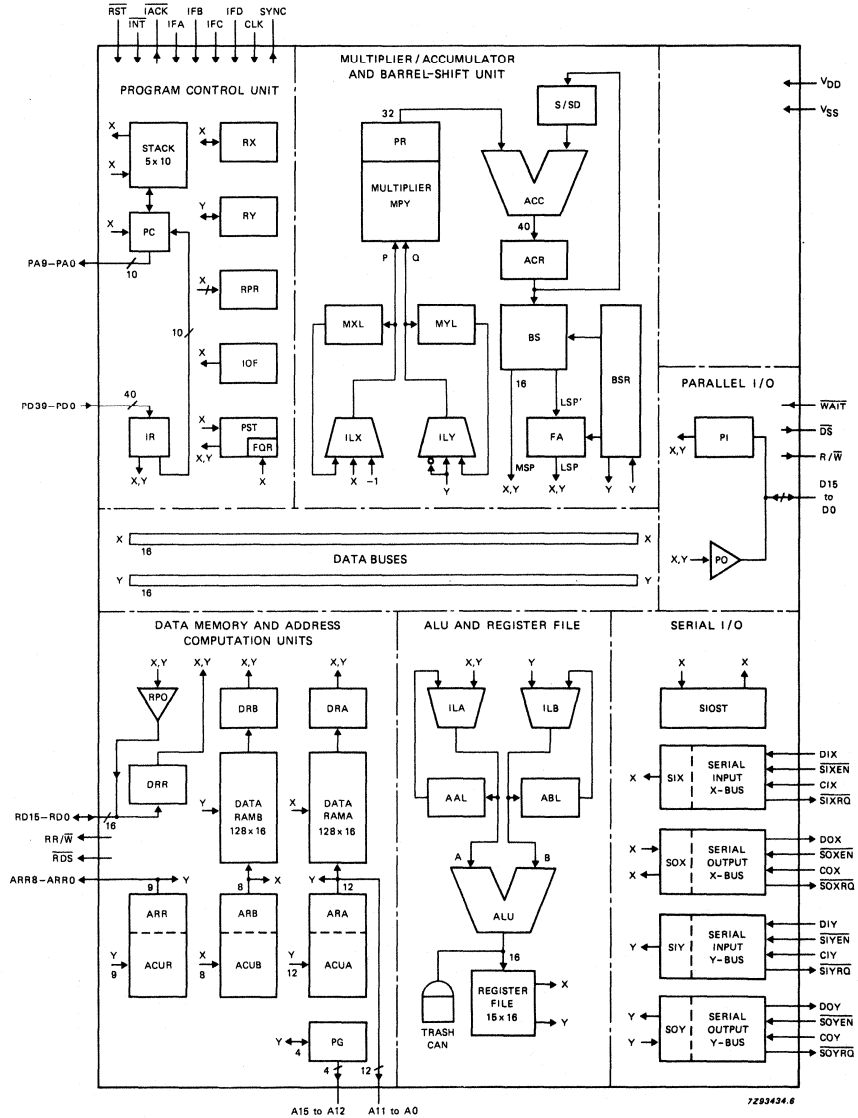
The functions of the main blocks are described in the following sections. The instruction set is described in the section 3.0.

DEVELOPMENT DATA



X,Y
Note 1: ↑ means connected to the X-bus/Y-bus.
Note 2: all data paths are 16 bits wide unless indicated otherwise.

Fig. 2.1-1 Detailed block diagram of the PCB5010.



X,Y

Note 1: ↑ means connected to the X-bus/Y-bus.

Note 2: all data paths are 16 bits wide unless indicated otherwise.

Fig. 2.1-2 Detailed block diagram of the PCB5011.

2.2 PROGRAM CONTROL UNIT

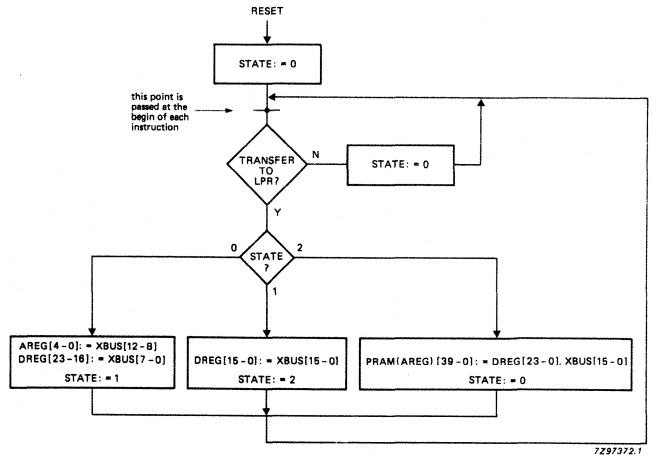
2.2.1 Program memory

The PCB5011 has no on-chip program memory but may be connected to an external program memory. To access the external program memory, there are 40 program data pins (PD39-PD0) and 10 program address pins (PA9-PA0). The contents of the on-chip 10 -bit program counter are available via these address pins.

The PCB5010 has 1K x 40-bit on-chip program memory:

- 984 x 40-bit mask programmable ROM (address 0-983)
- 32 x 40-bit static RAM (address 992-1023)
- 8 x 40-bit reserved for test purposes (address 984-991)

The memory is addressed by the 10-bit on-chip program counter. The static RAM of the program memory can be loaded via the X-bus by MOVE or LOAD IMMEDIATE operations, following the procedure described in the section 2.2.2 "Load program RAM circuitry".



AREG = address register
DREG = data register
PRAM(i) = position i in the program RAM
[m – n] = bit m to bit n

Fig. 2.2.2-1 Program RAM loading procedure.

2.2.2 Load program RAM circuitry (LPR)

LPR enables the programmer to load the 32 x 40-bit program RAM. To load each 40-bit instruction, three 16-bit words must be transferred to LPR via the X-bus, using MOVE or LOAD IMMEDIATE operations. LPR contains a 5-bit address register (AREG) in which the load address (range 0-31) is loaded and it contains a 24-bit data register (DREG) in which the instruction word is assembled. The loading procedure is shown in Fig. 2.2.2-1.

2.2.3 Program counter (PC) and mode circuitry (P and NP-mode)

The 10-bit program counter in the PCB5010 and PCB5011 is automatically incremented every instruction cycle during sequential program flow.

There are however, certain situations when the program counter is not incremented but updated differently:
- reset (see section 2.2.10)
- interrupt (see section 2.2.9)
- instruction repetition (see section 2.2.6)
- branch operations (see section 2.2.7)
- loading PC via the X-bus by means of a MOVE or LOAD IMMEDIATE operation (the 10 least significant bits of the X-bus data are loaded)

The processors work in two different modes:
1. Pipelined mode (P):
   instruction cycle = one clock cycle
2. Non-pipelined mode (NP):
   instruction cycle = two clock cycles

When the processor works in the P-mode, the result of a basic operation (see section 3.1 on instruction set) is not always available after the first instruction cycle but sometimes one clock cycle later. Since the processor uses pipelining, a new operation can start before the result of the previous operation is available. When the processor operates in NP-mode, the result of a basic operation is always available at the end of an instruction cycle. On reset, the processor is placed in the P-mode. Mode switching is possible under program control by setting and resetting the FQR bit in the PST register using a MOVE or LOAD IMMEDIATE operation. The instruction after the one that caused the change in the FQR bit is executed in the new mode. Return from an interrupt or a subroutine should be performed in the mode in which it was entered.

2.2.4 Instruction register (IR)

In every instruction cycle (i.e. every clock cycle when working in the P-mode and every two clock cycles when working in the NP-mode) an instruction word is fetched from the program memory. The program memory access and storing of the result in the instruction register (IR) takes one clock cycle. During the next clock cycle, the new contents of the IR is decoded and the processor controlled accordingly.

2.2.5 Stack

When an interrupt or subroutine call occurs, the value of PC (in the P-mode) or the value of PC+1 (in the NP-mode) is placed on the stack. The stack is a 5 x 10-bit LIFO register file that allows automatic nesting up to five levels of subroutines and/or interrupts. The top of the stack containing the most recent PC value can be accessed via the data buses. This enables the programmer to extend the stack in the data memory.

2.2.6 Instruction repeat circuitry (RPR)

RPR is a register that can be loaded via the X-bus with a number N by a MOVE or LOAD IMMEDIATE operation. The following instruction is then executed N times as long as $2 \leqslant N \leqslant 255$. The execution count is undefined when $N < 2$ or $N > 255$. The repetition of instructions by using the RPR is forbidden for the following operations:
- Load PC
- Load RPR
- Change of FQR bit in the PST
- Branch operations

2.2.7 Branch circuitry

The PCB5010 and PCB5011 make it possible to depart from the sequential program flow under software control. There are 4 branch types, and each branch can depend on any one of 50 different conditions.

The 4 branch types are:
- go to
- subroutine call
- return from subroutine
- return from interrupt.

The 50 branch conditions are the true and false status of the following flags or combination of flags:
- ALU flags: Z, N, C, $\overline{C.OR.Z}$, V, VL, $\{N.XOR.V\}.OR.Z$, $\overline{N.XOR.V}$
- Accumulator flags: SGNM, OVFL
- Barrel-shifter flags: OOR, OORL
- ALU and barrel-shifter flags: OORL.OR.VL
- ACU flags: ACA, ACB, ACR
- User flags: IFA, IFB, IFC, IFD, IFA.AND.IFB.AND.IFC.AND.IFD
- Serial I/O flags: SIXACK, SIYACK, SOXACK, SOYACK

2.2.8 The PST and IOF registers (PST, IOF, IFA – IFD pins)

PST and IOF are 16-bit registers that contain all the flags. Furthermore, PST also contains a bit (EI) that indicates whether the interrupt is enabled or not (enabled = 1; disabled = 0), a bit (FQR) indicating which mode (P = 0 or NP = 1) the processor is working in, and two bits (PIO1 and PIO2) determining the input criteria for the parallel input. The definition of each bit of PST and IOF registers is given in Table 2.2.8-1.

Table 2.2.8-1 PST and IOF registers; bit definition

bit	PST register		IOF register	
00	OVFL	(accumulator flag)	SIXACK	(serial I/O flag)
01	OORL	(barrel-shifter flag)	SOXACK	(serial I/O flag)
02	VL	(ALU flag)	SIYACK	(serial I/O flag)
03	V	(ALU flag)	SOYACK	(serial I/O flag)
04	C	(ALU flag)	IFA	(user flag)
05	Z	(ALU flag)	IFB	(user flag)
06	N	(ALU flag)	IFC	(user flag)
07	OOR	(barrel-shifter flag)	IFD	(user flag)
08	SGNM	(accumulator flag)	reserved	
09	ACA	(ACU flag)	reserved	
10	ACB	(ACU flag)	reserved	
11	ACR	(ACU flag)	reserved	
12	PIO2	(parallel I/O flag)	reserved	
13	PIO1	(parallel I/O flag)	reserved	
14	EI	(interrupt enable/disable)	reserved	
15	FQR	(operation mode)	reserved	

The flags in PST and IOF reflect the status of the functional units to which they belong and they are updated during each relevant instruction. The flags IFA, IFB, IFC and IFD reflect the signal level on their respective input pins. "Lock" type flags (OVFL, OORL and VL) can only be changed from 0 to 1 by the functional units to which they belong. The programmer can overrule the functional units updating the flags in the PST register: the PST register can be overwritten using a MOVE or LOAD IMMEDIATE operation. These operations are also used for loading the EI, FQR, PIO1 and PIO2 bits. Furthermore, the programmer can load the FQR bit using a MOVE or LOAD IMMEDIATE operation without changing the other bits in the PST register.

The PST and IOF register can be read using a MOVE operation. The flags can also be used as conditions in BRANCH operations (see section 2.2.7 on BRANCH circuitry). "Lock" type flags will automatically be reset to 0 when they are tested in a BRANCH operation.

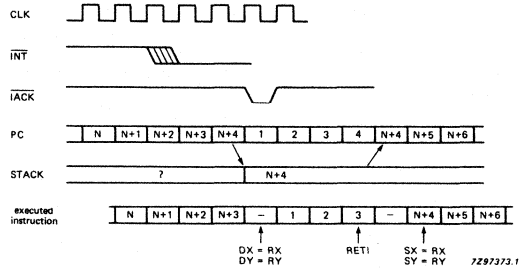
2.2.9 Interrupt circuitry ($\overline{INT}$ and $\overline{IACK}$ pins, RX and RY)

The processor has an interrupt facility that the user can access via the $\overline{INT}$ and $\overline{IACK}$ pins. When an interrupt is accepted by the processor the program counter is loaded with address 1. The interrupt procedure is described below and the logic timing diagrams are given in Figures 2.2.9-1 and 2.2.9-2.

An interrupt is initiated by a LOW on the $\overline{INT}$ pin. The first positive-going edge of CLK after a HIGH-to-LOW transition on $\overline{INT}$, the interrupt is clocked in by the processor. Two or three clock pulses later (see timing diagrams), the processor decides to accept the interrupt or postpone it. An interrupt is postponed:

- while the PC is being loaded (as part of a BRANCH, MOVE or LOAD IMMEDIATE operation)
- while the RPR register is loaded
- during instruction repetition
- when the stack is the source or destination to the X-bus
- when the interrupt is disabled by software (EI bit in PST register is 0).
- P-mode only: when RX or RY store data without having read it (MOVE or RETI BRANCH operations) after storing.

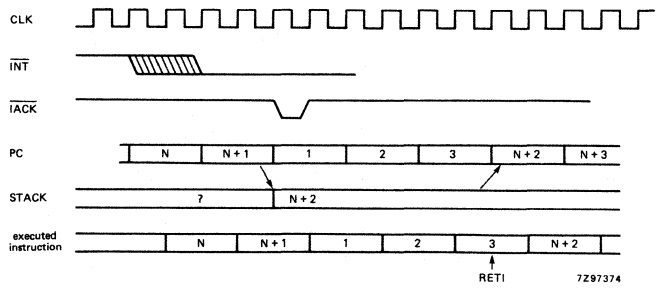
As soon as the above situations are completed, the postponed interrupt is accepted and thereafter handled in the same way as an interrupt that was accepted directly.



Note 1: The interrupt is postponed when one of the following conditions is true during instruction N + 3:
- loading of PC (as part of BRANCH or MOVE operation)
- loading of RPR
- stack source or destination to X-bus
- repetition mechanism on
- interrupt disabled by EI = 0

Note 2: Instruction N + 4 is executed only after the interrupt routine; before the interrupt routine only the bus sources are stored in RX and RY

Fig. 2.2.9-1 Interrupt logic timing in P-mode.



Note: The interrupt is postponed when one of the following conditions is true during instruction N + 1:
- loading of PC (as part of BRANCH or MOVE operation)
- loading of RPR
- stack source or destination to X-bus
- repetition mechanism on
- interrupt disabled by EI = 0

Fig. 2.2.9-2 Interrupt logic timing in NP-mode.

Accepting the interrupt means pushing the value of the PC (in P-mode) or PC+1 (NP-mode) on to the stack and loading the PC with address 1. When the PC contains address 1, the $\overline{IACK}$ pin goes LOW for one clock cycle to indicate to the outside world that the interrupt has been acknowledged.

In the P-mode, the instruction in the pipeline that should have been executed is not executed while the PC contains address 1 even though the expected X and Y-bus sources put their data on the buses. This data is stored in the bus-save register, RX and RY, that are automatically assigned as the destinations for the buses.

An interrupt routine is completed under program control using a RETI conditional BRANCH operation (see instruction set section 3.0). When the condition is true, PC is loaded with the address that was pushed onto the stack, and then the instruction at that address is executed. In the P-mode, however, RX and RY are used instead of the indicated X and Y-bus sources. Nested interrupts are permitted, but in the P-mode they are latched so long as the programmer has not stored the data in RX and RY elsewhere (i.e. so long as RX and RY have not been used as sources for the X and Y-buses). After returning from a nested interrupt in the P-mode, the old contents of RX and RY must be restored by the programmer.

To assure the correct functioning of the interrupt procedure, the following rules must be obeyed:

- an interrupt must be performed and exited in the same processor mode (P or NP)
- changing mode: the interrupt should be disabled before the FQR bit is altered

Note: Any READ/WRITE to the RX/RY bus-save registers, independent of the processor mode, will set/reset two internal interrupt disable flags. In P-mode the two internal interrupt disable flags are affected in the following ways:

- set by an interrupt
- individually set by writing to the RX/RY bus-save registers
- reset after an interrupt has been carried-out
- individually reset by reading from the RX/RY bus-save registers.

A new interrupt can only be generated after the $\overline{INT}$ signal has been HIGH for at least one positive going edge on CLK.

RX and RY can be used as general purpose registers when the interrupt is not used.

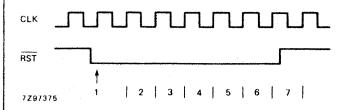
2.2.10 Reset circuitry (RST pin)

The processor is reset to the initial state when RST is LOW over at least 7 positive-going edges of CLK. A shorter reset may lead to an undefined situtation.

The initial state is characterized by:

- PC : all zeros
- PST : 0E00
- IOF : SIXACK=SIYACK =0 and SOXACK = SOYACK = 1
- RX, RY : all zeros
- STACK : all zeros (5 x 10)
- RPR : instruction repeat mechanism off
- LPR : STATE = 0
- MXL, MYL : all zeros
- RAMA(0) : all zeros
- RAMB(0) : all zeros
- PR : all zeros
- ACR : all zeros
- BSR : all zeros
- ARA, AA, SA : all zeros
- ARB, AB, SB : all zeros
- ARR, AR, SR : all zeros
- MA, MB, MR : all zeros
- PG : all zeros
- SIOST : all zeros
- SOX, SOY : all zeros
- $\overline{SIXRQ}$ = $\overline{SIYRQ}$ = 0
- $\overline{SOXRQ}$ = $\overline{SOYRQ}$ = 1

The logic timing of the reset is shown in Fig. 2.2.10-1.



1 – reset detection
2 – reset of all registers and latches mentioned above (excluding ACR), and "top of stack", serial I/O request signals, and PR
3 – reset of ACR and 2nd stack position
4 – reset of 3rd stack position
5 – reset of 4th stack position
6 – reset of 5th stack position
7 – reset of 6th stack position (note: this stack position must not be used, otherwise it may lead to an undefined state).

Fig. 2.2.10-1
The complete reset action.

2.2.11 Synchronization circuitry (SYNC pin)

The processor indicates where execution of a new instruction starts with a HIGH at the SYNC pin for half a clock cycle. This occurs once every two clock cycles in the NP-mode, and once every clock cycle in the P-mode. However, in the P-mode it will not occur when the program counter is loaded with a new address during the execution of a BRANCH operation, an interrupt or a reset.

2.3 DATA MEMORIES AND ACU'S

2.3.1 Data memories

The processor contains 3 on-chip data memories:

- RAMA: 128 x 16 bits, static
- RAMB: 128 x 16 bits, static
- ROM : 512 x 16 bits (only on PCB5010, external for PCB5011)

It is also possible to connect up to 64K of external data memory via the parallel I/O.

Memory outputs are connected to the data registers (DRA, DRB and DRR) and the parallel data input register PI. DRA, DRB and DRR are updated every instruction cycle, but in the P-mode, DRA and DRB are not updated when in that instruction cycle, data is moved (from one of the buses) into RAMA or RAMB. Updating PI is described in the section 2.6 on the parallel I/O. Data written into the data registers and PI can be transferred via the X or Y-bus during a subsequent instruction.

RAMA can be written-to via the X-bus, RAMB can be written-to via the Y-bus and, external RAM can be written-to via either bus.

With the PCB5011, it is not only possible to read from an external ROM, but in place of the read, it is also possible to write-to an external 512 x 16-bit memory because the port is bidirectional, and therefore can be used as a second parallel I/O port.

2.3.2 ACUs and PG register

The 3 address computation units, ACUA, ACUB and ACUR, function identically but, their address widths differ: 12, 8 and 9 bits respectively. ACUs calculate the addresses for the on-chip RAMs (only the 7 least significant address bits are used for this addressing) and data ROM. ACUA not only generates the address for RAMA but also the part of the address for external data memory that defines the position within a page of 4096 x 16 words. It is possible to have 16 pages of external data memory. Pages are selected using the address pins A12 to A15 that reflect the contents of the page register PG that is loaded using a MOVE or LOAD IMMEDIATE operation.

Fig. 2.3.2-1 illustrates the memory addressing.

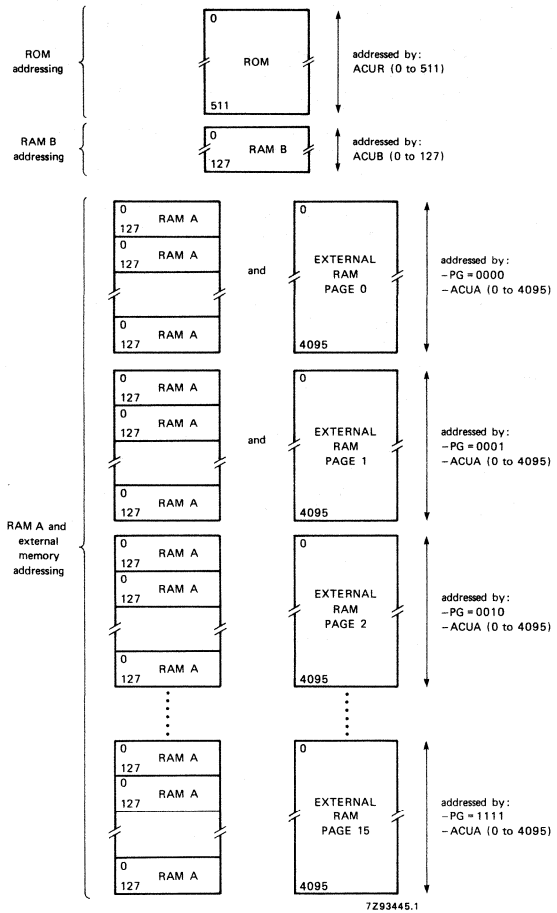


Fig. 2.3.2-1 Memory addressing.

Note to Fig. 2.3.2-1

RAMA and the external RAM are always simultaneously accessed by ACUA. A read-access results in loading of DRA and (under certain conditions determined by the PI01 and PI02 bits) simultaneous loading of PI. A next instruction specifies which of the two words (or both) are transferred to other places within the DSP via the data buses. A write-access results in an update of RAMA and/or the external RAM, depending on the specified destinations.

DEVELOPMENT DATA

An ACU contains:
- an address register AR (which addresses the ROM respectively RAM's)
- a base address register A
- an offset register S
- an address masking register M
- a dedicated arithmetic unit

Only the AR registers (ARR, ARB and ARA) are shown in Figs 2.1-1 and 2.1-2. The A, S and M registers of RAMA, RAMB and the ROM (AA/BA/RA, AS/BS/RS and AM/BM/RM) are not shown.
The A, S, M and AR registers can be loaded directly (for initialization) via one of the data buses (X-bus for ACUB registers and Y-bus for ACUA and ACUR registers) using a MOVE or LOAD IMMEDIATE operation or they can be modified during address computation operations. Direct loading and address computation cannot take place simultaneously (see the section 3.0 on the instruction set).

Direct loading offers the following options:
- Load AR with value on the bus
- Load AR and A with value on the bus
- Load AR and S with value on the bus
- Load A with value on the bus
- Load S with value on the bus
- Load M with value on the bus
- Load AR, A and S with value on the bus
- Load AR with (value on the bus) !M

The notation !M means that, depending on the contents of the M register, all bits are not necessarily updated as the expression indicates:
- the bits whose corresponding bits in the M register are 1 are updated as specified in the expression
- the bits whose corresponding bits in the M register are 0 will retain their value (for AR) or will receive the previous value of their AR bit (for A and S).

The notation br(. . .) means that the bits are reversed in order.

Three flags in the PST register indicate the status of the 3 ACU's:
- ACA – ACUA flag is 1 when AR contained 0000 0000 0000 (binary) during the last clock cycle;
  ACUA flag is 0 when the AR was not 0000 0000 0000 (binary) during the last clock cycle
- ACB – ACUB flag is 1 when AR contained 0000 0000 (binary) during the last clock cycle;
  ACUB flag is 0 when the AR was not 0000 0000 (binary) during the last clock cycle
- ACR – ACUR flag is 1 when AR contained 0 0000 0000 (binary) during the last clock cycle;
  ACUR flag is 0 when the AR was not 0 0000 0000 (binary) during the last clock cycle.

Address computation offers the following options:

• AR:=AR	A:=A	S:=S	M:=M
• AR:=(A+1)!M	A:=(A+1)!M	S:=S	M:=M
• AR:=(A−1)!M	A:=(A−1)!M	S:=S	M:=M
• AR:=(A+S)!M	A:=(A+S)!M	S:=S	M:=M
• AR:=(S+1)!M	A:=A	S:=(S+1)!M	M:=M
• AR:=(A)!M	A:=A	S:=S	M:=M
• AR:=(S)!M	A:=A	S:=S	M:=M
• AR:=br(A+S)	A:=A+S	S:=S	M:=M

2.4 MULTIPLIER, ACCUMULATOR, BARREL-SHIFTER AND FORMAT-ADJUSTER UNIT

2.4.1 Multiplier

The multiplier performs a multiplication of two signed 16 bits operands P and Q presented in 2's complement notation. The result is presented by 32 bits in 2's complement notation and stored in the product result latch PR.

One of the following values can be chosen as P-operand:
- The value present on the X-bus
- The previous value which was automatically latched in the MXL latch
- The number −1

One of the following values can be chosen as Q-operand:
- The value present on the Y-bus
- The previous value which was automatically latched in the MYL latch
- The negated Y-bus value

  Note: When the Y-bus contains the highest negative value, -2^{15} (1000 0000 0000 0000 in binary) then the operand will be the highest positive value plus one, $+2^{15}$ (0111 1111 1111 1111 + 1 in binary). This number is stored in MYL which has a width of 17 bits for this particular situation.

The contents of MXL, MYL and PR are not changed when no MULTIPLY operation or a multiply HOLD operation is executed.

2.4.2 Accumulator

The accumulator unit consists of a 40 bit adder ACC, a 40 bit multiplication/accumulation register ACR and a sign and scale down block S/SD. The adder adds the results of the multiplication stored in PR to a second operand (provided by the S/SD block) which can be chosen from the following set:

- + or − the contents of ACR
- + or − the contents of ACR divided by 2^{15} (which allows multiprecision multiplication and addition)
- the number 0

The result of the addition is stored in ACR and is fed simultaneously to the barrel-shifter. The contents of the ACR register are not changed when no MULTIPLY operation is performed or a multiply HOLD operation is executed.

The 40-bit width of the accumulator allows the programmer to accumulate a number of multiplier results (at least 511) without the risk of overflow. Two flags in the PST register indicate the status of the accumulator:

- OVFL — overflow lock flag; this flag is set when overflow occurs in the adder (result outside the range -2^{39} to $+2^{39}-1$). For reset conditions see description of PST register (section 2.2.8).
- SGNM — sign flag; indicates the sign of the result of the addition (is identical to bit ACR(39)).

2.4.3 Barrel-shifter

From the 40-bit ACR contents, the barrel-shifter extracts 32 contiguous bits. The programmer determines which group of 32 bits is extracted by a value placed in the BSR register (bits BSR3 to BSR0). Sixteen different sets are possible; see Table 2.4.3-1.

Table 2.4.3-1 16 possible sets of 32 contiguous bits

BSR contents BSR3 - BSR0	32-bit word, E31 - E0, extracted by the barrel-shifter
0000	ACR30, ... ,ACR0,0
0001	ACR31, ... ,ACR0
0010	ACR32, ... ,ACR1
0011	ACR33, ... ,ACR2
0100	ACR34, ... ,ACR3
0101	ACR35, ... ,ACR4
0110	ACR36, ... ,ACR5
0111	ACR37, ... ,ACR6
1000	ACR38, ... ,ACR7
1001	ACR39, ... ,ACR8
1010	ACR39,ACR39, ... ,ACR9
1011	ACR39,ACR39,ACR39, ... ,ACR10
1100	ACR39,ACR39,ACR39,ACR39, ... ,ACR11
1101	ACR39,ACR39,ACR39,ACR39,ACR39, ... ,ACR12
1110	ACR39,ACR39,ACR39,ACR39,ACR39,ACR39, ... ,ACR13
1111	ACR39,ACR39,ACR39,ACR39,ACR39,ACR39,ACR39,....,ACR14

Two flags in the PST register indicate the status of the barrel-shifter:

- OOR — Out of range flag. It is set when the sign bit of the extracted word E31-E0 has no significance. This occurs when one or more bits of ACR to the left of the extracted word differs from E31.
- OORL — Out of range lock flag. The conditions for setting are identical to those of OOR. The conditions for resetting are given in the section describing the PST register.

2.4.4 Format adjuster

The output E31-E0 of the barrel-shifter is split into a 16-bit most significant part (MSP) and a 16-bit least significant part (LSP). MSP can be connected directly to the X and/or Y bus. LSP passes through a format adjuster (FA) before it reaches the X or Y bus. The output of FA is called LSP. Under software control, three FA options can be selected by placing a value in the BSR register (bits BSR5 to BSR4). The options are shown in Table 2.4.4-1.

Table 2.4.4-1 The three FA output options (LSP)

BSR contents BSR5 - BSR4	output LSP of format adjuster
00	E15-E0 (no change)
01	E0-E15 (bits reversed in order, used to speed-up certain serial outputs)
10	0, E15-E1 (bits shifted right over 1 position, left adjusted with zero; used for multi-precision multiplications)
11	reserved/undefined

2.4.5 Barrel-shifter register (BSR)

BSR is a 6-bit register. Its contents control the barrel-shifter (bit 0-3) and the format adjuster (bit 4-5) as explained in the previous sections. BSR can be loaded by means of a MOVE or LOAD IMMEDIATE operation. Loading has to be done at least one instruction before LSP or MSP is read to the X or Y-bus.

2.5 ALU AND REGISTER FILE

2.5.1 ALU

The PCB5010/11 has an ALU totally independent from the multiplier/accumulator unit. It is a 16-bit, 2-operand unit capable of executing 31 distinct operations. There are arithmetic, logic and some special purpose operations. The arithmetic operations defined as "extended" (mnemonic starts with X) are included to facilitate multi-precision operations. Extended operands are represented by 16-bit multiples.

An ALU operation produces a result R that may be stored in the register file or may be ignored (dumped in the trash can).

Several flags in the PST register give the status of the ALU. The flags are:
Z – Zero flag
N – Negative flag
C – Carry flag
V – Overflow flag
VL – Overflow lock flag (same as V but locked; see PST register description, section 2.2.8).

One of the following values can be chosen as A-operand:
- the value on the X-bus
- the value on the Y-bus
- the previous value which was automatically latched in the AAL-latch (this is not the case with the "byte swap" instruction).

One of the following values can be chosen as B-operand:
- the value on the Y-bus
- the previous value which was automatically latched in the ABL-latch

Dyadic operations require an A and B-operand, while monadic operations require only an A-operand. Some operations do not require an operand at all.

The ALU operations and their result R and flag settings are summed up in the following three tables:
A: Arithmetic operations
B: Logic operations
C: Other operations

The following notation is used:
- ZERO(R) – 0 (when not all 16 bits of R are 0)
  – 1 (when all 16 bits of R are 0)
- CARRY(F) – 0 (when a function F does not lead to a carry)
  – 1 (when a function F leads to a carry)
  Note: For this calculation, the operands are unsigned 16-bit numbers from 0 to 65535. The carry is 1 when the result of the addition is greater than 0. In all other cases the carry is 0.
- BORROW(F) – 0 (when a function F does not lead to a borrow)
  – 1 (when a function F leads to a borrow)
  Note: For this calculation, the operands are unsigned 16-bit numbers from 0 to 65535. The borrow is 1 when the result of the subtraction is below 0. In all other cases the borrow is 0.
- OVERFLOW(F) – 0 (when a function F does not lead to an overflow)
  – 1 (when a function F leads to an overflow)
  Note: For this calculation, the operands are signed 16-bit numbers between -2^{15} and $2^{15}-1$. The overflow is 1 when the result of the calculation is outside this range. In all other cases the overflow is 0.
- R(i) – Bit i of the 16-bit word R.

A: Arithmetic operations (Table 2.5.1-1)

For the calculation of result R, the operands A and B are considered to be binary numbers in 2's complement notation (between -2^{15} and $+2^{15}-1$). R is also a binary number in 2's complement notation. However, with the DIV operation, the operands and the result are unsigned numbers (between 0 and 65535).

B: Logic operations (Table 2.5.1-2)

For the calculation of result R, the operands A and B are considered to be 16-bit binary words. R is also a 16-bit binary word.

C: Other operations (Table 2.5.1-3)

Table 2.5.1-1 Arithmetic operations

function	menmonic	result (R)	flags				condition
			Z	N	C	V	
addition	ADD	A+B	ZERO(R)	R(15)	CARRY(A+B)	OVERFLOW(A+B)	no overflow
		$A+B-2^{16}$	ZERO(R)	R(15)	CARRY(A+B)	OVERFLOW(A+B)	positive overflow
		$A+B+2^{16}$	ZERO(R)	R(15)	CARRY(A+B)	OVERFLOW(A+B)	negative overflow
extended addition	XADD	A+B+C	ZERO(R).AND.Z	R(15)	CARRY(A+B+C)	OVERFLOW(A+B+C)	no overflow
		A+B+C−2(16)	ZERO(R).AND.Z	R(15)	CARRY(A+B+C)	OVERFLOW(A+B+C)	positive overflow
		A+B+C+2(16)	ZERO(R).AND.Z	R(15)	CARRY(A+B+C)	OVERFLOW(A+B+C)	negative overflow
subtraction	SUB	A−B	ZERO(R)	R(15)	BORROW(A−B)	OVERFLOW(A−B)	no overflow
		$A-B-2^{16}$	ZERO(R)	R(15)	BORROW(A−B)	OVERFLOW(A−B)	positive overflow
		$A-B+2^{16}$	ZERO(R)	R(15)	BORROW(A−B)	OVERFLOW(A−B)	negative overflow
extended subtraction	XSUB	A−B−C	ZERO(R).AND.Z	R(15)	BORROW(A−B−C)	OVERFLOW(A−B−C)	no overflow
		$A-B-C-2^{16}$	ZERO(R).AND.Z	R(15)	BORROW(A−B−C)	OVERFLOW(A−B−C)	positive overflow
		$A-B-C+2^{16}$	ZERO(R).AND.Z	R(15)	BORROW(A−B−C)	OVERFLOW(A−B−C)	negative overflow
conditional subtraction	CSUB	A	ZERO(R)	R(15)	0	0	N=0
		A−B	ZERO(R)	R(15)	BORROW(A−B)	OVERFLOW(A−B)	no overflow
		$A-B-2^{16}$	ZERO(R)	R(15)	BORROW(A−B)	OVERFLOW(A−B)	positive overflow } N=1
		$A-B+2^{16}$	ZERO(R)	R(15)	BORROW(A−B)	OVERFLOW(A−B)	negative overflow
negate	NEG	0−A	ZERO(R)	R(15)	BORROW(0−A)	OVERFLOW(0−A)	$A \neq -2^{15}$
		A	ZERO(R)	R(15)	BORROW(0−A)	OVERFLOW(0−A)	$A = -2^{15}$
extended negate	XNEG	0−A−C	ZERO(R).AND.Z	R(15)	BORROW(0−A−C)	OVERFLOW(0−A−C)	$A \neq -2^{15}$.OR.C = 1
		A	ZERO(R).AND.Z	R(15)	BORROW(0−A−C)	OVERFLOW(0−A−C)	$A = -2^{15}$.AND.C = 0
conditional negate	CNEG	A	ZERO(R)	R(15)	0	0	N=0
		0−A	ZERO(R)	R(15)	BORROW(0−A)	OVERFLOW(0−A)	$A \neq -2^{15}$.AND.N = 1
		A	ZERO(R)	R(15)	BORROW(0−A)	OVERFLOW(0−A)	$A = -2^{15}$.AND.N = 1
decrement	DEC	A−1	ZERO(R)	R(15)	BORROW(A−1)	OVERFLOW(A−1)	$A \neq -2^{15}$
		$2^{15}-1$	ZERO(R)	R(15)	BORROW(A−1)	OVERFLOW(A−1)	$A = -2^{15}$
extended decrement	XDEC	A−C	ZERO(R).AND.Z	R(15)	BORROW(A−C)	OVERFLOW(A−C)	$A \neq -2^{15}$.OR.C = 0
		$2^{15}-1$	ZERO(R).AND.Z	R(15)	BORROW(A−C)	OVERFLOW(A−C)	$A = -2^{15}$.AND.C = 1
increment	INC	A+1	ZERO(R)	R(15)	CARRY(A+1)	OVERFLOW(A+1)	$A \neq 2^{15}-1$
		-2^{15}	ZERO(R)	R(15)	CARRY(A+1)	OVERFLOW(A+1)	$A = 2^{15}-1$
extended increment	XINC	A+C	ZERO(R).AND.Z	R(15)	CARRY(A+C)	OVERFLOW(A+C)	$A \neq 2^{15}-1$.OR.C = 0
		-2^{15}	ZERO(R).AND.Z	R(15)	CARRY(A+C)	OVERFLOW(A+C)	$A = 2^{15}-1$.AND.C = 1
arithmetic shift left	ASL	2*A	ZERO(R)	R(15)	CARRY(A+A)	OVERFLOW(A+A)	$-2^{14} < A < 2^{14}$
		$2*A-2^{16}$	ZERO(R)	R(15)	CARRY(A+A)	OVERFLOW(A+A)	$A \geqslant 2^{14}$
		$2*A+2^{16}$	ZERO(R)	R(15)	CARRY(A+A)	OVERFLOW(A+A)	$A < -2^{14}$
extended arithmetic shift left	XASL	2*A+C	ZERO(R).AND.Z	R(15)	CARRY(A+A)	OVERFLOW(A+A)	$-2^{14} < A < 2^{14}$
		$2*A+C-2^{16}$	ZERO(R).AND.Z	R(15)	CARRY(A+A)	OVERFLOW(A+A)	$A \geqslant 2^{14}$
		$2*A+C+2^{16}$	ZERO(R).AND.Z	R(15)	CARRY(A+A)	OVERFLOW(A+A)	$A < -2^{14}$
arithmetic shift right	ASR	A/2-fraction	ZERO(R)	R(15)	1(0)	0	
extended arithmetic shift right	XASR	A/2-fraction	ZERO(R).AND.Z	N	A(0)	0	MSB of A = C
		$A/2\text{-fraction}-2^{15}$	ZERO(R).AND.Z	N	A(0)	0	MSB of A = 0.AND.C = 1
		$A/2\text{-fraction}+2^{15}$	ZERO(R).AND.Z	N	A(0)	0	MSB of A = 1.AND.C = 0

Table 2.5.1-1 (continued)

function	mnemonic	result (R)	flags				condition
			Z	N	C	V	
add MSB of B to A	ADDM	A+B(15) A+B(15)−2^{16}	ZERO(R) ZERO(R)	R(15) R(15)	CARRY(A+B(15)) CARRY(A+B(15))	OVERFLOW(A+B(15)) OVERFLOW(A+B(15))	A+B(15) < 2^{15} A+B(15) = 2^{15}
unsigned division	DIV	2*(A−B) 2*A 2*(A−B) 2*A	ZERO(R) ZERO(R) ZERO(R) ZERO(R)	0 0 1 1	1 1 0 0	0 0 0 0	0 ⩽ A−B ⩽ $2^{15}-1$ 2^{15} ⩽ A−B ⩽ $2^{16}-1$ -2^{16} ⩽ A−B ⩽ $-2^{15}-1$ -2^{15} ⩽ A−B ⩽ −1
sign extension	XSGN	NN . . . . N	Z.AND.NOT.N	N	N	V	

Table 2.5.1-2 Logic operations

function	mnemonic	result (R)	flags				condition
			Z	N	C	V	
complement	COM	.NOT.A(i)		R(15)	0	0	for i=0 . . . 15
logic AND	AND	A(i).AND.B(i)	ZERO(R)	R(15)	0	0	for i=0 . . . 15
logic OR	OR	A(i).OR.B(i)	ZERO(R)	R(15)	0	0	for i=0 . . . 15
exclusive OR	EXOR	A(i).EXOR.B(i)	ZERO(R)	R(15)	0	0	for i=0 . . . 15
byte swap	SWAP	A(i+8) A(i−8)	ZERO(R) ZERO(R)	R(15) R(15)	0 0	0 0	for i=0 . . . 7 for i=8 . . . 15
logic shift left	LSL	A(i−1) 0	ZERO(R) ZERO(R)	A(14) A(14)	A(15) A(15)	0 0	for i=1 . . . 15 for i=0
logic rotate left	LROL	A(i−1) C	ZERO(R) ZERO(R)	A(14) A(14)	A(15) A(15)	0 0	for i=1 . . . 15 for i=0
logic shift right	LSR	A(i+1) 0	ZERO(R) ZERO(R)	0 0	A(0) A(0)	0 0	for i=0 . . . 14 for i=15
logic rotate right	LROR	A(i+1) C	ZERO(R) ZERO(R)	0 0	A(0) A(0)	0 0	for i=0 . . . 14 for i=15

Table 2.5.1-3 Other operations

function	mnemonic	result (R)	flags				condition
			Z	N	C	V	
pass and flag update	PASS	A	ZERO(A)	A(15)	0	0	
generate 0	NULL	0	1	0	0	0	
no operation	–	–	Z	N	C	V	

2.5.2 Register file

The output of the ALU is connected to the register file. This register file contains fifteen 16-bit registers. The programmer can choose to which register the ALU result is written and also has the option of discarding the result by writing it to the trash can.

The contents of any register may be read to either or both of the buses. Moreover, the register file is implemented as a 3-port memory, so that in the same instruction cycle three registers can be accessed: two accesses to read the present contents of register(s) and one to write in a new value.

The register file can be filled directly from the buses by a MOVE or LOAD IMMEDIATE operation. This does not affect the ALU flags but the AAL-latch will be updated. ALU operations cannot be specified simultaneously with the aforementioned MOVE operation.

2.6 PARALLEL I/O

Via the D15 – D0 pins, the PCB5010/11 permits parallel communication between the X or Y-bus and the outside world. An input or output can take place during each instruction cycle. Output occurs when data is transferred via the X or Y-bus with destination PO. The output is direct, there is no latching. Inputs are loaded into the parallel input latch PI, whose contents can be transferred via the X or Y-bus during a subsequent instruction. The programmer can select one of four input criteria by writing specified values into PST bits, PIO1 and PIO2; see Table 2.6-1.

The following control signals are associated with the parallel I/O (see timing in section 4):

- R/$\overline{W}$: indicates a read or write action (output)
- $\overline{DS}$: data strobe (output)
- $\overline{WAIT}$: signals for synchronization of the parallel I/O (input). This signal delays the internal clock, so that "slow" peripheral devices may be connected. Note: The $\overline{WAIT}$ signal can also be used with the second parallel I/O port in the PCB5011 (see section 2.3.1).

A block diagram of the parallel I/O circuitry is shown in Fig. 2.6-1.

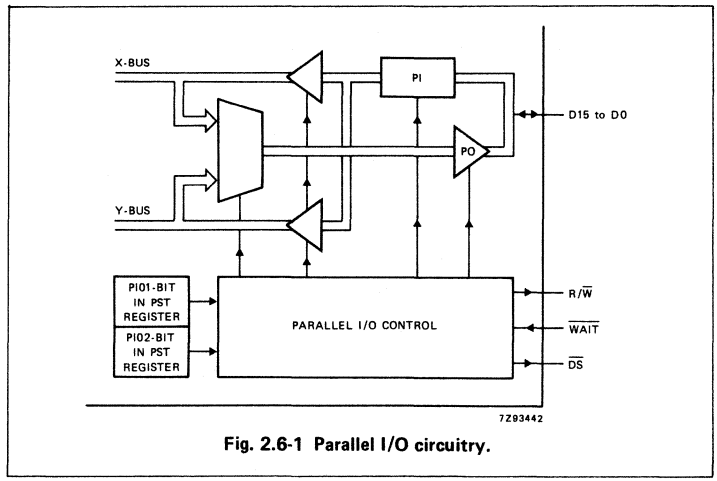


Fig. 2.6-1 Parallel I/O circuitry.

Table 2.6-1 Four selectable input criteria

PIO1	PIO2	DESCRIPTION
0	0	data is latched into PI every instruction cycle
0	1	data is latched into PI only when: – ACUA is not executing a "no operation" – PI latch is source to X or Y-bus
1	0	data is latched into PI only when: – PI latch is source to X or Y-bus
1	1	no data is latched into PI

Note to Table 2.6-1

A read is only performed when there is no write (MOVE or LOAD IMMEDIATE operation to PO).

2.7 SERIAL I/O

2.7.1 Serial data inputs/outputs

The PCB5010/11 has 2 independent serial data inputs DIX and DIY and 2 independent serial data outputs DOX and DOY (destinations and sources for X and Y-buses respectively). The maximum data transfer rate is 4.1 million bits/s. Data transfer is controlled by external clock signals CIX, COX, CIY and COY.

The following handshake signals, described in more detail in the following sections, are associated with the serial I/O:

- input/output enable $\overline{\text{SIXEN}}$, $\overline{\text{SOXEN}}$, $\overline{\text{SIYEN}}$ and $\overline{\text{SOYEN}}$ (input signals)
- input/output request $\overline{\text{SIXRQ}}$, $\overline{\text{SOXRQ}}$, $\overline{\text{SIYRQ}}$ and $\overline{\text{SOYRQ}}$ (output signals)

The following flags, whose functions are also described in the following sections, are associated with the serial I/O:

- serial I/O acknowledge flags SIXACK, SOXACK, SIYACK and SOYACK.

The programmer may control the length of the words to be transferred (between 1 and 16 bits) by writing the applicable values in the SIOST register fields, see Table 2.7-1.

Table 2.7-1 Word-length control

bit		word	word description
MSB	LSB		
03	00	SOLX	length of the serial output word, X-bus source
07	04	SILX	length of the serial output word, X-bus destination
11	08	SILY	length of the serial input word, Y-bus source
15	12	SOLY	length of the serial input word, Y-bus destination

Notes to Table 2.7-1

1. The binary number in each field specifies the length, the code 0000 indicates a length of 16 bits.
2. To avoid data transfers with incorrect word-length, the contents of the SIOST register should not be altered while the serial input/outputs are enabled.

2.7.2 Serial data input procedure

The X and Y serial data inputs are identical, therefore, only the serial input-X is described in the following paragraphs. Figures 2.7.2-1 and 2.7.2-2 are used to simplify the explanation of the serial data input procedure.

The serial data input procedure is controlled by the serial input control (SIC) and the serial input synchronization interface (SISI). The SIC controls the handshake signals $\overline{\text{SIXEN}}$ and $\overline{\text{SIXRQ}}$, the operation of the shift register SIXS, the counter CNTIX and the SIX latch. The SISI indicates, according to the CPU read actions and SIX write actions, the actual SIX latch status to both the CPU and SIC. SISI synchronizes the CPU events to the SIC and vice versa. Table 2.7.2-1 describes the serial data input signals.

The serial data input procedure consists of:

- the serial data input control procedure (Fig. 2.7.2-2)
- the serial data input synchronization procedure (Fig. 2.7.3-1).

Table 2.7.2-1 Serial data input signals

signal	description
SIXACK	SIX latch status indicator to CPU: 0; SIX data may be invalid 1; SIX data valid
SIXACKS	SIX latch status indicator to SIC: 0; SIX empty 1; SIX full
READ–SIX	SIX latch read indication from CPU
WRITE–SIX	SIX latch write indication from SIC
$\overline{\text{SIXEN}}$	SIC enable signal from an external device: 0; enables SIC 1; disables SIC
$\overline{\text{SIXRQ}}$	SIC ready indicator to external device: 0; SIC ready to shift 1; SIC not ready to shift
DIX	serial data input from an external device to the SIXS register
CIX	serial input clock signal from an external device

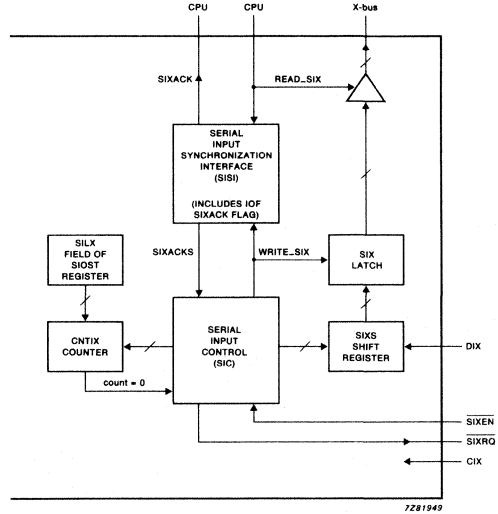


Fig. 2.7.2-1 Block diagram; serial data input.

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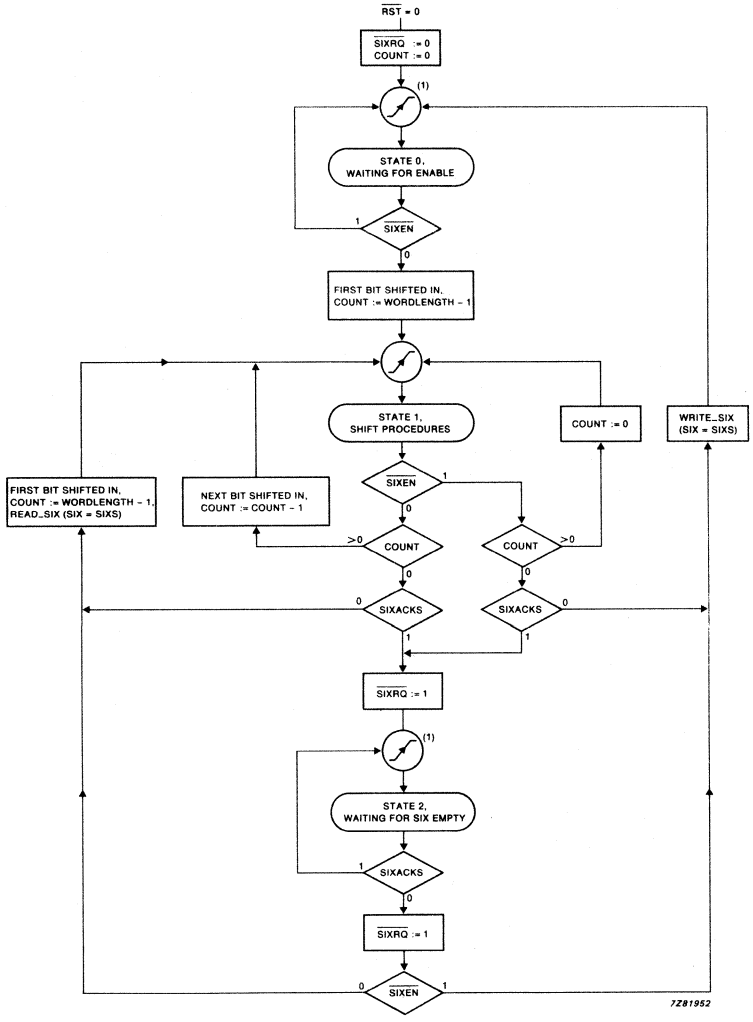

Fig. 2.7.2-2 Serial data input control procedure flow chart.

Note to Fig. 2.7.2-2

1. This point is passed at the next positive-going edge of CIX. At this point the assignments to SIX, SIXS and COUNT are executed. The assignments to $\overline{\text{SIXRQ}}$ are executed at the negative-going edge of SIX.

2.7.3 Serial data input control procedure

On RESET, SIC enters state 0 (awaiting enable), $\overline{\text{SIXRQ}}$ is reset to logic 0 (indicating that the serial input is ready to shift data) and the counter is reset to zero.

- state 0: SIC remains in state 0 until the serial input is enabled. Once enabled, the first bit (LSB) is shifted into SIXS, the counter is loaded with wordlength - 1 and SIC enters state 1 (shift procedure).
- state1: condition 1;
  - If the serial data input is enabled and the counter is not zero
  - then more bits are shifted-in, the counter decrements and SIC re-enters state 1.

  condition 2;
  - If the serial data input is enabled, the counter is zero and SIXACKS indicates an empty SIX latch
  - then the contents of SIXS is transmitted to SIX, a WRITE–SIX signal is transmitted to SISI, the counter is reloaded with word-length - 1, the first bit (LSB) of the next data word is shifted-in and SIC re-enters state 1.

  condition 3;
  - If the counter is zero and SIXACKS indicates that the SIX latch is full
  - then copy cannot performed, $\overline{\text{SIXRQ}}$ is set to logic 1 (indicating to an external device not to transmit new data) and SIC enters state 2.

  condition 4;
  - If the serial data input is disabled, the counter = 0 and SIXACKS indicates an empty SIX latch
  - then the contents of SIXS are transferred to SIX, a WRITE–SIX signal is transmitted to SISI and SIC enters state 0.

  condition 5;
  - If the serial data input is disabled and the counter is not zero
  - then shifting is aborted, the counter is reset to 0 and SIC enters state 1.

Note: Depending on the status of SIXACKS, condition 5 will result in aborted words being transferred from SIXS to SIX.

- state 2: When SIXACKS = logic 0 (indicating an empty SIX latch), then $\overline{\text{SIXRQ}}$ is set to logic 0, transmissions from SIXS to SIX are performed with or without starting (depending on the status of $\overline{\text{SIXEN}}$) the next shift transfer. SIC enters state 0 ($\overline{\text{SIXEN}}$ = logic 1) or state 1 ($\overline{\text{SIXEN}}$ = logic 0).

Note: If less than 16 bits have been received, the word is placed in the most significant part of the SIX latch and the remaining bits are set to logic 0.

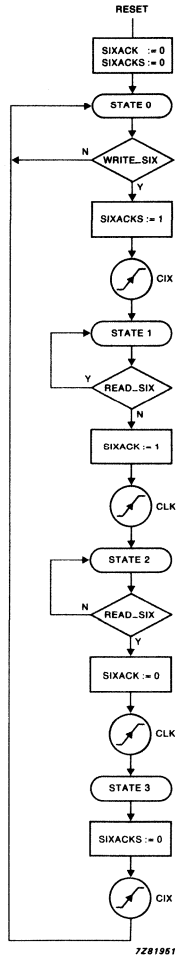

Fig. 2.7.3-1 Serial data input synchronization procedure flow chart.

2.7.4 Serial data input synchronization procedure

On RESET, SISI enters state 0. SIXACK and SIXACKS are reset to logic 0, indicating to the CPU and SIC that the SIX latch is empty.

- state 0: SISI awaiting a WRITE–SIX indication from SIC (indicates that a new data word has been transferred into the SIX latch). Then SIXACKS is set to logic 1 on the next positive-going edge of CIX, which indicates to the SIC that the SIX latch is full. SISI then enters state 1.

- state 1: If no READ–SIX occurs, SIXACK is set to logic 1 on the following positive-going edge of CLK and SISI enters state 2.
- state 2: If SIXACK = logic 1 (indicating to the CPU that valid data is available in the SIX latch), SISI awaits a read operation from the CPU. Then SIXACK is set to logic 0 on the next positive-going edge of CLK. SISI enters state 3.
- state 3: On the next positive-going edge of CIX, SIXACKS is reset to logic 0 and SISI re-enters state 0.

Note: If the CPU reads data from the SIX latch while SISI is not in state 2, invalid or old data maybe transferred onto the X-bus. This can be avoid by only allowing the CPU to perform read operations, from the SIX latch, when SIXACK = logic 1.

2.7.5 Serial data output.

The X and Y serial data outputs are identical, therefore, only the serial output-X described in the following paragraphs. Figures 2.7.5-1 and 2.7.5-2 are used to simplify the explanation of the serial output procedure.

The serial output procedure is controlled by the serial output control (SOC) and the serial output synchronization interface (SOSI). The SOC controls the handshake signals $\overline{\text{SOXEN}}$ en $\overline{\text{SOXRQ}}$, the operation of the shift register SOXS and the counter CNTOX. The SOSI indicates, according to the CPU write actions and SOC read actions, the actual SOX latch status to both the CPU and SOC. SOSI synchronizes the CPU events to the SOC events and vice versa.

Table 2.7.5-1 describes the serial data output signals.

The serial data output procedure consists of:

– the serial data output control procedure (Fig. 2.7.5-2)
– the serial data output synchronization procedure (Fig. 2.7.6-1).

Table 2.7.5-1

signal	description
SOXACK	SOX latch status indicator to CPU: 0; SOX latch full 1; SOX latch empty
SOXACKS	SOX latch status indicator to SOC: 0; SOX data valid 1; SOX data may be invalid
WRITE–SOX	SOX latch write indication from CPU
READ–SOX	SOX latch read indication from SOC
$\overline{\text{SOXEN}}$	SOC enable signal from an external device: 0; enables SOC 1; disables SOC
$\overline{\text{SOXRQ}}$	SOC ready indicator to an external device: 0; SOC ready to shift 1; SOC not ready to shift
DOX	serial data output from an external device to the SOXS register
COX	serial output clock signal from an external device

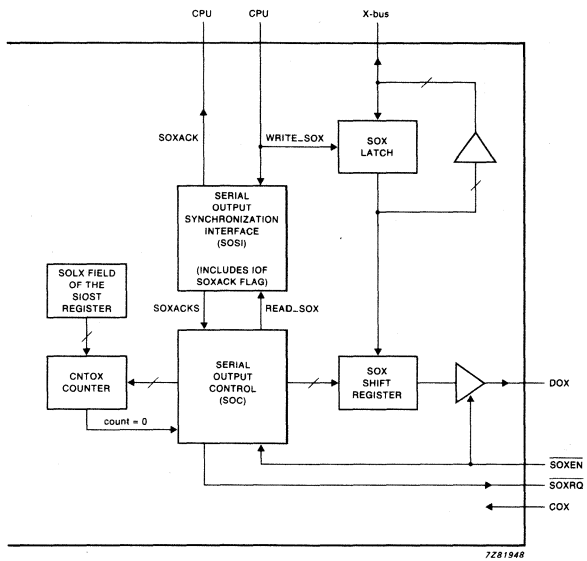

Fig. 2.7.5-1 Block diagram; serial data output.

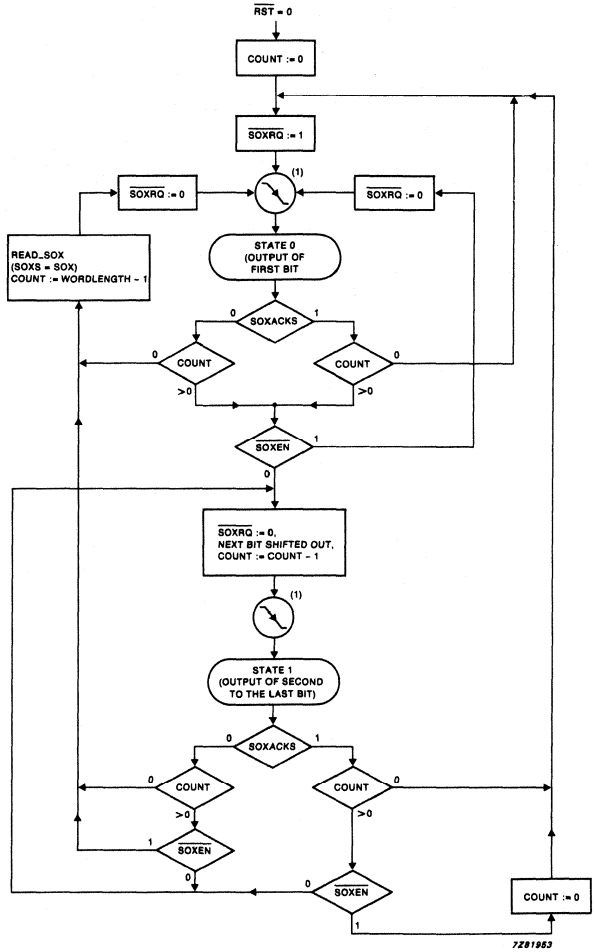

Fig. 2.7.5-2 Serial data output control procedure.

Note to Fig. 2.7.5-2

1. This point is passed at the next negative-going edge of COX. At this point the assignments to SOXS, COUNT and $\overline{\text{SOXRQ}}$ are executed.

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2.7.6 Serial data output control procedure

On RESET, SOC enters state 0 (output first bit), $\overline{\text{SOXRQ}}$ is set to logic 1 (indicating that the serial output is not ready to shift out data) and the counter is reset to zero.

- state 0: condition 1;
  - If the SOX latch contains valid data (SOXACKS = logic 0) and the counter is zero
  - then the counter is reloaded with word-length - 1, SOX is copied into SOXS, the first bit (LSB) is available at the output if $\overline{\text{SOXEN}}$ = logic 0, a READ–SOX is transmitted to SOSI, $\overline{\text{SOXRQ}}$ is reset to logic 0 and SOC re-enters state 0.

  condition 2;
  - If the counter is not zero and the serial output is enabled
  - then the next bit is shifted out, the counter is decremented, $\overline{\text{SOXRQ}}$ remains at logic 0 and SOC enters state 1.

  condition 3;
  - If the counter is not zero and the serial output is disabled
  - then $\overline{\text{SOXRQ}}$ remains at logic 0 and SOC re-enters state 0.

  condition 4;
  - If the SOX latch does not contain valid data SOXACKS = logic 1) when the counter is zero
  - then $\overline{\text{SOXRQ}}$ is set to logic 1 and SOC re-enters state 0.

- state 1: condition 1;
  - If the SOX latch contains valid data (SOXACKS = logic 0) and the counter is zero or the serial data output is disabled
  - then the counter is reloaded with word-length - 1, SOX is copied into SOXS, the first data bit (LSB) is available at the output if $\overline{\text{SOXEN}}$ = logic 0, a READ–SOX is transmitted to SOSI, the $\overline{\text{SOXRQ}}$ remains at logic 0 and SOC enters state 0.

  condition 2;
  - If the counter is not zero and the serial data output is enabled
  - then the next bit is shifted out, the counter is decremented, $\overline{\text{SOXRQ}}$ remains at logic 0 and SOC remains in state 1.

  condition 3;
  - If the serial data output disabled while the counter is not zero and no new data is available from SOX
  - then the output procedure is aborted, the counter is reset to zero, $\overline{\text{SOXRQ}}$ is set to logic 1 and SOC enters state 0. When the serial output is re-enabled with new data available in SOX, then the serial output procedure will continue with the new data word and not with the aborted data word.

  condition 4;
  - If the SOX latch does not contain valid data (SOXACKS = logic 1) and the counter is zero
  - then $\overline{\text{SOXRQ}}$ is set to logic 1 and SOC re-enters state 0.

Note: If 1 bit words (counter loaded with zero) are transferred, the the counter is permanently zero and $\overline{\text{SOXEN}}$ is not examined by SOC. Only SOXACKS is checked to determine the status of the SOX latch. When a new word (bit) is available from SOX latch, then the word is loaded into SOXS (independent of the previous actions). The word is available from SOXS until the next word arrives but $\overline{\text{SOXRQ}}$ is only logic 0 for the first cycle. As soon as the word is transmitted from SOX to SOXS it should be read by the external device with $\overline{\text{SOXEN}}$ = 0 because during the next cycle $\overline{\text{SOXRQ}}$ will be set to logic 1 and this may disable the receiver.

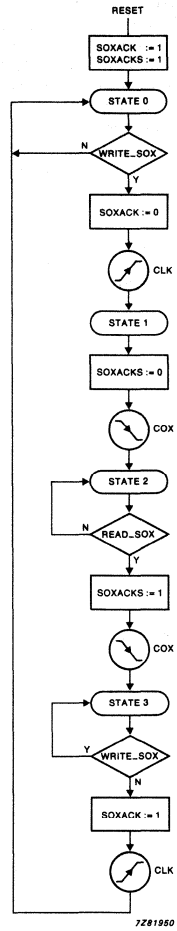


Fig. 2.7.6-1 Serial data output synchronization procedure flow chart.

2.7.7 Serial data output synchronization procedure

On RESET, SOSI enters state 0. SOXACK and SOXACKS are set to logic 1, indicating to the CPU and SOC that the SOX latch is empty.

- state 0: SOXACK = logic 1, indicating to the CPU that data may be written into SOX. SOSI waits for the CPU to perform a write operation. On the next positive-going edge of CLK, SOXACK is reset to logic 0 (indicating to the CPU that SOX is full) and SOSI enters state 1.
- state 1: On the next negative-going edge of COX, SOXACKS is reset to logic 0 (indicating to the SOC that SOX contains new data) and SOSI enters state 2.
- state 2: SOSI awaits a READ–SOX indication from SOC (indicating that a new word has been transmitted from SOX to SOXS). On the next negative-going edge of COX, SOXACKS is set to logic 1 (indicating that data has been transmitted) and SOSI enters state 3.
- state 3: If no WRITE–SOX operation occurs, then on the next positive-going edge of CLK, SOXACK is set to logic 1 and SOSI re-enters state 0.

Note: If the CPU writes data into the SOX latch while SOSI is not in state 0, data in the SOX latch maybe lost or corrupted data may be transferred into SOXS. This can be avoided by only allowing the CPU to perform write operations to the SOX latch, when SOXACK is logic 1.

APPENDIX A

PCB5010/PCB5011 INSTRUCTION SUMMARY

Type 0 instructions: ALU/MOVE/ADDRESS COMPUTATION

TY	ALU			AOPS			SX		SY		DX		DY		RFILE		ACUA		ACUR		ACUB	
	mnemonic	m/d	hex code	mnemonic	m/d	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code
	ADD	d	14	SX,SY	d	0	–	00	–	00	–	0	–	0	–	0	**DY=A**		**DY=E**		**DX=E**	
0	XADD	d	15	AAL,SY	d	1	ROM	01	RAMB	01	FQR	1	BSR	1	R1	1	AR	0	AR	0	AR	0
	SUB	d	16	SX,ABL	d	2	–	02	–	02	SIOST	2	–	2	R2	2	AAR	1	AAR	1	AAR	1
	XSUB	d	17	AAL,ABL	d	3	TOS	03	RAMA	03	RPO	3	RAMB	3	R3	3	SAR	2	SAR	2	SAR	2
	CSUB	d	18				RX	04	RY	04	RX	4	–	4	R4	4	A	3	A	3	A	3
	NEG	m	0C	AAL	m	0	PI	05	ROM	05	PC	5	RY	5	R5	5	S	4	S	4	S	4
	XNEG	m	0D	(*/SWAP)			IOF	06	SIY	06	SOX	6	–	6	R6	6	M	5	M	5	M	5
	CNEG	m	0E	SX	m	1	SOX	07	–	07	(LPR)	7	–	7	R7	7	ASAR	6	ASAR	6	ASAR	6
	DEC	m	0A	SY	m	2	SIX	08	PG	08	–	8	–	8	R8	8	AR1M	7	AR1M	7	AR1M	7
	XDEC	m	0B	–	–	3	SIOST	09	BSR	09	RPR	9	PG	9	R9	9						
	INC	m	08				–	0A	ACU(ROM)	0A	P0	A	ACU(RAMA)	A	R10	A	**DY≠A**		**DY≠E**		**DX≠E**	
	XINC	m	09				RAMB	0B	ACU(RAMA)	0B	RAMA	B	P0	B	R11	B	–	0	–	0	–	0
	ASL	m	07				PST	0C	PST	0C	PST	C	RPO	C	R12	C	INCA	1	INCA	1	INCA	1
	XASL	m	06				RAMA	0D	PI	0D	TOS	D	SOY	D	R13	D	DECA	2	DECA	2	DECA	2
	ASR	m	03				ACU(RAMB)	0E	SOY	0E	ACU(RAMB)	E	ACU(ROM)	E	R14	E	STEP	3	STEP	3	STEP	3
	XASR	m	00				LSP	0F	LSP	0F	RFILE	F	RFILE	F	R15	F	INCS	4	INCS	4	INCS	4
	ADDM	d	1A				MSP	10	MSP	10							A	5	A	5	A	5
	DIV	d	19				R1	11	R1	11							S	6	S	6	S	6
	XSGN	–	1E				R2	12	R2	12							REV	7	REV	7	REV	7
	COM	m	10				R3	13	R3	13												
	AND	d	11				R4	14	R4	14												
	OR	d	12				R5	15	R5	15												
	EXOR	d	13				R6	16	R6	16												
	SWAP	m	1C				R7	17	R7	17												
	LSL	m	05				R8	18	R8	18												
	LROL	m	04				R9	19	R9	19												
	LSR	m	01				R10	1A	R10	1A												
	LROR	m	02				R11	1B	R11	1B												
	PASS	m	0F				R12	1C	R12	1C												
	NULL	–	1D				R13	1D	R13	1D												
	–	–	1B				R14	1E	R14	1E												
	–	–	1F				R15	1F	R15	1F												

* = exclusive

Type 1 instructions: MPY/MOVE/ADDRESS COMPUTATION

TY	MPY		MOPS		SX		SY		DX		DY		RFILE		ACUA		ACUR		ACUB	
	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code
	–	0	SX,SY	0																
1	0	1	SX,–SY	1																
	+ACR	2	MXL,SY	2																
	–ACR	3	MXL,–SY	3																
	+ACRS	4	SX,MYL	4	as above		as above		as above		as above		as above		as above		as above		as above	
	–ACRS	5	MXL,MYL	5																
			–1,–SY	6																
			–1,SY	7																
			–1,MYL	8																

Type 2 instructions: BRANCH/ADDRESS COMPUTATION

TY	NAP	BR		CONDITION		CONDITION			ACUA		ACUR		ACUB	
		mnemonic	hex code	mnemonic	hex code	mnemonic	hex code		mnemonic	hex code	mnemonic	hex code	mnemonic	hex code
2	address of next instruction if condition matches	GOTO	0	–	00	–	01		as above		as above		as above	
		CALL	1	AN	02	NOT AN	03							
		RET	2	X0	04	NOT X0	05							
		RETI	4	–	06	–	07							
				GE	08	LT	09							
				LE	0A	GT	0B							
				IFX	0C	NOT IFX	0D							
				HI	0E	LS	0F							
				OFL	10	NOT OFL	11							
				XOL	12	NOT XOL	13							
				AOL	14	NOT AOL	15							
				VL	16	NOT VL	17							
				Z	18	NOT Z	19							
				N	1A	NOT N	1B							
				C	1C	NOT C	1D							
				V	1E	NOT V	1F							
				SIX	20	NOT SIX	21							
				SOX	22	NOT SOX	23							
				SIY	24	NOT SIY	25							
				SOY	26	NOT SOY	27							
				ACU(RAMA)	28	NOT ACU(RAMA)	29							
				ACU(RAMB)	2A	NOT ACU(RAMB)	2B							
				ACU(ROM)	2C	NOT ACU(ROM)	2D							
				–	2E	–	2F							
				IFA	30	NOT IFA	31							
				IFB	32	NOT IFB	33							
				IFC	34	NOT IFC	35							
				IFD	36	NOT IFD	37							

Type 3 instructions: LOAD IMMEDIATE/ADDRESS COMPUTATION

TY		DATA	DX		DY		RFILE		ACUA		ACUR		ACUB	
			mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code
3		16-bit data transferred to both X and Y buses	as above		as above		as above		as above		as above		as above	

2.8 DATA BUSES X AND Y

The data buses have a width of 16-bits and are used for transferring data between the functional units connected to them. Bus transfers are always part of MOVE and LOAD IMMEDIATE operations and can be part of MPY and ALU operations. The possible sources and destinations of the bus are given in Table 2.8-1.

Table 2.8-1 Possible destinations and sources for the X and Y-bus

source on X	destination on X	source on Y	destination on Y
STACK	STACK		
RX	RX	RY	RY
	PC		
	RPR		
IOF			
IR(DATA field)		IR(DATA field)	
PST	PST	PST	
	FQR		
DRA DRB DRR		DRA DRB DRR	
	RAMA		RAMB
ARB		ARA ARR	
	ACUB		ACUA ACUR
		PG	PG
	ILX		ILY
LSP MSP		LSP MSP	
		BSR	BSR
RFILE	RFILE	RFILE	RFILE
	ILA		ILA ILB
PI	PO	PI	PO
	RPO		RPO
SIOST	SIOST		
SIX SOX	SOX	SIY SOY	SOY
	LPR		

Notes to Table 2.8-1

1. FQR is loaded by putting the required value (0 or 1) in bit 15 of the 16-bit word that is sent. The other bits are 'don't cares'.
2. When the source or destination has a width of less than 16 bits, only the least significant bits on the bus (same width) contain information. For a source, the MSBs are set to zero.
3. ILX and ILY select the operands for the multiplier; ILA and ILB select the operands for the ALU.
4. Destination RPO is only valid for PCB5011.
5. Specifying the same destination for the X and Y-bus results in no data transfer.
6. Destination LPR is only valid for PCB5010.

3.0 INSTRUCTION SET

The behaviour of the processor is controlled by the instructions stored in on-chip ROM (PCB5010) or external program memory (PCB5011). Each instruction leads to the execution of one or more (up to 6) basic operations. The basic operations, the instruction format and the instruction fields are described in the following sections.

3.1 BASIC OPERATIONS

The execution of a basic operation can take either 1 or 2 clock cycles. This means that:

- for 2 cycle basic operations pipelining is used in the P-mode
- a 1 cycle operation is extended by a second "no action" cycle when the processor is operating in the NP-mode.

Basic operation sequencing is shown in Fig. 3.1-1 for the P-mode, and Fig. 3.1-2 for the NP-mode. There are 6 different basic operations which are described below.

- **ALU operation** (1 clock cycle)

  One of 31 different ALU operations is executed. The operations need 2, 1 or 0 operands. The operation's result is stored in the register file or thrown away (into the trash can). In addition, a number of flags are updated.

- **MOVE operation** (1 clock cycle)

  Data from an X-bus (Y-bus) source is transferred via the X-bus (Y-bus) to an X-bus (Y-bus) destination. In the case that both buses have the same destination no transfer takes place.

- **ACU (address computation and memory access) operation** (2 clock cycles)

  Clock cycle 1:
  An address is calculated by the ACU and written into an address register (ARA, ARB, or ARR).

  Clock cycle 2:
  RAMA, RAMB, ROM or external memory is accessed at the location given by the address register (ARA, ARB, or ARR). This access is normally a read which updates one of the data registers (DRA, DRB, DRR, or PI). If in the P-mode, however, the relevant RAM (RAMA, RAMB or external RAM) is assigned as a destination during a MOVE executed in parallel, the access will be a write. The result in this case is that the RAM is updated.

- **MPY (multiply/accumulate) operation** (2 clock cycles)

  Clock cycle 1:
  Two operands are multiplied together and the result stored in the PR latch.

  Clock cycle 2:
  The content of PR is added to the output of S/SD and stored in the ACR.

  Note 1: The contents of the ACR are accessed via the barrel-shifter and format adjuster allowing transfer onto the X or Y-bus during the clock cycle following ACR loading. The buses are selected by specifying LSP and/or MSP as the source for the X or Y-bus.

  Note 2: The explanation of the MPY operation is a simplified presentation of what really happens. In fact, clock cycle 1 is not just used for multiplication, but part of the accumulation as well: i.e. accumulation of the lower part of the multiplier result and the contents of the accumulator. Therefore, in the P-mode, an MPY with +ACRS or −ACRS in the MPY field (see section 3.3 on description of MPY field) that directly follows another MPY operation leads to an undefined situation where the higher part of the first multiplication/accumulation result is already required at the end of clock cycle 1, but is only ready after clock cycle 2. If it is necessary to have an MPY operation with +ACRS or −ACRS directly after a previous MPY operation (for multiprecision multiplication), then there has to be a no operation cycle (or at least no MPY operation) between them.

- **BRANCH operation** (1 or 2 clock cycles)

  Clock cycle 1:
  The branch condition is checked, the result of which can be true or false. When the result is false, the BRANCH operation is terminated. When the result is true, the program counter is loaded with the branch address.

  Clock cylce 2: (only when condition is true)
  The new instruction is fetched to the instruction register IR.

  Note: During this fetch no new operation is started.

- **LOAD IMMEDIATE operation** (1 clock cycle)

  The 16-bit data word specified in the instruction is put on the X-bus and the Y-bus and transferred to one or two specified destinations. In the case that two identical destinations are specified no transfer takes place.

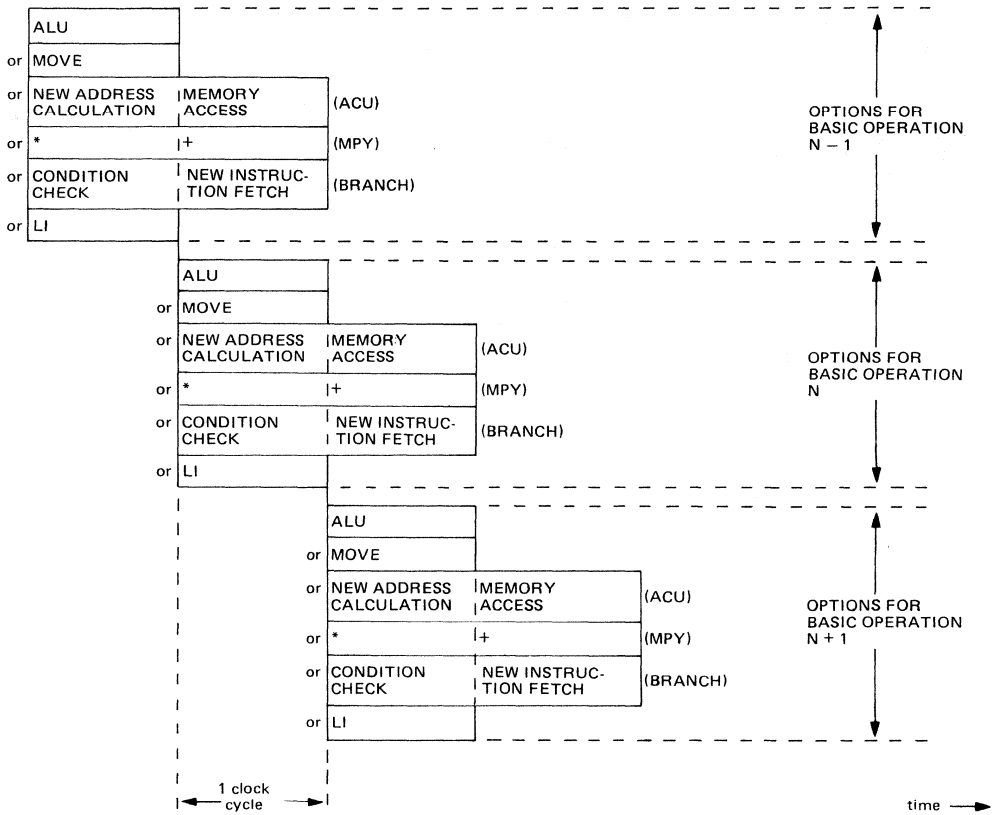


Fig. 3.1-1 Basic operation sequencing in P-mode.

Notes to Fig. 3.1-1

1. Each instruction may contain several simultaneous basic operations (see section 3.2 on instruction formats).
2. "New instruction fetch" (BRANCH) takes place only when the condition is true.
3. During "New instruction fetch" (BRANCH) no new operation is started.
4. Memory access is normally a data register (DRA, DRB, DRR, or PI) read. This read doesn't take place when there is a simultaneous MOVE to a RAM (during a RAM access).
5. An MPY operation with +ACRS or –ACRS in the MPY field directly following another MPY operation leads to an undefined situation (see description of MPY operation).
6. After instruction N which specifies a MOVE or LOAD IMMEDIATE operation to PC first instruction N + 1 is executed.

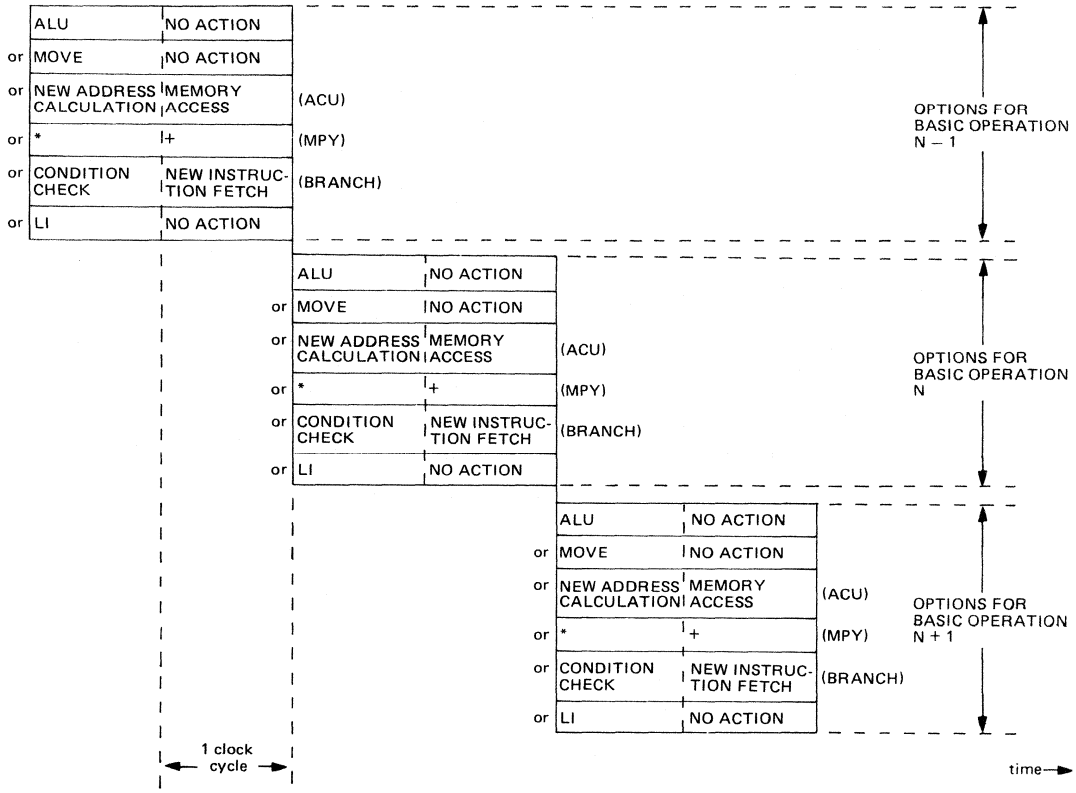


Fig. 3.1-2 Basic operation sequencing in NP-mode.

Notes to Fig. 3.1-2

1. Each instruction may contain several simultaneous basic operations (see section 3.2 on instruction format).
2. "New instruction fetch" (BRANCH) takes place only when the condition is true. If the condition is false, there is no action during the second clock cycle.
3. Memory access is a data register read.

3.2 INSTRUCTION FORMAT

All instruction words are 40-bits wide.

4 types of instructions are defined, each with their own set of basic operations:

Type 0: ALU operation + 2 MOVE operations + 3 ACU operations

Type 1: MULTIPLY operation + 2 MOVE operations + 3 ACU operations

Type 2: BRANCH operation + 3 ACU operations

Type 3: LOAD IMMEDIATE operation + 3 ACU operations.

Each basic operation is specified by the contents of one or more instruction fields (see Fig. 3.2-1).

The field at the far left of each instruction indicates the instruction type (see Table 3.2-1). The other fields are defined in Tables 3.3-1 to 3.3-13.

Table 3.2-1 Instruction types

ALU	= Type of ALU operation	dedicated for ALU operations
AOPS	= ALU operands	dedicated for ALU operations
SX	= Source on X-bus	These fields are for ALU and/or MOVE operations,
SY	= Source on Y-bus	or for MPY and/or MOVE operations
DX	= Destination on X-bus	for MOVE or LI operations
DY	= Destination on Y-bus	for MOVE or LI operations
RFILE	= Destination in Register file	for ALU, MOVE or LI operations
ACUA	= Type of ACUA operation	dedicated for ACU operations
ACUB	= Type of ACUB operation	dedicated for ACU operations
ACUR	= Type of ACUR operation	dedicated for ACU operations
MPY	= Type of accumulator operation	dedicated for MPY operations
MOPS	= Multiply operands	dedicated for MPY operations
NAP	= Address of next instruction when condition is true	dedicated for BRANCH operations
BR	= Type of branch operation	dedicated for BRANCH operations
COND	= Branch condition	dedicated for BRANCH operations
DATA	= 16 bits data word that is transmitted on X and Y-bus	dedicated for LI operations

3.3 INSTRUCTION FIELDS

For each instruction field, the valid codes and their function are specified. For most fields, not only the function is specified but also a mnemonic. The PCB5010/11 assembly language, using the mnemonics in this data sheet, is described in a separate document.

Instruction type 0:

39	38	37 36 35 34 33	32 31	30 29 28 27 26	25 24 23 22 21	20 19 18 17	16 15 14 13	12 11 10 9	8 7 6	5 4 3	2 1 0
0	0	ALU	AOPS	SX	SY	DX	DY	RFILE	ACUA	ACUR	ACUB

Instruction type 1:

39	38	37 36 35	34 33 32 31	30 29 28 27 26	25 24 23 22 21	20 19 18 17	16 15 14 13	12 11 10 9	8 7 6	5 4 3	2 1 0
0	1	MPY	MOPS	SX	SY	DX	DY	RFILE	ACUA	ACUR	ACUB

Instruction type 2:

39	38	37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22	21 20 19	18 17 16 15 14 13	12 11 10 9	8 7 6	5 4 3	2 1 0
1	0	NAP*	BR	CONDITION	0 0 0 0	ACUA	ACUR	ACUB

Instruction type 3:

39	38	37	36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21	20 19 18 17	16 15 14 13	12 11 10 9	8 7 6	5 4 3	2 1 0
1	1	0	DATA	DX	DY	RFILE	ACUA	ACUR	ACUB

* Only bits 22 to 31 are used.

Fig. 3.2-1 The four instruction types and their fields.

Table 3.3-1 ALU instruction field

mnemonic	code binary	code hex	type	function
Arithmetic operations:				
ADD	10100	14	dyadic	addition
XADD	10101	15	dyadic	extended addition
SUB	10110	16	dyadic	subtraction
XSUB	10111	17	dyadic	extended subtraction
CSUB	11000	18	dyadic	conditional subtraction
NEG	01100	0C	monadic	negate
XNEG	01101	0D	monadic	extended negate
CNEG	01110	0E	monadic	conditional negate
DEC	01010	0A	monadic	decrement
XDEC	01011	0B	monadic	extended decrement
INC	01000	08	monadic	increment
XINC	01001	09	monadic	extended increment
ASL	00111	07	monadic	arithmetic shift left
XASL	00110	06	monadic	extended arithmetic shift left
ASR	00011	03	monadic	arithmetic shift right
XASR	00000	00	monadic	extended arithmetic shift right
ADDM	11010	1A	dyadic	add MSB of B to A
DIV	11001	19	dyadic	unsigned division step
XSGN	11110	1E	no operand	extended N flag
Logic operations:				
COM	10000	10	monadic	logic complement
AND	10001	11	dyadic	logic AND
OR	10010	12	dyadic	logic OR
EXOR	10011	13	dyadic	logic exclusive OR
SWAP	11100	1C	monadic	byte swap
LSL	00101	05	monadic	logic shift left
LROL	00100	04	monadic	logic rotate left
LSR	00001	01	monadic	logic shift right
LROR	00010	02	monadic	logic rotate right
Other operations:				
PASS	01111	0F	monadic	pass with flag update
NULL	11101	1D	no operand	generate 0
–	11111	1F	–	reserved
–	11011	1B	–	reserved

Table 3.3-2 AOPS instruction field (note 1)

mnemonic	code binary	code hex	ALU-type	A-operand	B-operand
*, *	00	0	dyadic	source on X-bus	source on Y-bus
AAL, *	01	1	dyadic	AAL	source on Y-bus
*, ABL	10	2	dyadic	source on X-bus	ABL
AAL, ABL	11	3	dyadic	AAL	ABL
AAL (note 2)	00	0	monadic	AAL	–
*	01	1	monadic	source on X-bus	–
*	10	2	monadic	source on Y-bus	–
–	11	3	–	reserved	–

Notes to Table 3.3-2

1. The AOPS field has no meaning when a no operand operation is specified in the ALU field and as there is no operation, AAL and ABL retain their values.
2. The operation is undefined when this operand is selected with a SWAP operation.

* The mnemonic of the particular source is used (see SX and SY fields).

Table 3.3-3 SX instruction field

mnemonic	code binary	code hex	full name of source
–	00000	00	no source
ROM	00001	01	data register DRR
–	00010	02	reserved
TOS	00011	03	top of stack (notes 1 and 2)
RX	00100	04	bussave register X
PI	00101	05	parallel data input register
IOF	00110	06	input/output status and user flag register
SOX	00111	07	serial output register connected to X-bus
SIX	01000	08	serial input register connected to X-bus
SIOST	01001	09	serial I/O control register
–	01010	0A	reserved
RAMB	01011	0B	data register DRB
PST	01100	0C	processor status register
RAMA	01101	0D	data register DRA
ACU(RAMB)	01110	0E	address register ARB
LSP	01111	0F	least significant 16 bits of multiply/shift/adjust result
MSP	10000	10	most significant 16 bits of multiply/shift/adjust result
R1	10001	11	register 1
R2	10010	12	register 2
R3	10011	13	register 3
R4	10100	14	register 4
R5	10101	15	register 5
R6	10110	16	register 6
R7	10111	17	register 7
R8	11000	18	register 8
R9	11001	19	register 9
R10	11010	1A	register 10
R11	11011	1B	register 11
R12	11100	1C	register 12
R13	11101	1D	register 13
R14	11110	1E	register 14
R15	11111	1F	register 15

Notes to Table 3.3-3

1. When TOS is used as a source, the stack is popped one level.
2. It is forbidden to simultaneously use TOS as a source and destination. The interrupt must be disabled before this operation is performed.

Table 3.3-4 SY instruction field

mnemonic	code binary	code hex	full name of source
–	00000	00	no source
RAMB	00001	01	data register DRB
–	00010	02	reserved
RAMA	00011	03	data register DRA
RY	00100	04	bussave register Y
ROM	00101	05	data register DRR
SIY	00110	06	serial input register connected to Y-bus
–	00111	07	reserved
PG	01000	08	page register
BSR	01001	09	barrel-shifter/format adjuster control register
ACU(ROM)	01010	0A	address register ARR
ACU(RAMA)	01011	0B	address register ARA
PST	01100	0C	processor status register
PI	01101	0D	parallel data input register
SOY	01110	0E	serial output register connected to Y-bus
LSP	01111	0F	least significant 16 bits of multiply/shift/adjust result
MSP	10000	10	most significant 16 bits of multiply/shift/adjust result
R1	10001	11	register 1
R2	10010	12	register 2
R3	10011	13	register 3
R4	10100	14	register 4
R5	10101	15	register 5
R6	10110	16	register 6
R7	10111	17	register 7
R8	11000	18	register 8
R9	11001	19	register 9
R10	11010	1A	register 10
R11	11011	1B	register 11
R12	11100	1C	register 12
R13	11101	1D	register 13
R14	11110	1E	register 14
R15	11111	1F	register 15

Table 3.3-5 DX instruction field

mnemonic	code binary	code hex	full name of destination
–	0000	0	no destination
FQR	0001	1	FQR bit in PST; the required value for FQR must be present in bit 15 on the bus; the other bits are don't cares
SIOST	0010	2	serial I/O control register
RPO	0011	3	second parallel data output buffer (PCB5011 only)
RX	0100	4	bussave register X
PC	0101	5	program counter
SOX	0110	6	serial output register connected to X-bus
LPR	0111	7	Load program RAM circuitry (PCB5010 only)
–	1000	8	reserved
RPR	1001	9	instruction repeat register
PO	1010	A	parallel data output buffer
RAMA	1011	B	RAMA
PST	1100	C	processor status register
TOS	1101	D	top of stack (notes 1 and 2)
ACU(RAMB,*)	1110	E	ACUB
**	1111	F	register file

Notes to Table 3.3-5

1. When TOS is used as a destination, the stack is pushed one level.
2. It is forbidden to simultaneously use TOS as a source and destination.

Table 3.3-6 DY instruction field

mnemonic	code binary	code hex	full name of destination
–	0000	0	no destination
BSR	0001	1	barrel-shifter/format adjuster control register
–	0010	2	reserved
RAMB	0011	3	RAMB
–	0100	4	reserved
RY	0101	5	bussave register Y
–	0110	6	reserved
–	0111	7	reserved
–	1000	8	reserved
PG	1001	9	page register
ACU(RAMA,*)	1010	A	ACUA
PO	1011	B	parallel data output buffer
RPO	1100	C	second parallel data output buffer (PCB5011 only)
SOY	1101	D	serial output register connected to Y-bus
ACU(ROM,*)	1110	E	ACUR
**	1111	F	register file

* fill in a mnemonic of the ACU-initialization field.
** fill in a mnemonic of the RFILE field.

Table 3.3-7 RFILE instruction field

mnemonic	code		full name of destination
	binary	hex	
–	0000	0	no destination
R1	0001	1	register 1
R2	0010	2	register 2
R3	0011	3	register 3
R4	0100	4	register 4
R5	0101	5	register 5
R6	0110	6	register 6
R7	0111	7	register 7
R8	1000	8	register 8
R9	1001	9	register 9
R10	1010	A	register 10
R11	1011	B	register 11
R12	1100	C	register 12
R13	1101	D	register 13
R14	1110	E	register 14
R15	1111	F	register 15

Table 3.3-8 ACU initialization (notes 1 and 2)

mnemonic	code		New values for:			
	binary	hex	AR	A	S	M
AR	000	0	source	A	S	M
AAR	001	1	source	source	S	M
SAR	010	2	source	A	source	M
A	011	3	AR	source	S	M
S	100	4	AR	A	source	M
M	101	5	AR	A	S	source
ASAR	110	6	source	source	source	M
AR1M	111	7	(source)!M	A	S	M

Table 3.3-9 ACU computation (notes 1 and 2)

mnemonic	code		New values for:			
	binary	hex	AR	A	S	M
	000	0	AR	A	S	M
INCA	001	1	(A+1)!M	(A+1)!M	S	M
DECA	010	2	(A–1)!M	(A–1)!M	S	M
STEP	011	3	(A+S)!M	(A+S)!M	S	M
INCS	100	4	(S+1)!M	A	(S+1)!M	M
A	101	5	(A)!M	A	S	M
S	110	6	(S)!M	A	S	M
REV	111	7	br(A+S)	A+S	S	M

Notes to Tables 3.3-8 and 3.3-9

1. The ACU fields for RAMA, RAMB and ROM are identical. The content of the field has a different meaning if it is for ACU initialization or address computation.
2. See section 2.3.2 on ACUs and PG register for explanation of !M and br(....).

Table 3.3-10 MPY instruction field

mnemonic	code binary	code hex	new ACR-value
–	000	0	ACR (HOLD)
0	001	1	P*Q
+ACR	010	2	P*Q + ACR
–ACR	011	3	P*Q – ACR
+ACRS	100	4	P*Q + ACR x 2^{-15}
–ACRS	101	5	P*Q – ACR x 2^{-15}
	other		reserved

Table 3.3-11 MOPS instruction field (note 1)

mnemonic	code binary	code hex	P-input of multiplier	Q-input of multiplier
*, *	0000	0	source on X-bus	source on Y-bus
, –	0001	1	source on X-bus	–(source on Y-bus)
MXL,*	0010	2	MXL	source on Y-bus
MXL, –*	0011	3	MXL	–(source on Y-bus)
*, MYL	0100	4	source on X-bus	MYL
MXL, MYL	0101	5	MXL	MYL
–1, –*	0110	6	–1	–(source on Y-bus)
–1, *	0111	7	–1	source on Y-bus
–1, MYL	1000	8	–1	MYL
	other		reserved	reserved

Note to Table 3.3-11

1. When the MPY-field contains 000, then independent of the MOPS-code the following is true.

mnemonic	code	P-input of multiplier	Q-input of multiplier
–	XXXX	MXL	MYL

* Fill in the mnemonic of the particular source (see SX and SY fields).

NAP

The NAP field contains the address of the next instruction to be executed if a branch condition is true.

Table 3.3-12 BR instruction field

mnemonic	code binary	code hex	function
GOTO	000	0	goto
CALL	001	1	subroutine call
RET	010	2	return from subroutine
RETI	100	4	return $\overline{\text{INT}}$ interrupt
	other		reserved

DEVELOPMENT DATA

Table 3.3-13 COND instruction field (notes 1 and 2)

mnemonic	code binary	code hex(X=0)	condition	mnemonic explanation
–	00000X	00	always true	
AN	00001X	02	SGNM = 1	accumulator negative
XO	00010X	04	OOR = 1	
–	00011X	06	reserved	
GE or NOT LT	00100X	08	$\overline{N.EXOR.V} = 1$	greater or equal to/not less than
NOT GT or LE	00101X	0A	(N.EXOR.V).OR.Z = 1	not greater than/less than or equal to
IFX	00110X	0C	IFA.AND.IFB.AND.IFC.AND.IFD = 1	
HI or NOT LS	00111X	0E	$\overline{C.OR.Z} = 1$	higher/not less than or equal to
OFL	01000X	10	OORL.OR.VL = 1	system overflow
XOL	01001X	12	OORL = 1	extractor overflow
AOL	01010X	14	OVFL = 1	accumulator overflow
VL	01011X	16	VL = 1	
Z or EQ	01100X	18	Z = 1	
N	01101X	1A	N = 1	
C	01110X	1C	C = 1	
V	01111X	1E	V = 1	
SIX	10000X	20	SIXACK = 1	
SOX	10001X	22	SOXACK = 1	
SIY	10010X	24	SIYACK = 1	
SOY	10011X	26	SOYACK = 1	
ACU(RAMA)	10100X	28	ACA = 1	
ACU(RAMB)	10101X	2A	ACB = 1	
ACU(ROM)	10110X	2C	ACR = 1	
–	10111X	2E	reserved	
IFA	11000X	30	IFA = 1	
IFB	11001X	32	IFB = 1	
IFC	11010X	34	IFC = 1	
IFD	11011X	36	IFD = 1	
–	11100X	38	reserved	
–	11101X	3A	reserved	
–	11110X	3C	reserved	
–	11111X	3E	reserved	

X = 0: branch takes place when condition = true
X = 1: branch takes place when condition = false

Notes to Table 3.3-13

1. The mnemonic names GE, LT, GT, LE, HI, and LS refer to situations where the flag setting is a result of a subtraction (SUB) of operands A and B. For example, GE means that A is greater than or equal to B.
2. OOR and OORL are set to logic 1 one clock cycle after the ACR register has been filled with an out-of-range value. OOR is set to logic 0 one clock cycle after the ACR register has been filled with a value with the specified range.

DATA

Data is a 16-bit data word which is transmitted on the X and Y-bus.

4.0 ELECTRICAL SPECIFICATION

4.1 ABSOLUTE MAXIMUM RATINGS (NOTE 1)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	−0.5	+ 6.5	V
Voltage at any input		V_I	−0.5	V_{DD} + 0.5	V
Input/output current		$I_{I/O}$	−	5	mA
Total power dissipation	note 2				
	PLCC 68	P_{tot}	−	1	W
	PGA 144	P_{tot}	−	1	W
Operating ambient temperature range	PCB5010/11	T_{amb}	0	+ 70	°C
	PCF5010/11	T_{amb}	−40	+ 85	°C
Storage temperature range		T_{stg}	−55	+ 150	°C

Note to the Absolute Maximum Ratings

1. Stress above those listed under 'Absolute Maximum Ratings' may cause permanent damage to this device. This is a stress rating only and functional operating of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute rating conditions for extended periods may affect device reliability.
2. This value is based on the maximum allowable die temperature and thermal resistance of the packages.

DEVELOPMENT DATA

4.2 DC CHARACTERISTICS

V_{DD} = 5 V ± 5%; V_{SS} = 0 V; T_{amb} = 0 to + 70 °C; all voltages with respect to V_{SS}; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.75	−	5.25	V
Supply current	notes 1 and 2					
PCB5010		I_{DD}	−	100	130	mA
PCB5011		I_{DD}	−	100	120	mA
HIGH level input voltage	except CLK	V_{IH}	2.0	−	V_{DD} + 0.5	V
HIGH level input voltage	CLK only	V_{IH1}	2.4	−	V_{DD} + 0.5	V
LOW level input voltage		V_{IL}	−0.5	−	0.8	V
LOW level input current	V_I = 0.4 V	$-I_{IL}$	−	−	100	μA
HIGH level input current	V_I = 2.0 V	$-I_{IH}$	−	−	100	μA
HIGH level output voltage	$-I_{OH}$ = 100 μA	V_{OH}	2.4	−	−	V
LOW level output voltage	I_{OL} = 2.0 mA	V_{OL}	−	−	0.4	V

Notes to the DC characteristics

1. $I_{DD(typ.)}$ is based on V_{DD} = 5 V, T_{amb} = 22 °C and under operating conditions (excluding the reset condition).
2. $I_{DD(max.)}$ is based on $V_{DD} = V_{DD(max.)}$, $\overline{RST}$ = 0, f = 8.2 MHz and all other pins disconnected.

4.3 AC CHARACTERISTICS

V_{DD} = 5 V ± 5%; V_{SS} = 0 V , T_{amb} = 0 °C to 70 °C (PCB5010/5011); C_L 80 pF (capacitive load per output);
Timing measurements are taken at 2.0 V for logic 1 and 0.8 V for logic 0; unless otherwise specified.

no.	parameter	min.	max.	unit	note
0	CLK period	122	2000	ns	
1	CLK width HIGH	55	1000	ns	
2	CLK width LOW (time 2)	55	1000	ns	
3	CLK HIGH to SYNC HIGH	20	50	ns	
4	CLK HIGH to Ax valid	20	60	ns	
5	CLK HIGH to R/$\overline{W}$ LOW	20	85	ns	
6	CLK HIGH to R/$\overline{W}$ HIGH	20	85	ns	x = 0 . . . 15
7	CLK LOW to $\overline{DS}$ LOW	10	45	ns	
8	R/$\overline{W}$ LOW to $\overline{DS}$ LOW	0	–	ns	
9	CLK HIGH to $\overline{DS}$ HIGH	10	45	ns	
10	$\overline{DS}$ HIGH to R/$\overline{W}$ HIGH	0	–	ns	
11a	$\overline{DS}$ HIGH to Ax invalid	5	–	ns	x = 0 . . . 11
11b	$\overline{DS}$ HIGH to Ay invalid	0	–	ns	y = 12 . . . 15
12	$\overline{DS}$ width LOW	*	–	ns	
13	Dx access time	–	60	ns	
14	Dx hold time	0	–	ns	x = 0 . . . 15
15	Dx valid to $\overline{DS}$ HIGH	50	–	ns	x = 0 . . . 15
16	$\overline{DS}$ HIGH to Dx invalid	5	–	ns	x = 0 . . . 15
17	$\overline{WAIT}$ set-up time	15	–	ns	
18	$\overline{WAIT}$ hold time	30	–	ns	
19	$\overline{INT}$ set-up time	5	–	ns	
20	$\overline{INT}$ hold time	30	–	ns	
21	CLK HIGH to $\overline{IACK}$ LOW	–	60	ns	
22	CLK HIGH to $\overline{IACK}$ HIGH	–	60	ns	
23	IFA, IFB, IFC, IFD set-up time	5	–	ns	
24	IFA, IFB, IFC, IFD hold time	30	–	ns	
25	$\overline{RST}$ set-up time	10	–	ns	
26	$\overline{RST}$ hold time	30	–	ns	
27	CLK HIGH to PAx or ARRx valid	20	60	ns	x = 0 . . . 9 or 0 . 8
28	CLK HIGH to RR/$\overline{W}$ LOW	20	85	ns	
29	CLK HIGH to RR/$\overline{W}$ HIGH	20	85	ns	
30	CLK LOW to $\overline{RDS}$ LOW	10	45	ns	
31	RR/$\overline{W}$ LOW to $\overline{RDS}$ LOW	0	–	ns	
32	CLK HIGH to $\overline{RDS}$ HIGH	10	45	ns	
33	$\overline{RDS}$ HIGH to RR/$\overline{W}$ HIGH	0	–	ns	
34	$\overline{RDS}$ HIGH to ARRx invalid	5	–	ns	
35	$\overline{RDS}$ width LOW	*	–	ns	
36	RDx access time	–	60	ns	x = 0 . . . 15
37	RDx hold time	0	–	ns	x = 0 . . . 15
38	RDx valid to $\overline{RDS}$ HIGH	50	–	ns	x = 0 . . . 15
39	$\overline{RDS}$ HIGH to RDx invalid	5	–	ns	x = 0 . . . 15
40	COX, CIX, COY, CIY period	244	–	ns	
41	COX, CIY, COY, CIY width HIGH	110	–	ns	
42	COX, CIX, COY, CIY width LOW	110	–	ns	
43	COX(Y) LOW to $\overline{SOX(Y)RQ}$ LOW	–	40	ns	
44	COX(Y) LOW to $\overline{SOX(Y)RQ}$ HIGH	–	40	ns	
45	$\overline{SOX(Y)EN}$ set-up time	40	–	ns	
46	$\overline{SOX(Y)EN}$ hold time	10	–	ns	
47	COX(Y) LOW to next DOX(Y) valid	–	40	ns	
48	$\overline{SOX(Y)EN}$ LOW to DOX(Y) valid	–	40	ns	
49	$\overline{SOX(Y)EN}$ to DOX(Y) 3-state	–	40	ns	
53	CIX(Y) LOW to $\overline{SIX(Y)RQ}$ LOW	–	40	ns	
54	CIX(Y) LOW to $\overline{SIX(Y)RQ}$ HIGH	–	40	ns	
55	$\overline{SIX(Y)EN}$ set-up time	30	–	ns	
56	$\overline{SIX(Y)EN}$ hold time	10	–	ns	
57	DIX, DIY set-up time	10	–	ns	
58	DIX, DIY hold time	40	–	ns	
59	PDx access time	–	60	ns	x = 0 . . . 39
60	PDx hold time	20	–	ns	x = 0 . . . 39

* Value given is equal to (time 2) – 15 ns.

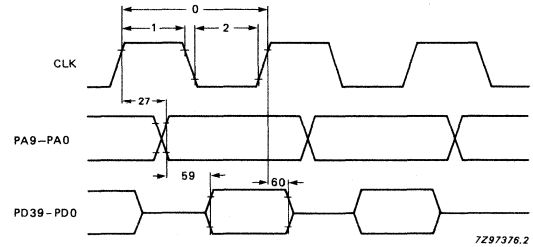


Fig. 4.3-1 Program memory access timing (for PCB5011 only).

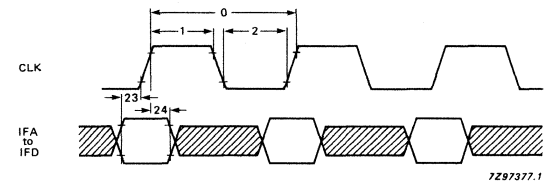


Fig. 4.3-2 User flag timing.

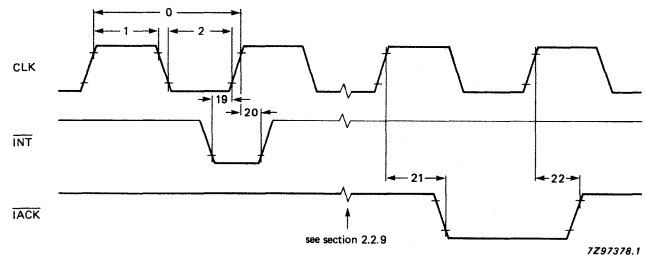


Fig. 4.3-3 Interrupt timing.

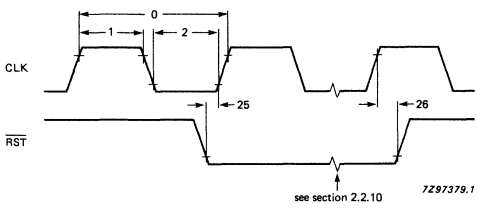


Fig. 4.3-4 Reset timing.

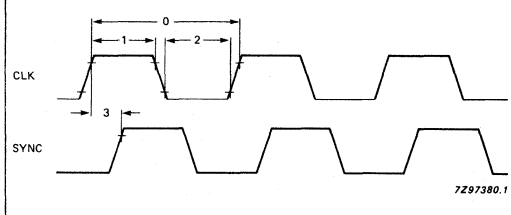
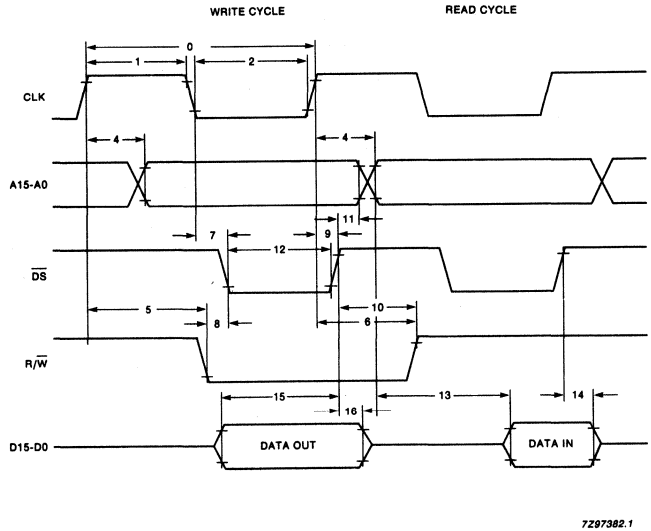


Fig. 4.3-5 Synchronization timing.

DEVELOPMENT DATA



Note: (part of) the signals A15 – A0 can be used just as hardware controlling outputs if they are not needed for addressing external RAM.

Fig. 4.3-6 Parallel I/O timing; $\overline{\text{WAIT}}$ inactive.

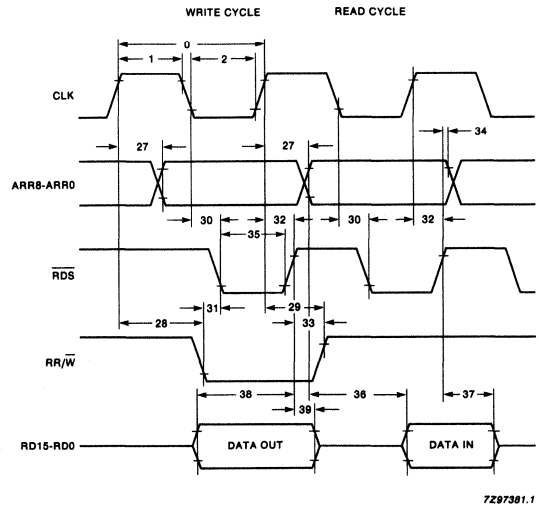
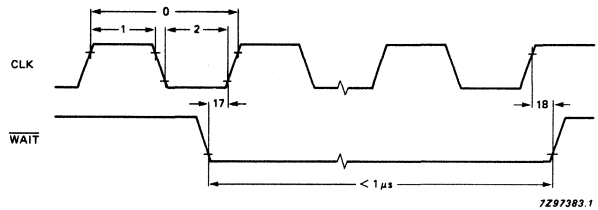


Fig. 4.3-7 Second parallel I/O timing; $\overline{\text{WAIT}}$ inactive (for PCB5011 only).



Note: As long as $\overline{WAIT}$ = 0 all clocked (by CLK) processor actions are suspended i.e. the internal status and all signals remain unchanged.

Fig. 4.3-8 $\overline{WAIT}$ signal timing.

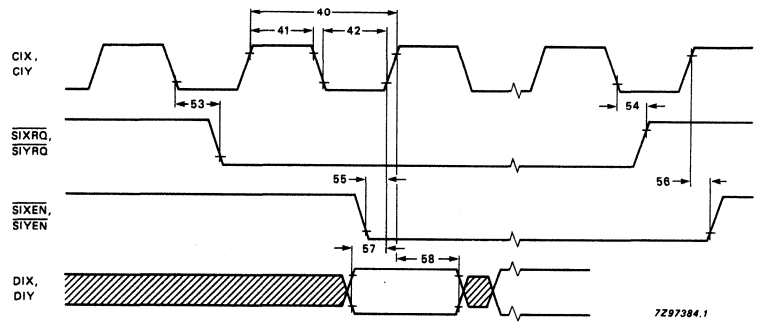


Fig. 4.3-9 Serial input timing.

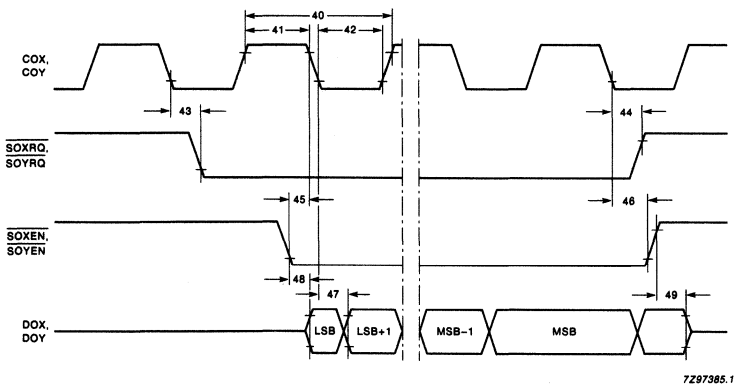


Fig. 4.3-10 Serial output timing.

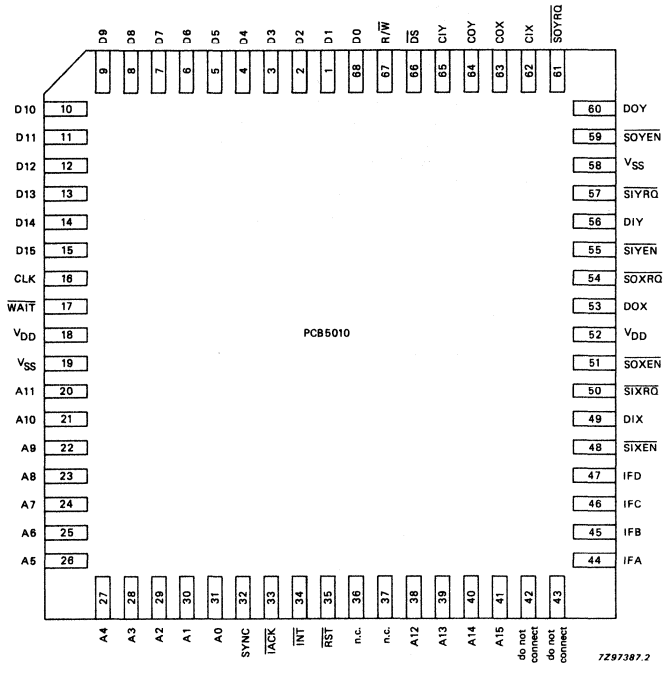


Fig. 5.1-2 Pinning for the PCB5010 (PLCC).

DEVELOPMENT DATA

5.2 PCB5011 PACKAGE OUTLINE (dimensions in mm)

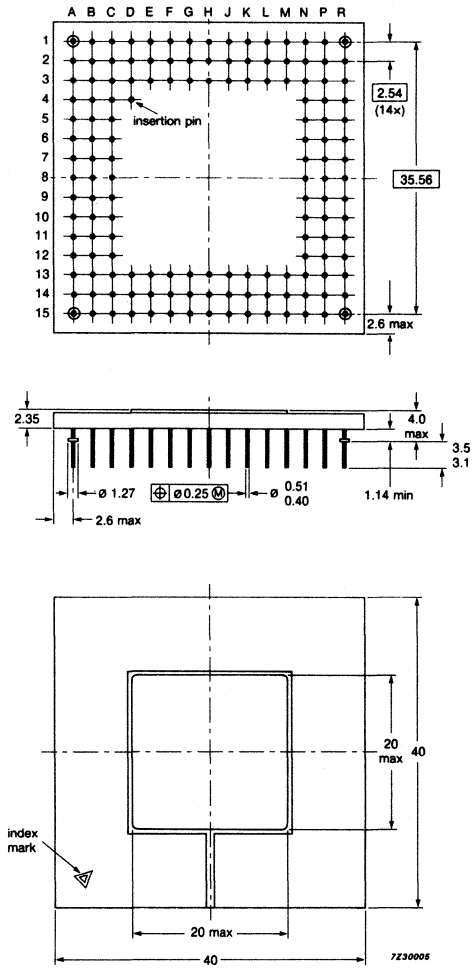


Fig. 5.2-1 144-pin grid array (PGA) (NO275) package for the PCB5011.

5.3 PIN ASSIGNMENT FOR Fig. 5.2-1

PCB5011 signal name	pin number
V_{DD}	N8, C8
V_{SS}	N9, A2
CLK	Q2
$\overline{RST}$	L14
D15	P3
D14	N4
D13	Q1
D12	P2
D11	N3
D10	M3
D9	P1
D8	N2
D7	L3
D6	M2
D5	N1
D4	M1
D3	L2
D2	L1
D1	K3
D0	K2
A15	A1
A14	B2
A13	C3
A12	C4
A11	N5
A10	Q3
A9	P5
A8	Q4
A7	N6
A6	P6
A5	Q5
A4	P7
A3	N7
A2	Q6
A1	Q7
A0	P8
R/$\overline{W}$	J2
$\overline{DS}$	K1
$\overline{WAIT}$	P4
DIX	B1

PCB5011 signal name	pin number
$\overline{SIXEN}$	C2
$\overline{SIXRQ}$	D2
CIX	D3
DIY	H3
$\overline{SIYEN}$	J3
$\overline{SIYRQ}$	H1
CIY	J1
DOX	C1
$\overline{SOXEN}$	E2
$\overline{SOXRQ}$	E3
COX	D1
DOY	G1
$\overline{SOYEN}$	F1
$\overline{SOYRQ}$	H2
COY	G3
$\overline{INT}$	M15
$\overline{IACK}$	M14
SYNC	N14
IFA	F3
IFB	F2
IFC	E1
IFD	G2
PA9	Q13
PA8	P12
PA7	N11
PA6	P13
PA5	Q14
PA4	N12
PA3	N13
PA2	P14
PA1	Q15
PA0	M13

(continued on next page)

DEVELOPMENT DATA

PCB5011 signal name	pin number
PD39	C5
PD38	B4
PD37	A3
PD36	A4
PD35	B5
PD34	A5
PD33	C6
PD32	B6
PD31	B7
PD30	A6
PD29	A7
PD28	C7
PD27	A8
PD26	B8
PD25	A9
PD24	A10
PD23	C9
PD22	B9
PD21	A11
PD20	B10
PD19	C10
PD18	A12
PD17	B11
PD16	A13
PD15	C11
PD14	B12
PD13	A14
PD12	B13
PD11	C12
PD10	G15
PD9	G13
PD8	K14
PD7	L15
PD6	J14
PD5	J13
PD4	K15
PD3	J15
PD2	H14
PD1	H15
PD0	H13
ARR8	Q8
ARR7	Q9
ARR6	Q10
ARR5	P9
ARR4	P10
ARR3	N10
ARR2	Q11
ARR1	P11
ARR0	Q12

PCB5011 signal name	pin number
RD15	F15
RD14	G14
RD13	F14
RD12	F13
RD11	E15
RD10	E14
RD9	D15
RD8	C15
RD7	D14
RD6	E13
RD5	C14
RD4	B15
RD3	D13
RD2	C13
RD1	B14
RD0	A15
RR/$\overline{W}$	L13
$\overline{RDS}$	N15
Do not connect	K13
Do not connect	P15
Do not connect	B3

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C552-4 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C552-4 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C552-4" is used to refer to both family members:

- PCB83C552-4: 8 K bytes mask-programmable ROM
- PCB80C552-4: ROM-less version of the PCB84C552-4

This I/O intensive device provides architectural enhancements to function as a controller in the field of automotive electronics, specifically engine management and gear box control.

The PCB83C552-4 contains a non-volatile 8 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a fifteen-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC with pulse width modulated outputs, two serial interfaces (UART and I^2C-bus), a 'watchdog' timer and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C552-4 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16 MHz crystal, 58% of the instructions are executed in 0.75 μs and 40% in 1.5 μs. Multiply and divide instructions require 3 μs.

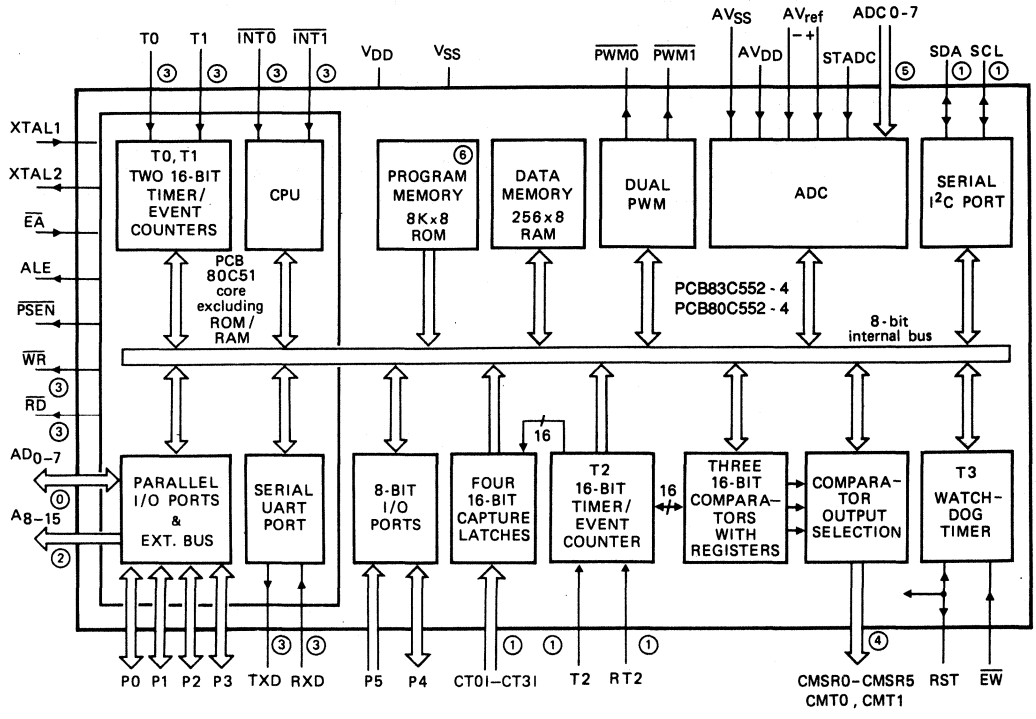
Features

- 80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- A 10-bit ADC with 8 multiplexed analog inputs
- Two 8-bit resolution, Pulse Width Modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART compatible with the standard PCB80C51
- On-chip watchdog timer
- Operating ambient temperature range: PCB83C552-4 0 to +70 °C
  PCF83C552-4 −40 to +85 °C
  PCA83C552-4 −40 to +125 °C
- XTAL frequency: 1.2 to 16 MHz

PACKAGE OUTLINES

PCA/PCB/PCF83C552-4WP:
PCA/PCB/PCF80C552-4WP: 68-lead plastic leaded chip carrier (PLCC); (SOT188AA; AGA).

PCA/PCB/PCF83C552-4H:
PCA/PCB/PCF80C552-4H: 80-lead quad flat-pack; plastic (SOT219).



7Z97647.8

⓪ alternative function of port 0
① alternative functions of port 1
② alternative function of port 2
③ alternative function of port 3
④ alternative function of port 4
⑤ alternative function of port 5
⑥ not present in PCB80C552 - 4

Fig.1 Block diagram.

DEVELOPMENT DATA

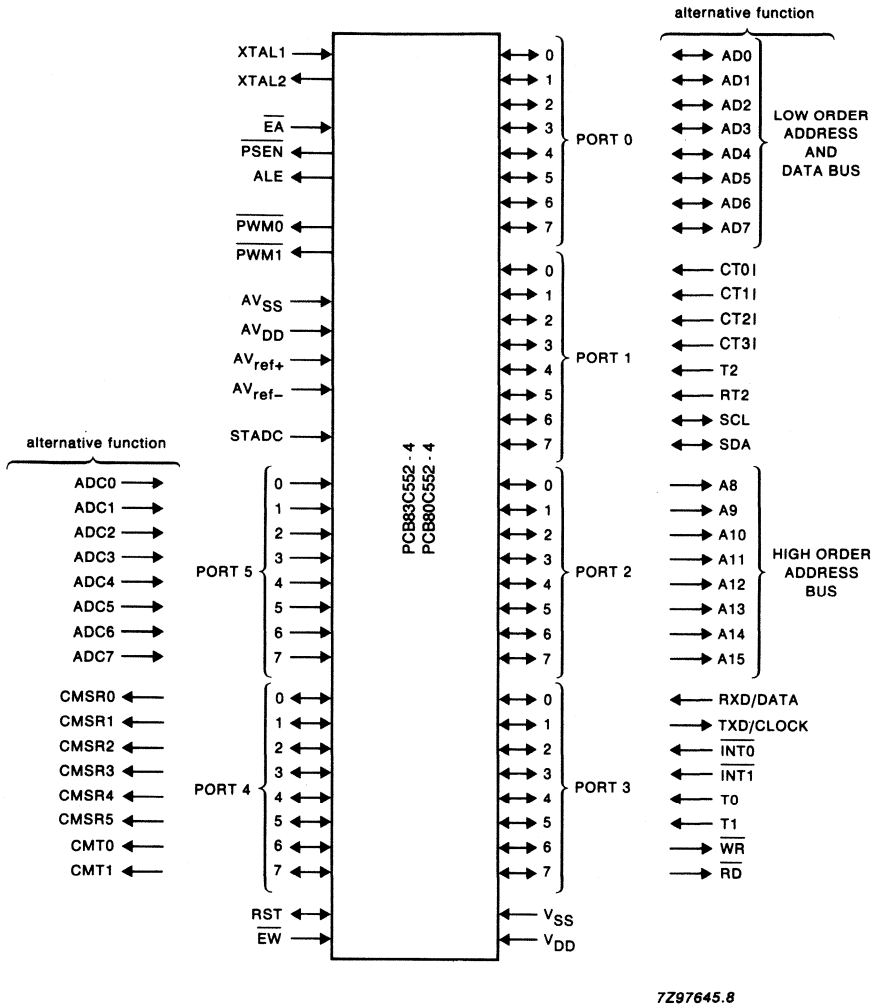


Fig.2 Functional diagram.

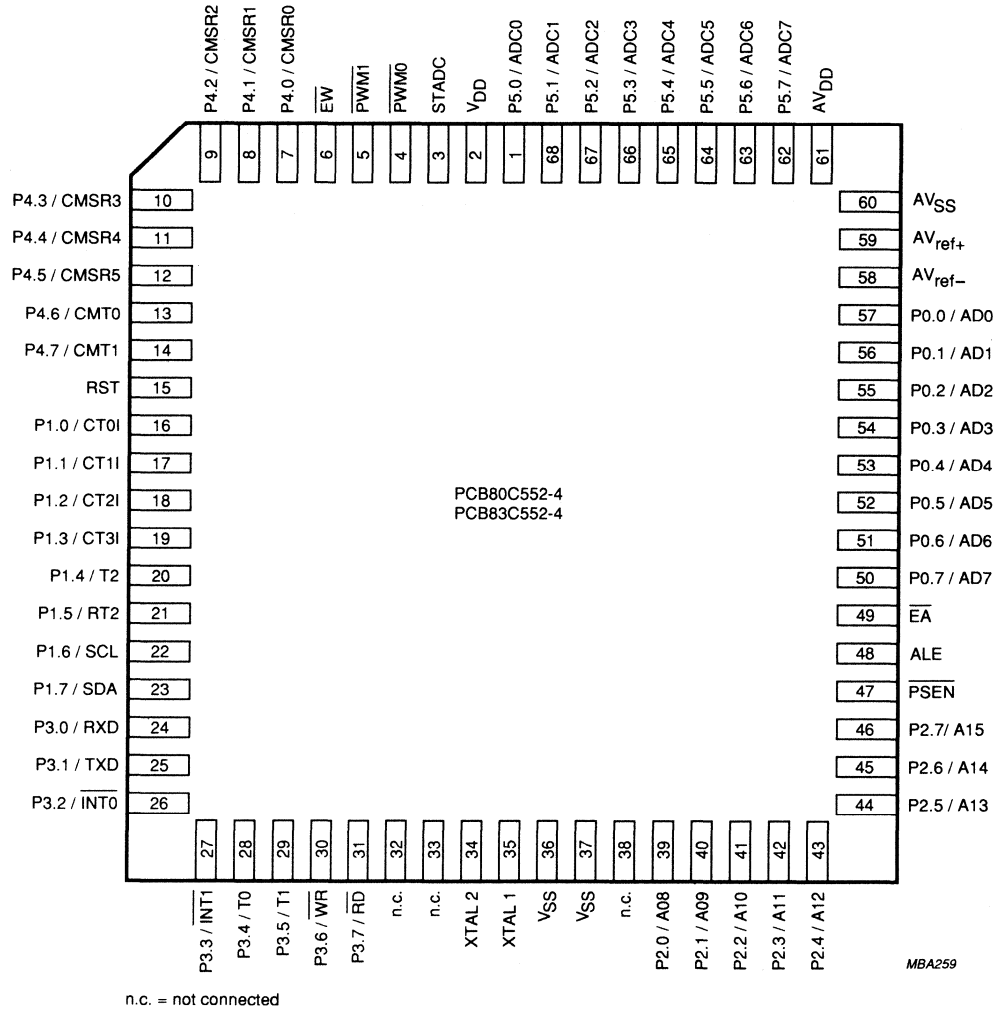
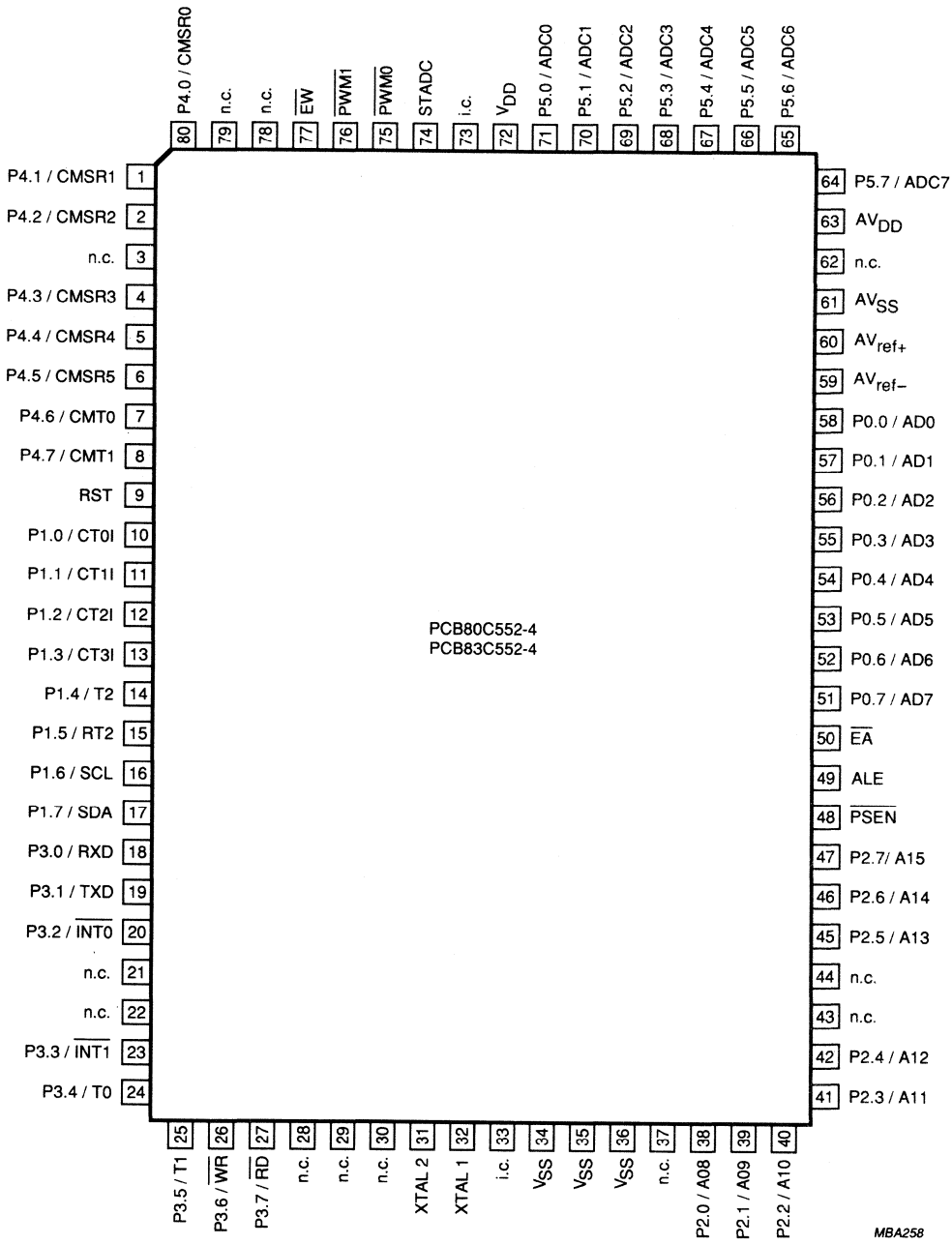


Fig.3(a) Pinning diagram; for SOT188AA; AGA package.

DEVELOPMENT DATA



n.c. = not connected
i.c. = internally connected (do not use)

Fig.3(b) Pinning diagram; for SOT219 package.

PINNING (pin numbers refer to the PLCC68 package)

2	V_{DD}	**Digital power supply**: + 5 V power supply pin during normal operation, Idle mode and Power-down mode
3	STADC	**Start ADC operation**: Input starting analog to digital conversion (ADC operation can also be started by software). This pin must not float
4	$\overline{PWM0}$	**Pulse width** modulation output 0
5	$\overline{PWM1}$	**Pulse width** modulation output 1
6	$\overline{EW}$	**Enable watchdog timer**: Enable for T3 watchdog timer and disable Power-down mode. This pin must not float
		Port 4
7-14	P4.0-P4.7	8-bit quasi-bidirectional I/O port

Port pin	Alternative function	
P4.0	CMSR0	Timer T2: compare and set/reset outputs on a match with timer T2
P4.1	CMSR1	
P4.2	CMSR2	
P4.3	CMSR3	
P4.4	CMSR4	
P4.5	CMSR5	
P4.6	CMT0	Timer T2: compare and toggle outputs on a match with timer T2
P4.7	CMT1	

15	RST	**Reset**: Input to reset the PCB83C552. It also provides a reset pulse as output when timer T3 overflows.
		Port 1
16-23	P1.0-P1.7	8-bit quasi-bidirectional I/O port

Port pin	Alternative function	
P1.0	CT0I	Capture timer input signals for timer T2
P1.1	CT1I	
P1.2	CT2I	
P1.3	CT3I	
P1.4	T2	: T2 event input. Rising edge triggered
P1.5	RT2	: T2 timer reset signal. Rising edge triggered
P1.6	SCL	: Serial port clock line I^2C-bus
P1.7	SDA	: Serial port data line I^2C-bus

		Port 3
24-31	P3.0-P3.7	8-bit quasi-bidirectional I/O port

Port pin	Alternative function	
P3.0	RXD	: Serial input port
P3.1	TXD	: Serial output port
P3.2	$\overline{INT0}$	: External interrupt
P3.3	$\overline{INT1}$	: External interrupt
P3.4	T0	: Timer 0 external input
P3.5	T1	: Timer 1 external input
P3.6	$\overline{WR}$	: External data memory write strobe
P3.7	$\overline{RD}$	: External data memory read strobe

32, 33	Not connected

34	XTAL2	**Crystal input 2:** output of the inverting amplifier that forms the oscillator. Left open-circuit when an external oscillator clock is used.
35	XTAL1	**Crystal input 1:** input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator clock signal when an external oscillator is used.
36, 37	V_{SS}	**Two digital** ground pins
38		Not connected
		Port 2
39-46	P2.0-P2.7	8-bit quasi-bidirectional I/O port Port pin — Alternative function P2.0-P2.7 — High-order address byte for external memory (A08-A15)
47	$\overline{PSEN}$	**Program store enable:** active LOW read strobe to external program memory
48	ALE	**Address latch enable:** latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods. During an external data memory access one ALE pulse is skipped. ALE can drive up to 8 LSTTL inputs and handles CMOS inputs without an external pull-up.
49	$\overline{EA}$	**External access:** When $\overline{EA}$ is held at TTL level HIGH, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When $\overline{EA}$ is held at TTL LOW level, the CPU executes out of external program memory. $\overline{EA}$ is not allowed to float.
		Port 0
50-57	P0.7-P0.0	8-bit binary I/O port Port pin — Alternative function P0.0-P0.7 — Multiplexed low-order address and data bus of external memory (AD0-AD7)
58	$AV_{ref}-$	**Low end** of analog to digital conversion reference resistor
59	$AV_{ref}+$	**High end** of analog to digital conversion reference resistor
60	AV_{SS}	**Analog** ground
61	AV_{DD}	**Analog** power supply
		Port 5
62-68,1	P5.7-P5.0	8-bit input port Port pin — Alternative function P5.0-P5.7 — Eight input channels to ADC (ADC0-ADC7)

To avoid a 'latch-up' effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0.5 V or V_{SS} − 0.5 V respectively.

DEVELOPMENT DATA

DC CHARACTERISTICS

All voltages measured with respect to V_{SS} unless otherwise specified

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
PCB83C552-4	T_{amb} = 0 to +70 °C	V_{DD}	4.0	6.0	V
PCF83C552-4	T_{amb} = −40 to +85 °C	V_{DD}	4.0	6.0	V
PCA83C552-4	T_{amb} = −40 to +125 °C	V_{DD}	4.5	5.5	V
Supply current operating	note 1				
PCB83C552-4	f_{osc} = 16 MHz	I_{DD}	–	45	mA
PCF83C552-4	f_{osc} = 16 MHz	I_{DD}	–	45	mA
PCA83C552-4	f_{osc} = 16 MHz	I_{DD}	–	40	mA
Supply current Idle mode	note 2				
PCB83C552-4	f_{osc} = 16 MHz	I_{ID}	–	10	mA
PCF83C552-4	f_{osc} = 16 MHz	I_{ID}	–	10	mA
PCA83C552-4	f_{osc} = 16 MHz	I_{ID}	–	9	mA
Power-down current	note 3; $2\ V < V_{PD} < V_{DD}$ max				
PCB83C552-4		I_{PD}	–	50	μA
PCF83C552-4		I_{PD}	–	50	μA
PCA83C552-4		I_{PD}	–	150	μA
Inputs					
LOW level input voltage (except $\overline{EA}$, P1.6/SCL, P1.7/SDA)		V_{IL}	−0.5	$0.2V_{DD}-0.1$	V
LOW level input voltage ($\overline{EA}$)		V_{IL1}	−0.5	$0.2V_{DD}-0.3$	V
LOW level input voltage (P1.6/SCL, P1.7/SDA)		V_{IL2}	−0.5	$0.3V_{DD}$	V
HIGH level input voltage (except RST, XTAL1, P1.6/SCL, P1.7/SDA)		V_{IH}	$0.2V_{DD}+0.9$	$V_{DD}+0.5$	V
HIGH level input voltage (RST and XTAL1)		V_{IH1}	$0.7V_{DD}$	$V_{DD}+0.5$	V
HIGH level input voltage (P1.6/SCL, P1.7/SDA)		V_{IH2}	$0.7V_{DD}$	6.0	V
Input current logic 0 (Ports 1, 2, 3 and 4; except P1.6/SCL, P1.7/SDA)	V_I = 0.45 V	$-I_{IL}$	–	50	μA

parameter	conditions	symbol	min.	max.	unit
Input current logic 1 to 0 transition (Ports 1, 2, 3 and 4; except P1.6/SCL, P1.7/SDA)	V_I = 2.0 V	$-I_{TL}$	–	650	μA
Input leakage current (Port 0, Port 5, $\overline{EA}$, STADC, $\overline{EW}$)	0.45 V < V_I < V_{DD}	$\pm I_{LI1}$	–	10	μA
Input leakage current (P1.6/SCL, P1.7/SDA)	0 V < V_I < 6.0 V 0 V < V_{DD} < V_{DD}max	$\pm I_{LI2}$	–	10	μA
Outputs					
LOW level output voltage (Ports 1, 2, 3 and 4; except P1.6/SCL, P1.7/SDA)	I_{OL} = 1.6 mA	V_{OL}	–	0.45	V
LOW level output voltage (Port 0, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$)	I_{OL} = 3.2 mA	V_{OL1}	–	0.45	V
LOW level output voltage (P1.6/SCL, P1.7/SDA)	I_{OL} = 3.0 mA	V_{OL2}	–	0.40	V
HIGH level output voltage (Ports 1, 2, 3 and 4; except P1.6/SCL, P1.7/SDA)	V_{DD} = 5 V + 10% $-I_{OH}$ = 60 μA $-I_{OH}$ = 25 μA $-I_{OH}$ = 10 μA	V_{OH} V_{OH} V_{OH}	2.4 0.75V_{DD} 0.9V_{DD}	– – –	V V V
HIGH level output voltage (Port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$)	V_{DD} = 5 V + 10% $-I_{OH}$ = 400 μA $-I_{OH}$ = 150 μA $-I_{OH}$ = 40 μA	V_{OH1} V_{OH1} V_{OH1}	2.4 0.75V_{DD} 0.9V_{DD}	– – –	V V V
HIGH level output voltage (RST)	$-I_{OH}$ = 400 μA $-I_{OH}$ = 120 μA	V_{OH2} V_{OH2}	2.4 0.8V_{DD}	– –	V V
RST pull-down resistor		R_{RST}	50	150	kΩ
Capacitance of I/O buffer	Test freq. = 1 MHz T_{amb} = 25 °C	$C_{I/O}$	–	10	pF

DEVELOPMENT DATA

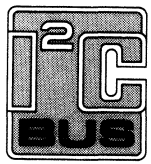
CHARACTERISTICS OF THE ADC

parameter	conditions	symbol	min.	max.	unit
Analog supply voltage					
PCB83C552-4	$AV_{DD} = V_{DD} \pm 0.2$ V	AV_{DD}	4.0	6.0	V
PCF83C552-4	$AV_{DD} = V_{DD} \pm 0.2$ V	AV_{DD}	4.0	6.0	V
PCA83C552-4	$AV_{DD} = V_{DD} \pm 0.2$ V	AV_{DD}	4.5	5.5	V
Analog supply current operating	Port 5 = 0 to AV_{DD}	AI_{DD}	–	1.2	mA
Analog supply current Idle mode					
PCB83C552-4		AI_{ID}	–	50	μA
PCF83C552-4		AI_{ID}	–	50	μA
PCA83C552-4		AI_{ID}	–	100	μA
Power-down current	$2\text{ V} < AV_{PD} < AV_{DD}max$				
PCB83C552-4		AI_{PD}	–	50	μA
PCF83C552-4		AI_{PD}	–	50	μA
PCA83C552-4		AI_{PD}	–	100	μA
Analog inputs					
Analog input voltage		AV_{IN}	$AV_{SS}-0.2$	$AV_{DD}+0.2$	V
Reference voltage		AV_{ref-}	$AV_{SS}-0.2$	–	V
		AV_{ref+}	–	$AV_{DD}+0.2$	V
Resistance between AV_{ref+} and AV_{ref-}		R_{ref}	10	50	kΩ
Analog input capacitance		C_{IA}	–	15	pF
Sampling time		t_{ADS}	–	$8t_{CY}$	μs
Conversion time (including sample time)		t_{ADC}	–	$50t_{CY}$	μs
Differential non-linearity	notes 4, 5 and 10	DL_e	–	± 1	LSB
Integral non-linearity	notes 4 and 6	IL_e	–	± 2	LSB
Offset error	notes 4 and 8	OS_e	–	± 2	LSB
Gain error	notes 4 and 7	G_e	–	± 0.4	%
Absolute voltage error	notes 4 and 9	A_e	–	± 3	LSB
Channel to channel matching		M_{ctc}	–	± 1	LSB
Crosstalk between P5 inputs	0 to 100 kHz	C_t	–	–60	dB

Notes to the DC characteristics

1. The operating supply current is measured with all output pins disconnected; XTAL1 is driven with $t_r = t_f = 10$ ns; $V_{IL} = V_{SS} + 0.5$ V; $V_{IH} = V_{DD} - 0.5$ V; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = P1.6 = P1.7 = $\overline{EW} = V_{DD}$; STADC = V_{SS}.
2. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10$ ns; $V_{IL} = V_{SS} + 0.5$ V; $V_{IH} = V_{DD} - 0.5$ V; XTAL2 not connected; $\overline{EA}$ = Port 0 = P1.6 = P1.7 = $\overline{EW} = V_{DD}$; RST = STADC = V_{SS}.
3. The power-down current is measured with all output pins disconnected; XTAL2 not connected; $\overline{EA}$ = Port 0 = P1.6 = P1.7 = $\overline{EW} = V_{DD}$; RST = STADC = XTAL1 = V_{SS}.
4. $AV_{ref+} = 5.12$ V; $AV_{ref-} = 0$ V; $AV_{DD} = 5.0$ V.
5. The differential non-linearity (DL_e) is the difference between the actual step width and the ideal step width.
6. The integral non-linearity (IL_e) is the peak difference between the centre of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error.
7. The gain error (G_e) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve.
8. The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve after removing gain error, and a straight line which fits the ideal transfer curve. The offset error is constant at every point of the actual transfer curve.
9. The absolute voltage error (A_e) is the maximum difference between the centre of the steps of the actual transfer curve of the not calibrated ADC and the ideal transfer curve.
10. The ADC is monotonic, there are no missing codes.
11. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the low level output voltage of ALE and Ports 1, 3 and 4. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the most adverse condition (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such events it may be required to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger strobe input.
12. Capacitive loading on Ports 0 and 2 may cause the high level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{DD} specification when the address bits are stabilizing.

DEVELOPMENT DATA



Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

AC CHARACTERISTICS

PCB83C552-4: V_{DD} = 5 V ± 20%; T_{amb} = 0 to +70 °C
PCF83C552-4: V_{DD} = 5 V ± 20%; T_{amb} = −40 to +85 °C
PCA83C552-4: V_{DD} = 5 V ± 10%; T_{amb} = −40 to +125 °C

C_L = 100 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 80 pF for all other outputs unless specified (see Figs 22, 23 and 24)

parameter	symbol	f_{osc} = 16 MHz		f_{osc} = 12 MHz		f_{osc} = variable		unit
		min.	max.	min.	max.	min.	max.	
Program memory								
ALE pulse duration	t_{LL}	85	–	127	–	$2t_{CK}-40$	–	ns
Address set-up time to ALE	t_{AL}	8	–	28	–	$t_{CK}-55$	–	ns
Address hold time after ALE	t_{LA}	28	–	48	–	$t_{CK}-35$	–	ns
Time from ALE to valid instruction input	t_{LIV}	–	150	–	233	–	$4t_{CK}-100$	ns
Time from ALE to control pulse $\overline{PSEN}$	t_{LC}	23	–	43	–	$t_{CK}-40$	–	ns
Control pulse duration $\overline{PSEN}$	t_{CC}	143	–	205	–	$3t_{CK}-45$	–	ns
Time from $\overline{PSEN}$ to valid instruction input	t_{CIV}	–	83	–	145	–	$3t_{CK}-105$	ns
Input instruction hold time after $\overline{PSEN}$	t_{CI}	0	–	0	–	0	–	ns
Input instruction float delay after $\overline{PSEN}$	t_{CIF}	–	38	–	59	–	$t_{CK}-25$	ns
Address to valid instruction input	t_{AIV}	–	208	–	312	–	$5t_{CK}-105$	ns
Address float delay after $\overline{PSEN}$	t_{AFC}	–	10	–	10	–	10	ns

parameter	symbol	f_{osc} = 16 MHz		f_{osc} = 12 MHz		f_{osc} = variable		unit
		min.	max.	min.	max.	min.	max.	
External data memory								
RD pulse duration	t_{RR}	275	–	400	–	$6t_{CK}-100$	–	ns
WR pulse duration	t_{WW}	275	–	400	–	$6t_{CK}-100$	–	ns
Address set up time to ALE	t_{AL}	8	–	28	–	$t_{CK}-55$	–	ns
Address hold time after ALE	t_{LA}	28	–	48	–	$t_{CK}-35$	–	ns
RD to valid data input	t_{RD}	–	148	–	252	–	$5t_{CK}-165$	ns
Data hold time after $\overline{RD}$	t_{DR}	0	–	0	–	0	–	ns
Data float delay after $\overline{RD}$	t_{DFR}	–	55	–	97	–	$2t_{CK}-70$	ns
Time from ALE to valid data input	t_{LD}	–	350	–	517	–	$8t_{CK}-150$	ns
Address to valid data input	t_{AD}	–	398	–	585	–	$9t_{CK}-165$	ns
Time from ALE to $\overline{RD}$ or $\overline{WR}$	t_{LW}	138	238	200	300	$3t_{CK}-50$	$3t_{CK}+50$	ns
Time from address to $\overline{RD}$ or $\overline{WR}$	t_{AW}	120	–	203	–	$4t_{CK}-130$	–	ns
Time from $\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	t_{WHLH}	23	103	43	123	$t_{CK}-40$	$t_{CK}+40$	ns
Data valid to $\overline{WR}$ transition	t_{DWX}	3	–	23	–	$t_{CK}-60$	–	ns
Data set-up time before $\overline{WR}$	t_{DW}	288	–	433	–	$7t_{CK}-150$	–	ns
Data hold time after $\overline{WR}$	t_{WD}	13	–	33	–	$t_{CK}-50$	–	ns
Address float delay after $\overline{RD}$	t_{AFR}	–	0	–	0	–	0	ns

DEVELOPMENT DATA

Note to AC characteristics

$t_{CK} = 1/f_{osc}$ = one oscillator clock period
t_{CK} = 83.3 ns at f_{osc} = 12 MHz
t_{CK} = 62.5 ns at f_{osc} = 16 MHz

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C562 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. PCB83C562 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C562" is used to refer to both family members:

- PCB83C562: 8 K bytes mask-programmable ROM
- PCB80C562: ROM-less version of the PCB83C562

The PCB83C562 contains a non-volatile 8 K x 8 read-only program memory (not ROM-less version), a volatile 256 x 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the PCB80C51), an additional 16-bit timer coupled to capture and compare latches; a fourteen source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC with pulse width modulated outputs, a UART serial interface, a 'watchdog' timer and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C562 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions; 44% one-byte, 41% two-byte and 15% three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

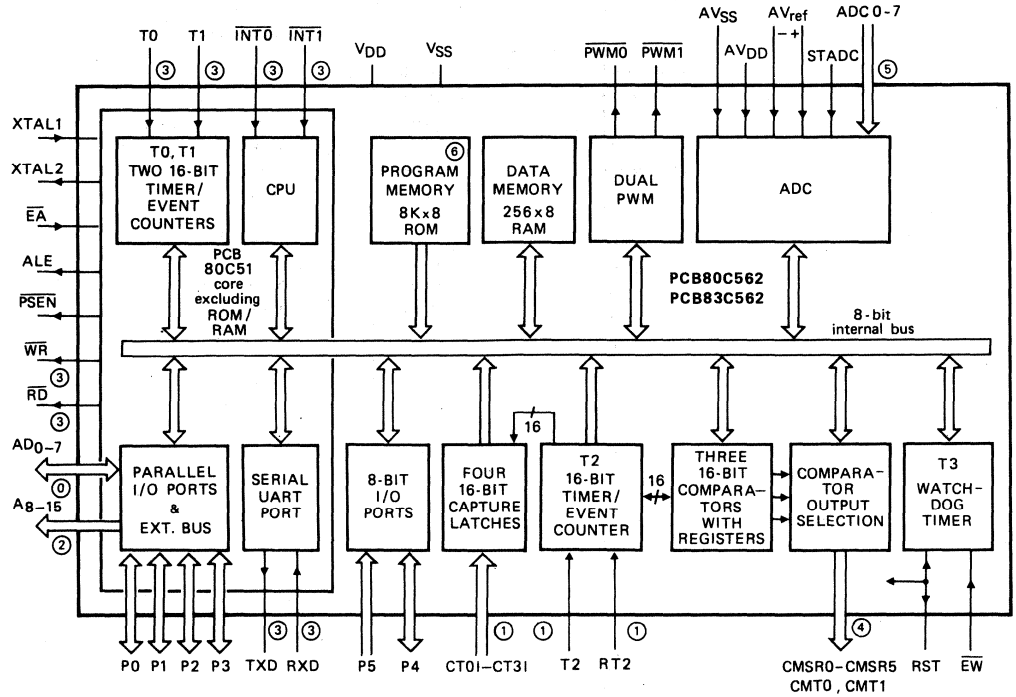
Features

- PCB80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- An ADC with 8 multiplexed analog inputs and 8-bit resolution
- Two 8-bit resolution, Pulse Width Modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- Full-duplex UART compatible with the standard PCB80C51
- On-chip watchdog timer
- Operating ambient temperature range and XTAL frequency range:

  PCB83C562: 0 to + 70 °C; 1.2 MHz – 16 MHz
  PCF83C562: –40 to + 85 °C; 1.2 MHz – 12 MHz
  PCA83C562: –40 to + 125 °C; 1.2 MHz – 12 MHz

PACKAGE OUTLINES

PCA/PCB/PCF83C562WP:
PCA/PCB/PCF80C562WP: 68-lead plastic leaded chip carrier (PLCC); (SOT188AA, AGA).
PCA/PCB/PCF83C562H:
PCA/PCB/PCF80C562H: 80-lead quad flat-pack; plastic (SOT219).



⓪ alternative function of port 0
① alternative functions of port 1
② alternative function of port 2
③ alternative function of port 3
④ alternative function of port 4
⑤ alternative function of port 5
⑥ not present in PCB80C562

7Z22645.2

Fig.1 Block diagram.

DEVELOPMENT DATA

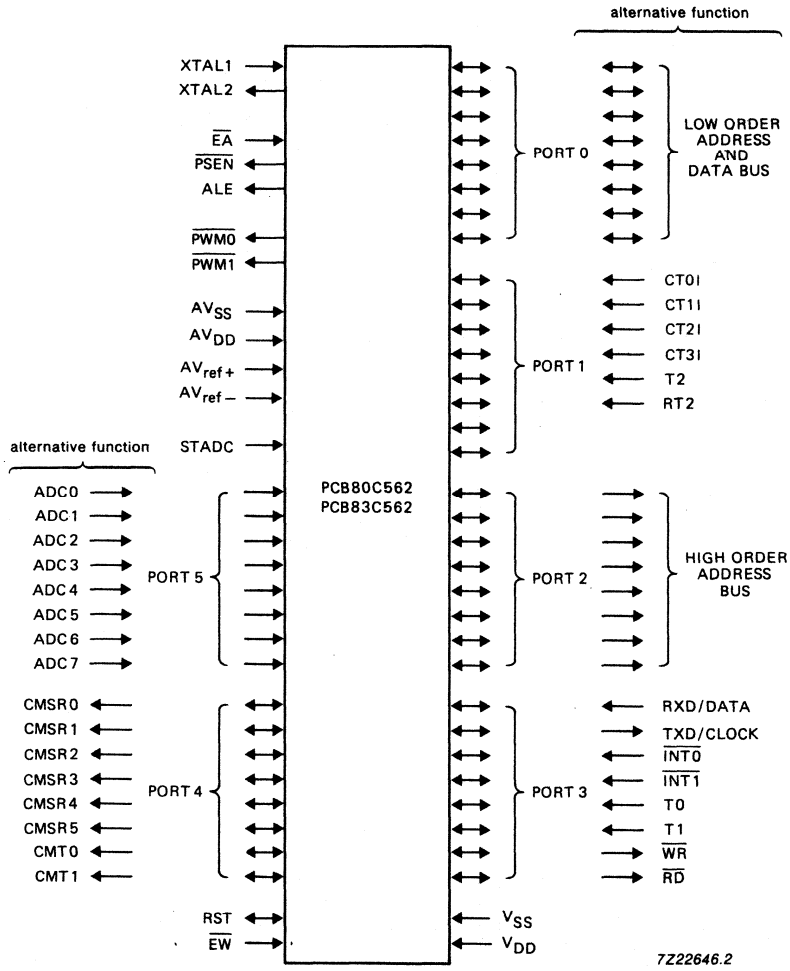


Fig. 2 Functional diagram.

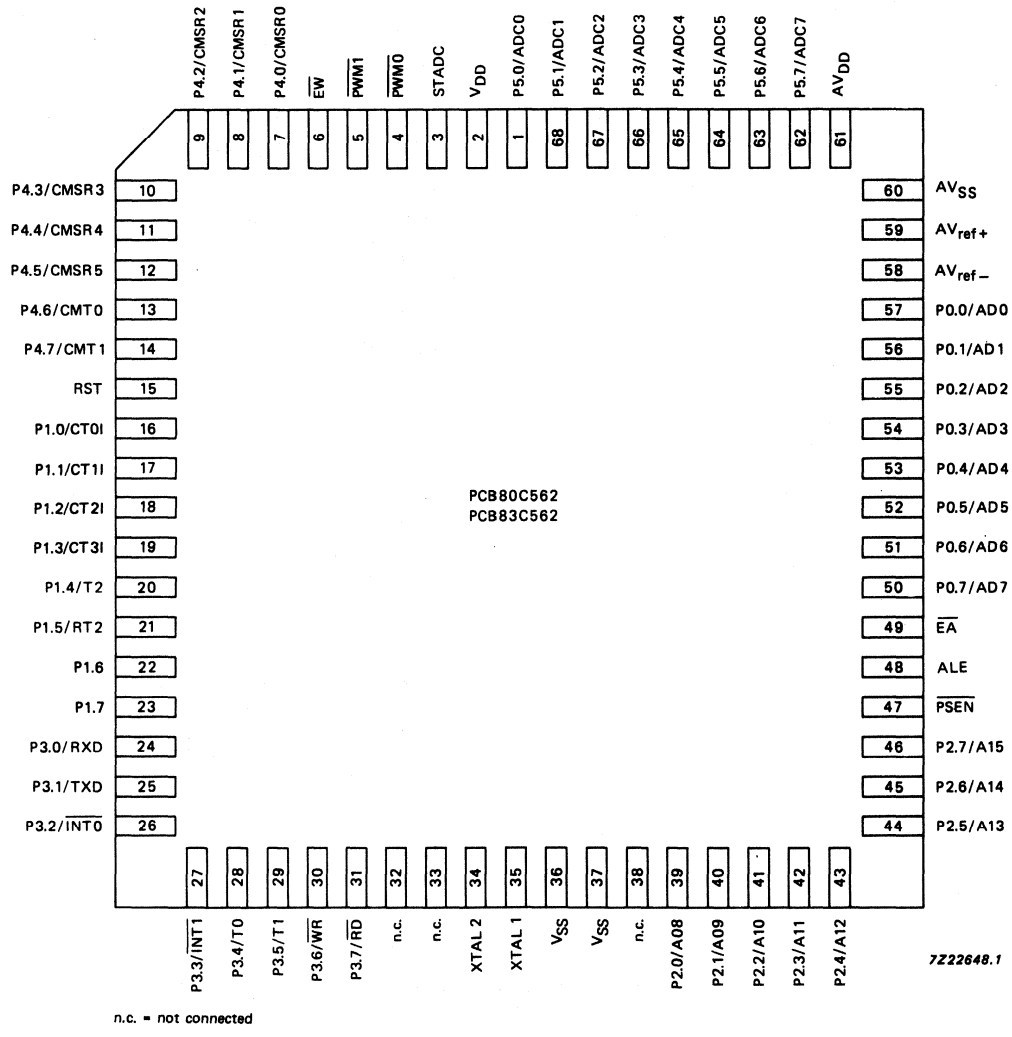
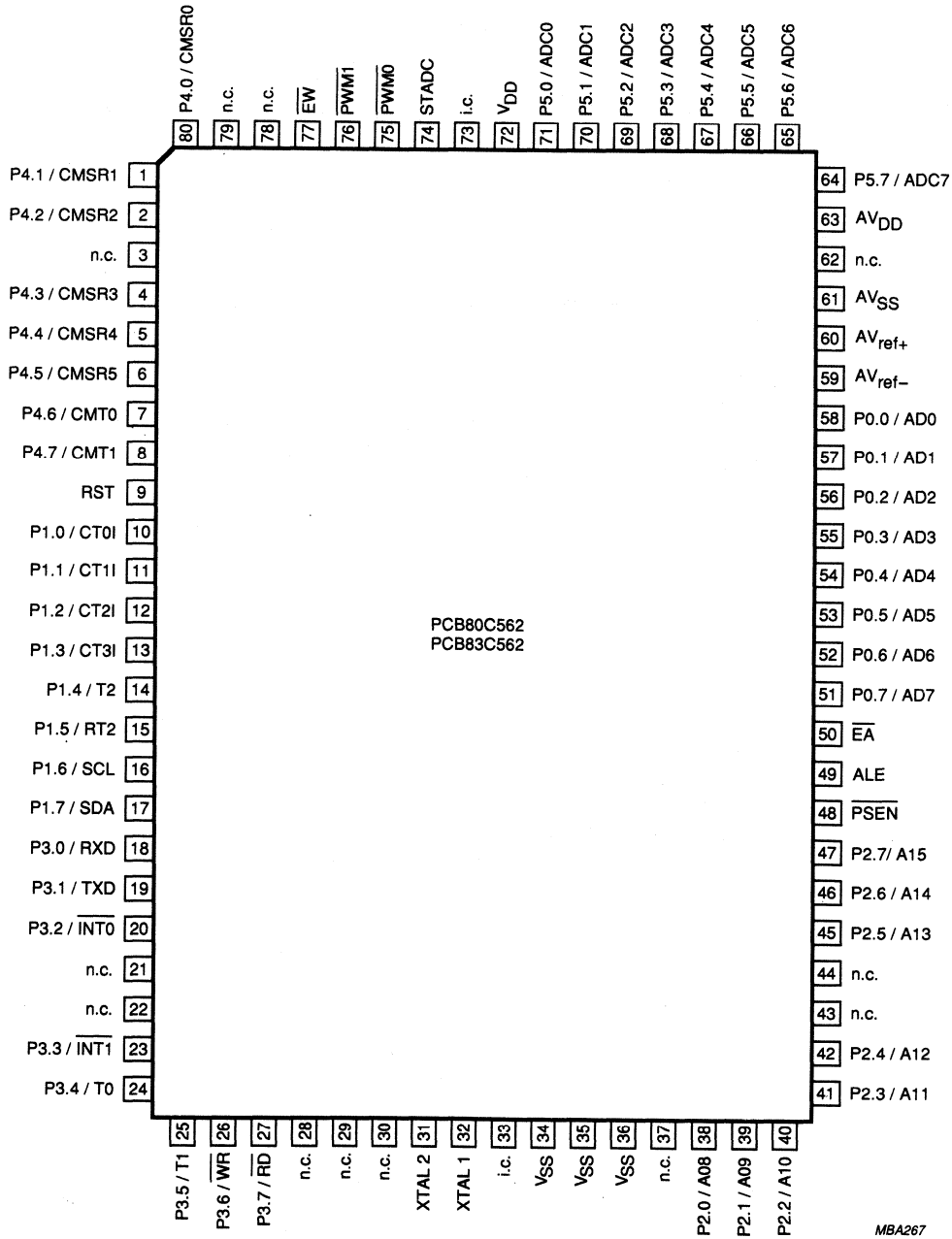


Fig. 3(a) Pinning diagram for PCB83C562WP (PLCC68).

DEVELOPMENT DATA



n.c. = not connected
i.c. = internally connected (do not use)

Fig. 3(b) Pinning diagram for PCB83C562H (QFP80).

PINNING

2	V_{DD}	**Digital power supply**: + 5 V power supply pin during normal operation, Idle mode and Power-down mode
3	STADC	**Start ADC operation**: Input starting analog to digital conversion (ADC operation can also be started by software). This pin must not float.
4	$\overline{PWM0}$	**Pulse width** modulation output 0
5	$\overline{PWM1}$	**Pulse width** modulation output 1
6	$\overline{EW}$	**Enable watchdog timer**: Enable for T3 watchdog timer and disable Power-down mode. This pin must not float.
7-14	P4.0-P4.7	**Port 4** 8-bit quasi-bidirectional I/O port

Port pin	Alternative function	
P4.0	CMSR0	Timer T2: compare and set/reset outputs on a match with timer T2
P4.1	CMSR1	
P4.2	CMSR2	
P4.3	CMSR3	
P4.4	CMSR4	
P4.5	CMSR5	
P4.6	CMT0	Timer T2: compare and toggle outputs on a match with timer T2
P4.7	CMT1	

15	RST	**Reset**: Input to reset the PCB83C562. It also provides a reset pulse as output when timer T3 overflows.
16-23	P1.0-P1.7	**Port 1** 8-bit quasi-bidirectional I/O port

Port pin	Alternative function	
P1.0	CT0I	Capture timer input signals for timer T2
P1.1	CT1I	
P1.2	CT2I	
P1.3	CT3I	
P1.4	T2	: T2 event input. Rising edge triggered
P1.5	RT2	: T2 timer reset signal. Rising edge triggered
P1.6		
P1.7		

24-31	P3.0-P3.7	**Port 3** 8-bit quasi-bidirectional I/O port

Port pin	Alternative function	
P3.0	RXD	: Serial input port
P3.1	TXD	: Serial output port
P3.2	$\overline{INT0}$	: External interrupt
P3.3	$\overline{INT1}$	: External interrupt
P3.4	T0	: Timer 0 external input
P3.5	T1	: Timer 1 external input
P3.6	$\overline{WR}$	: External data memory write strobe
P3.7	$\overline{RD}$	: External data memory read strobe

32, 33 Not connected

34	XTAL2	**Crystal input 2:** output of the inverting amplifier that forms the oscillator. Left open-circuit when an external oscillator clock is used.
35	XTAL1	**Crystal input 1:** input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator clock signal when an external oscillator is used.
36, 37	V_{SS}	**Two digital** ground pins
38		Not connected
		Port 2
39-46	P2.0-P2.7	8-bit quasi-bidirectional I/O port Port pin — Alternative function P2.0-P2.7 — High-order address byte for external memory (A08-A15)
47	$\overline{PSEN}$	**Program store enable:** active LOW read strobe to external program memory
48	ALE	**Address latch enable:** latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods. During an external data memory access one ALE pulse is skipped. ALE can drive up to 8 LSTTL inputs and handles CMOS inputs without an external pull-up.
49	$\overline{EA}$	**External access:** When $\overline{EA}$ is held at TTL level HIGH, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When $\overline{EA}$ is held at TTL LOW level, the CPU executes out of external program memory. $\overline{EA}$ is not allowed to float.
		Port 0
50-57	P0.7-P0.0	8-bit binary I/O port Port pin — Alternative function P0.0-P0.7 — Multiplexed low-order address and data bus of external memory (AD0-AD7)
58	$AV_{ref}-$	**Low end** of analog to digital conversion reference resistor
59	$AV_{ref}+$	**High end** of analog to digital conversion reference resistor
60	AV_{SS}	**Analog** ground
61	AV_{DD}	**Analog** power supply
		Port 5
62-68,1	P5.7-P5.0	8-bit input port Port pin — Alternative function P5.0-P5.7 — Eight input channels to ADC (ADC0-ADC7)

To avoid a 'latch-up' effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0,5 V or V_{SS} − 0,5 V respectively.

DEVELOPMENT DATA

DC CHARACTERISTICS

PCB83C562: V_{DD} = 5 V ± 20%; T_{amb} = 0 to + 70 °C
PCF83C562: V_{DD} = 5 V ± 20%; T_{amb} = −40 to + 85 °C
PCA83C562: V_{DD} = 5 V ± 10%; T_{amb} = −40 to + 125 °C

All voltages measured with respect to V_{SS} unless otherwise specified.

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
PCB83C562		V_{DD}	4.0	6.0	V
PCF83C562		V_{DD}	4.0	6.0	V
PCA83C562		V_{DD}	4.5	5.5	V
Supply current operating	see note 1				
PCB83C562	f_{osc} = 16 MHz	I_{DD}	–	45	mA
PCF83C562	f_{osc} = 12 MHz	I_{DD}	–	34	mA
PCA83C562	f_{osc} = 12 MHz	I_{DD}	–	30	mA
Idle mode	see note 2				
PCB83C562	f_{osc} = 16 MHz	I_{ID}	–	10	mA
PCF83C562	f_{osc} = 12 MHz	I_{ID}	–	8	mA
PCA83C562	f_{osc} = 12 MHz	I_{ID}	–	7	mA
Power-down current	2 V < V_{PD} < V_{DD} max.; see note 3				
PCB83C562		I_{PD}	–	50	μA
PCF83C562		I_{PD}	–	50	μA
PCA83C562		I_{PD}	–	100	μA
Inputs					
LOW level input voltage (except $\overline{EA}$)		V_{IL}	−0.5	$0.2V_{DD}-0.1$	V
LOW level input voltage ($\overline{EA}$)		V_{IL1}	−0.5	$0.2V_{DD}-0.3$	V
HIGH level input voltage (except RST, XTAL 1)		V_{IH}	$0.2V_{DD}+0.9$	$V_{DD}+0.5$	V
HIGH level input voltage (RST and XTAL 1)		V_{IH1}	$0.7V_{DD}$	$V_{DD}+0.5$	V
Input current logic 0 (Ports 1, 2, 3 and 4)	V_I = 0,45 V	$-I_{IL}$	–	50	μA
Input current logic 1 to 0 transition (Ports 1, 2, 3 and 4)	V_I = 2,0 V	$-I_{TL}$	–	650	μA
Input leakage current (Port 0, Port 5, $\overline{EA}$, STADC, $\overline{EW}$)	0,45 V < V_I < V_{DD}	$\pm I_{LI1}$	–	10	μA

parameter	conditions	symbol	min.	max.	unit
Outputs					
LOW level output voltage (Ports 1, 2, 3 and 4)	see note 4 I_{OL} = 1.6 mA	V_{OL}	–	0.45	V
LOW level output voltage (Port 0, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$)	see note 4 I_{OL} = 3.2 mA	V_{OL1}	–	0.45	V
HIGH level output voltage (Ports 1, 2, 3 and 4)	V_{DD} = 5 V ± 10% $-I_{OH}$ = 60 μA $-I_{OH}$ = 25 μA $-I_{OH}$ = 10 μA	 V_{OH} V_{OH} V_{OH}	 2.4 $0.75V_{DD}$ $0.9V_{DD}$	 – – –	 V V V
HIGH level output voltage (Port 0 in external bus) mode, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$)	see note 5 V_{DD} = 5 V ± 10% $-I_{OH}$ = 400 μA $-I_{OH}$ = 150 μA $-I_{OH}$ = 40 μA	 V_{OH1} V_{OH1} V_{OH1}	 2.4 $0.75V_{DD}$ $0.9V_{DD}$	 – – –	 V V V
HIGH level output voltage (RST)	$-I_{OH}$ = 400 μA $-I_{OH}$ = 120 μA	V_{OH2} V_{OH2}	2.4 $0.8V_{DD}$	– –	V V
RST pull-down resistor		R_{RST}	50	150	kΩ
Capacitance of I/O buffer	Test freq. = 1 MHz T_{amb} = 25 °C	$C_{I/O}$	–	10	pF

DEVELOPMENT DATA

CHARACTERISTICS OF THE ADC

PCB83C562: AV_{DD} = 5 V ± 20%; T_{amb} = 0 to + 70 °C
PCF83C562: AV_{DD} = 5 V ± 20%; T_{amb} = −40 to + 85 °C
PCA83C562: AV_{DD} = 5 V ± 10%; T_{amb} = −40 to + 125 °C

All voltages measured with respect to AV_{SS} unless otherwise specified.

parameter	conditions	symbol	min.	max.	unit
Supply					
Analog supply voltage					
PCB83C562	$AV_{DD} = V_{DD} \pm 0.2$ V	AV_{DD}	4.0	6.0	V
PCF83C562	$AV_{DD} = V_{DD} \pm 0.2$ V	AV_{DD}	4.0	6.0	V
PCA83C562	$AV_{DD} = V_{DD} \pm 0.2$ V	AV_{DD}	4.5	5.5	V
Analog supply current					
operating	Port 5 = 0 to AV_{DD}	AI_{DD}	–	1.2	mA
idle mode					
PCB83C562		AI_{ID}	–	50	μA
PCF83C562		AI_{ID}	–	50	μA
PCA83C562		AI_{ID}	–	100	μA
power-down	2 V < AV_{PD} < AV_{DD} max				
PCB83C562		AI_{PD}	–	50	μA
PCF83C562		AI_{PD}	–	50	μA
PCA83C562		AI_{PD}	–	100	μA
Analog inputs					
Analog input voltage		AV_{IN}	AV_{SS}−0.2	AV_{DD}+0.2	V
Reference voltage		AV_{ref-}	AV_{SS}−0.2	–	V
		AV_{ref+}	–	AV_{DD}+0.2	V
Resistance between AV_{ref+} and AV_{ref-}		R_{ref}	5	25	kΩ
Analog input capacitance		C_{IA}	–	15	pF
Sampling time		t_{ADS}	–	$6t_{CY}$	μs
Conversion time (including sample time)		t_{ADC}	–	$24t_{CY}$	μs
Differential non-linearity	see notes 6, 7 and 11	DL_e	–	± 1	LSB
Integral non-linearity	see notes 6 and 8	IL_e	–	± 1	LSB
Offset error	see notes 6 and 10	OS_e	–	± 1	LSB
Gain error	see notes 6 and 9	G_e	–	± 0.4	%
Channel to channel matching		M_{ctc}	–	± 1	LSB
Crosstalk between inputs of Port 5	0 to 100 kHz	C_t	–	−60	dB

Notes to the characteristics

1. The operating supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f = 10$ ns; $V_{IL} = V_{SS} + 0.5$ V; $V_{IH} = V_{DD} - 0.5$ V; XTAL 2 not connected; $\overline{EA}$ = RST = Port 0 = $\overline{EW}$ = V_{DD}; STADC = V_{SS}.
2. The Idle mode supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f = 10$ ns; $V_{IL} = V_{SS} + 0.5$ V; $V_{IH} = V_{DD} - 0.5$ V; XTAL 2 not connected; $\overline{EA}$ = Port 0 = $\overline{EW}$ = V_{DD}; RST = STADC = V_{SS}.
3. The power-down current is measured with all output pins disconnected; XTAL 2 not connected; $\overline{EA}$ = Port 0 = $\overline{EW}$ = V_{DD}; RST = STADC = XTAL 1 = V_{SS}.
4. Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1, Port 3 and Port 4. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make a 1-to-0 transition during bus operations. In the most adverse condition (capacitive loading > 100 pF) the noise pulse on ALE line may exceed 0.8 V. In this event it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.
5. Capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{DD} specification when the address bits are stabilizing.
6. $AV_{ref+} = 5.12$ V; $AV_{ref-} = 0$ V; $AV_{DD} = 5.0$ V.
7. The differential non-linearity (DL_e) is the difference between the actual step width and the ideal step width.
8. The integral non-linearity (IL_e) is the peak difference between the centre of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error.
9. The gain error (G_e) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve.
10. The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and a straight line which fits the ideal transfer curve. For an uncalibrated ADC, the offset error is constant at every point of the actual transfer curve.
11. The ADC is monotonic; there are no missing codes.

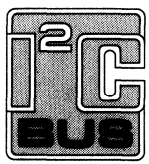
DEVELOPMENT DATA

AC CHARACTERISTICS

PCB83C562: V_{DD} = 5 V ± 20%; T_{amb} = 0 to + 70 °C; f_{osc} = 1.2 to 16 MHz
PCF83C562: V_{DD} = 5 V ± 20%; T_{amb} = −40 to + 85 °C; f_{osc} = 1.2 to 12 MHz
PCA83C562: V_{DD} = 5 V ± 10%; T_{amb} = −40 to + 125 °C; f_{osc} = 1.2 to 12 MHz

C_L = 100 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 80 pF for all other outputs unless otherwise specified. (see waveforms Figs 21, 22 and 23).

parameter	symbol	f_{osc} = 16 MHz		f_{osc} = 12 MHz		f_{osc} = variable		unit
		min.	max.	min.	max.	min.	max.	
Program memory								
ALE pulse duration	t_{LL}	85	–	127	–	$2t_{CK}-40$	–	ns
Address set-up time to ALE	t_{AL}	8	–	28	–	$t_{CK}-55$	–	ns
Address hold time after ALE	t_{LA}	28	–	48	–	$t_{CK}-35$	–	ns
Time from ALE to valid instruction input	t_{LIV}	–	150	–	233	–	$4t_{CK}-100$	ns
Time from ALE to control pulse $\overline{PSEN}$	t_{LC}	23	–	43	–	$t_{CK}-40$	–	ns
Control pulse duration $\overline{PSEN}$	t_{CC}	143	–	205	–	$3t_{CK}-45$	–	ns
Time from $\overline{PSEN}$ to valid instruction input	t_{CIV}	–	83	–	145	–	$3t_{CK}-105$	ns
Input instruction hold time after $\overline{PSEN}$	t_{CI}	0	–	0	–	0	–	ns
Input instruction float delay after $\overline{PSEN}$	t_{CIF}	–	38	–	59	–	$t_{CK}-25$	ns
Address to valid instruction input	t_{AIV}	–	208	–	312	–	$5t_{CK}-105$	ns
Address float delay after $\overline{PSEN}$	t_{AFC}	–	10	–	10	–	10	ns



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

parameter	symbol	f_{osc} = 16 MHz		f_{osc} = 12 MHz		f_{osc} = variable		unit
		min.	max.	min.	max.	min.	max.	
External data memory								
$\overline{RD}$ pulse duration	t_{RR}	275	–	400	–	$6t_{CK}-100$	–	ns
$\overline{WR}$ pulse duration	t_{WW}	275	–	400	–	$6t_{CK}-100$	–	ns
Address set up time to ALE	t_{AL}	8	–	28	–	$t_{CK}-55$	–	ns
Address hold time after ALE	t_{LA}	28	–	48	–	$t_{CK}-35$	–	ns
$\overline{RD}$ to valid data input	t_{RD}	–	148	–	252	–	$5t_{CK}-165$	ns
Data hold time after $\overline{RD}$	t_{DR}	0	–	0	–	0	–	ns
Data float delay after $\overline{RD}$	t_{DFR}	–	55	–	97	–	$2t_{CK}-70$	ns
Time from ALE to valid data input	t_{LD}	–	350	–	517	–	$8t_{CK}-150$	ns
Address to valid data input	t_{AD}	–	398	–	585	–	$9t_{CK}-165$	ns
Time from ALE to $\overline{RD}$ or $\overline{WR}$	t_{LW}	138	238	200	300	$3t_{CK}-50$	$3t_{CK}+50$	ns
Time from address to $\overline{RD}$ or $\overline{WR}$	t_{AW}	120	–	203	–	$4t_{CK}-130$	–	ns
Time from $\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	t_{WHLH}	23	103	43	123	$t_{CK}-40$	$t_{CK}+40$	ns
Data valid to $\overline{WR}$ transition	t_{DWX}	3	–	23	–	$t_{CK}-60$	–	ns
Data set-up time before $\overline{WR}$	t_{DW}	288	–	433	–	$7t_{CK}-150$	–	ns
Data hold time after $\overline{WR}$	t_{WD}	13	–	33	–	$t_{CK}-50$	–	ns
Address float delay after $\overline{RD}$	t_{AFR}	–	0	–	0	–	0	ns

DEVELOPMENT DATA

Note:

$t_{CK} = 1/f_{osc}$ = one oscillator clock period at XTAL 1
$t_{CK} = 83$ ns @$f_{osc} = 12$ MHz
$t_{CK} = 63$ ns @$f_{osc} = 16$ MHz

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C652 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C652 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C652" is used to refer to both family members:

- PCB83C652: 8 K bytes mask-programmable ROM, 256 bytes RAM
- PCB80C652: ROM-less version of the PCB83C652

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems.

The PCB83C652 contains a non-volatile 8 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

Features

- 80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART facilities
  Three temperature ranges available
  0 to + 70 °C; PCB83C652 versions
  –40 to + 85 °C; PCF83C652 versions
  –40 to + 125 °C; PCA83C652 versions
- Extended frequency range: 1.2 MHz to 12 MHz

PACKAGE OUTLINES

PCA/PCB/PCF83C652P; PCA/PCB/PCF80C652P: 40-lead DIL; plastic (SOT129).
PCA/PCB/PCF83C652WP; PCA/PCB/PCF80C652WP: 44-lead plastic leaded-chip-carrier (PLCC) (SOT187AA, AGA) and (SOT188AA, AGA) these are interchangeable.
PCA/PCB/PCF83C652H; PCA/PCB/PCF80C652H: 44-lead quad flat-pack (QFP). This is in preparation.

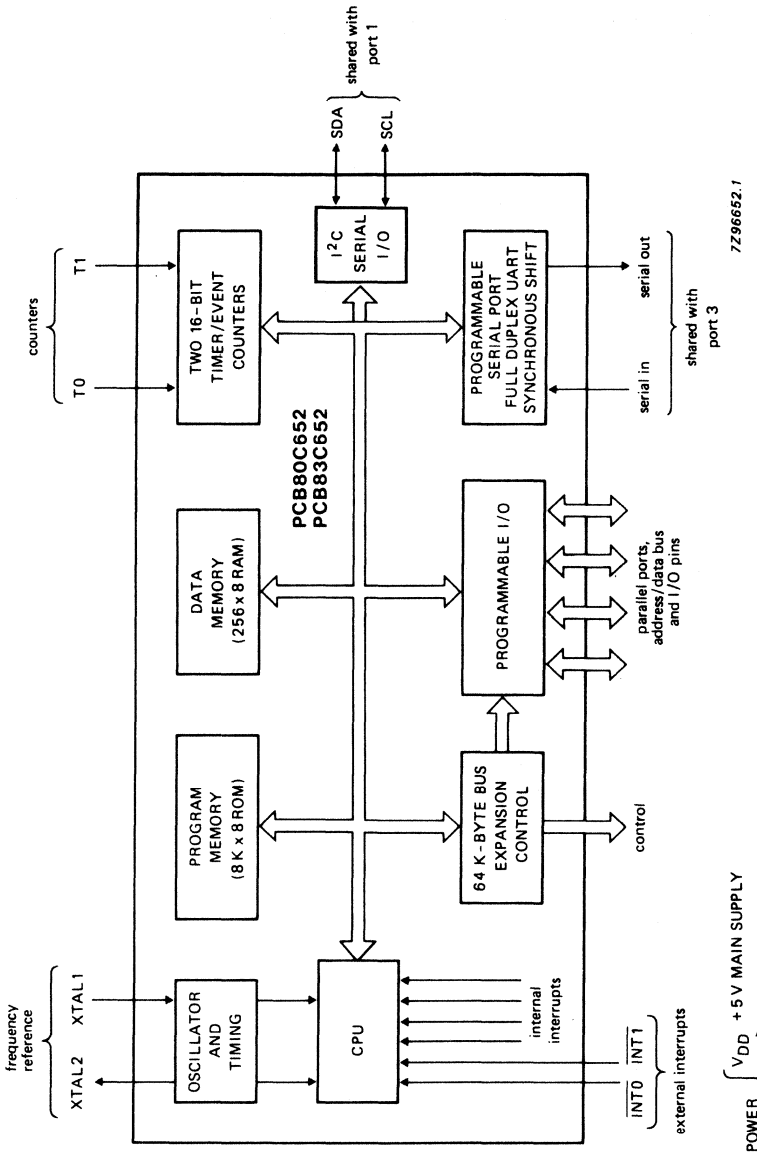


Fig. 1 Block diagram.

DEVELOPMENT DATA

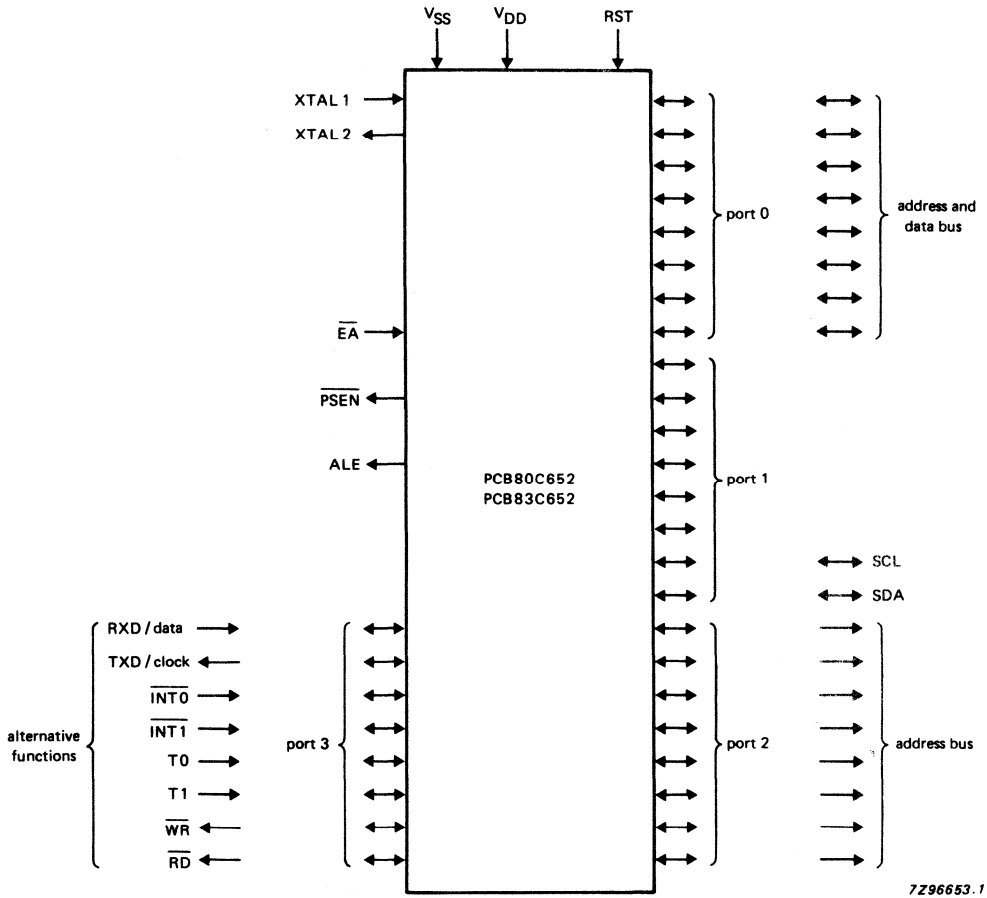


Fig. 2 Functional diagram.

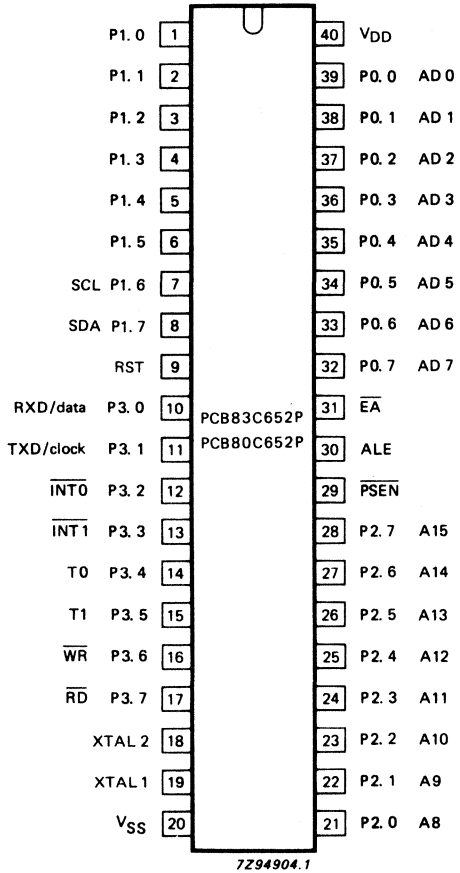


Fig. 3a Pinning diagram for 40-lead DIL package (SOT129).

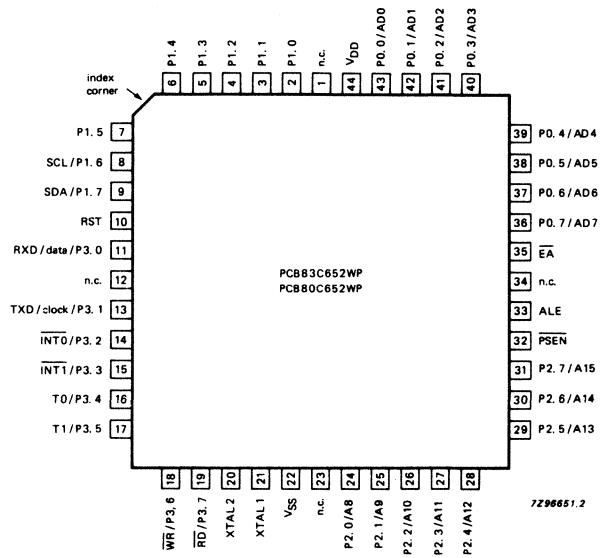


Fig. 3b Pinning diagram for 44-lead PLCC package (SOT187).

PINNING (PCB83C652P, PCB80C652P)

1-8	P1.0-P1.7	**Port 1:** 8-bit quasi-bidirectional I/O port. Port 1 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups, except P1.6 and P1.7 which have open drain outputs. Port pin — Alternative function P1.6 — SCL: I^2C-bus serial port clock line P1.7 — SDA: I^2C-bus serial port data line
9	RST	**RESET:** a high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V_{DD}.

10-17	P3.0-P3.7	**Port 3:** 8-bit quasi-bidirectional I/O port with internal pull-ups. It also serves the following alternative functions:

Port pin	Alternative function
P3.0	RXD/data: serial port receiver data input (asynchronous) or data input/output (synchronous)
P3.1	TXD/clock: serial port transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{INT0}$: external interrupt 0 or gate control input for timer/event counter 0
P3.3	$\overline{INT1}$: external interrupt 1 or gate control input for timer/event counter 1
P3.4	T0: external input for timer/event counter 0
P3.5	T1: external input for timer/event counter 1
P3.6	$\overline{WR}$: external data memory write strobe
P3.7	$\overline{RD}$: external data memory read strobe

The generation or use of a Port 3 pin as an alternative function is carried out automatically by the PCB83C652 provided the associated Special Function Register bit is set high. Port 3 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups.

18	XTAL 2	**Crystal input 2:** output of the inverting amplifier that forms the oscillator. Left open-circuit when an external oscillator clock is used (see Figs 10 and 11).
19	XTAL 1	**Crystal input 1:** input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator clock signal when an external oscillator is used (see Figs 10 and 11).
20	V_{SS}	**Ground:** circuit ground potential.
21-28	P2.0-P2.7	**Port 2:** 8-bit quasi-bidirectional I/O port with internal pull-ups. During access to external memories (RAM/ROM) that use 16-bit addresses (MOVX @DPTR) Port 2 emits the high order address byte. When external RAM is accessed with an 8-bit address (MOVX @Ri) Port 2 emits the contents of the P2 special function register. Port 2 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups.
29	$\overline{PSEN}$	**Program Store Enable output:** read strobe to the external program memory via Port 0 and 2. It is activated twice each machine cycle during fetches from external program memory. When executing out of external program memory two activations of $\overline{PSEN}$ are skipped during each access to external data memory. $\overline{PSEN}$ is not activated (remains HIGH) during no fetches from external program memory. $\overline{PSEN}$ can sink/source 8 LSTTL inputs. It can drive CMOS inputs without an external pull-up.
30	ALE	**Address Latch Enable output:** latches the low byte of the address during accesses to external memory in normal operation. It is activated every six oscillator periods except during an external data memory access. ALE can sink/source 8 LSTTL inputs. It can drive CMOS inputs without an external pull-up.

DEVELOPMENT DATA

PINNING (continued)

31	$\overline{EA}$	**External Access input:** When $\overline{EA}$ is held at a TTL high level the CPU executes out of the internal program ROM provided the program counter is less than 8192. When $\overline{EA}$ is held at a TTL low level, the CPU executes out of external program memory via Port 0 and Port 2. $\overline{EA}$ is not allowed to float.
32-39	P0.7-P0.0	**Port 0:** 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus during accesses to external memory (during these accesses it activates internal pull-ups). Port 0 can sink/source eight LSTTL inputs.
40	V_{DD}	**Power supply:** + 5 V power supply pin during normal operation, Idle mode and Power-down mode.

To avoid a 'latch-up' effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0,5 V or V_{SS} – 0,5 V respectively.

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 5 V (± 10%); V_{SS} = 0 V; T_{amb} = 0 to 70 °C (PCB83C652); −40 to 85 °C (PCF83C652); −40 to 125 °C (PCA83C652). All voltages with respect to V_{SS} unless otherwise specified.

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	4.5	5.5	V
Supply current					
operating	(notes 1 and 2)	I_{DD}	–	24	mA
	(notes 1 and 3)	I_{DD}	–	27	mA
idle mode	(notes 2 and 4)	I_{ID}	–	5.0	mA
	(notes 3 and 4)	I_{ID}	–	6.0	mA
Power-down current	(notes 2, 5 and 6)	I_{PD}	–	50	μA
	(notes 3, 5 and 6)	I_{PD}	–	120	μA
Inputs					
LOW level input voltage (except $\overline{EA}$, P1.6/SCL, P1.7/SDA)		V_{IL}	−0.5	$0.2V_{DD}-0.1$	V
LOW level input voltage ($\overline{EA}$)		V_{IL1}	−0.5	$0.2V_{DD}-0.3$	V
LOW level input voltage (P1.6/SCL, P1.7/SDA)*		V_{IL2}	−0.5	1.5	V
HIGH level input voltage (except RST, XTAL 1, P1.6/SCL, P1.7/SDA)		V_{IH}	$0.2V_{DD}+0.9$	$V_{DD}+0.5$	V
HIGH level input voltage (RST and XTAL 1)		V_{IH1}	$0.7V_{DD}$	$V_{DD}+0.5$	V
HIGH level input voltage (P1.6/SCL, P1.7/SDA)*		V_{IH2}	3.0	6	V
Input current logic 0 (Ports 1, 2 and 3 except P1.6/SCL, P1.7/SDA)	V_I = 0.45 V	$-I_{IL}$	–	50	μA
Input current logic 1 to 0 transition (Ports 1, 2, 3 except P1.6/SCL, P1.7/SDA)	V_I = 2.0 V	$-I_{TL}$	–	650	μA
Input leakage current (Port 0, $\overline{EA}$)	$0.45\ V < V_I < V_{DD}$	$\pm I_{LI1}$	–	10	μA
Input leakage current (P1.6/SCL, P1.7/SDA)	$0\ V < V_I < 6\ V$; $0\ V < V_{DD} < 5.5\ V$	$\pm I_{LI2}$	–	10	μA

* The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I^2C specification, so an input voltage below 1.5 V will be recognized as a logic 0 while an input voltage above 3.0 V will be recognized as a logic 1.

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	max.	unit
Outputs					
LOW level output voltage (Ports 1, 2, 3 except P1.6/SCL, P1.7/SDA)*	I_{OL} = 1.6 mA	V_{OL}	–	0.45	V
LOW level output voltage (Port 0, ALE, $\overline{PSEN}$)*	I_{OL} = 3.2 mA	V_{OL1}	–	0.45	V
LOW level output voltage (P1.6/SCL, P1.7/SDA)	I_{OL} = 3.0 mA	V_{OL2}	–	0.40	V
HIGH level output voltage (Ports 1, 2, 3)	$-I_{OH}$ = 60 μA	V_{OH}	2.4	–	V
	$-I_{OH}$ = 25 μA	V_{OH}	$0.75V_{DD}$	–	V
	$-I_{OH}$ = 10 μA	V_{OH}	$0.9V_{DD}$	–	V
HIGH level output voltage (Port 0 in external bus mode, ALE, $\overline{PSEN}$)**	$-I_{OH}$ = 400 μA	V_{OH1}	2.4	–	V
	$-I_{OH}$ = 150 μA	V_{OH1}	$0.75V_{DD}$	–	V
	$-I_{OH}$ = 40 μA	V_{OH1}	$0.9V_{DD}$	–	V
RST pull-down resistor		R_{RST}	50	150	kΩ
I/O pin capacitance	test freq. = 1 MHz; T_{amb} = 25 °C	$C_{I/O}$	–	10	pF

Notes to the DC characteristics

1. The operating supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ −0.5 V; XTAL 2 not connected; $\overline{EA}$ = RST = Port 0 = P1.6 = P1.7 = V_{DD}; f_{CLK} = 12 MHz.
2. This is a preliminary value and applies to PCB83C652 (0 to 70 °C) and PCF83C652 (−40 to 85 °C).
3. This is a preliminary value and applies to PCA83C652 (−40 to 125 °C).
4. The idle mode supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ −0.5 V; XTAL 2 not connected; $\overline{EA}$ = Port 0 = P1.6 = P1.7 = V_{DD}; RST = V_{SS}; f_{CLK} = 12 MHz.
5. The power-down current is measured with all output pins disconnected; XTAL 2 not connected; $\overline{EA}$ = Port 0 = P1.6 = P1.7 = V_{DD}; RST = V_{SS}.
6. 2 V $\leqslant V_{PD} \leqslant V_{DD}$ max..

* Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make a 1-to-0 transition during Bus operations. In the most adverse condition (capacitive loading > 100 pF) the noise pulse on ALE line may exceed 0.8 V. In this event it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.

** Capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{DD} specification when the address bits are stabilizing

DEVELOPMENT DATA

AC CHARACTERISTICS

V_{DD} = 5 V (± 10%); V_{SS} = 0 V; T_{amb} = 0 to 70 °C (PCB83C652); −40 to 85 °C (PCF83C652); −40 to 125 °C (PCA83C652). C_L = 100 pF (Port 0, ALE and $\overline{PSEN}$); C_L = 80 pF (all other outputs); unless otherwise specified (see waveforms Figs 16, 17 and 18).

parameter	symbol	10 MHz		12 MHz		variable clock		unit
		min.	max.	min.	max.	min.	max.	
Program memory								
ALE pulse duration	t_{LL}	160	–	127	–	$2t_{CK}-40$	–	ns
Address set-up time to ALE	t_{AL}	45	–	28	–	$t_{CK}-55$	–	ns
Address hold time after ALE	t_{LA}	65	–	48	–	$t_{CK}-35$	–	ns
Time from ALE to valid instruction input	t_{LIV}	–	300	–	233	–	$4t_{CK}-100$	ns
Time from ALE to control pulse $\overline{PSEN}$	t_{LC}	60	–	43	–	$t_{CK}-40$	–	ns
Control pulse duration $\overline{PSEN}$	t_{CC}	255	–	205	–	$3t_{CK}-45$	–	ns
Time from $\overline{PSEN}$ to valid instruction input	t_{CIV}	–	195	–	145	–	$3t_{CK}-105$	ns
Input instruction hold time after $\overline{PSEN}$	t_{CI}	0	–	0	–	0	–	ns
Input instruction float delay after $\overline{PSEN}$	t_{CIF}	–	75	–	59	–	$t_{CK}-25$	ns
Address to valid instruction input	t_{AIV}	–	395	–	312	–	$5t_{CK}-105$	ns
Address float delay after $\overline{PSEN}$	t_{AFC}	–	10	–	10	–	10	ns

AC CHARACTERISTICS (continued)

parameter	symbol	10 MHz		12 MHz		variable clock		unit
		min.	max.	min.	max.	min.	max.	
External data memory								
$\overline{RD}$ pulse duration	t_{RR}	500	–	400	–	$6t_{CK}-100$	–	ns
$\overline{WR}$ pulse duration	t_{WW}	500	–	400	–	$6t_{CK}-100$	–	ns
Address set-up time to ALE	t_{AL}	45	–	28	–	$t_{CK}-55$	–	ns
Address hold time after ALE	t_{LA}	65	–	48	–	$t_{CK}-35$	–	ns
$\overline{RD}$ to valid data input	t_{RD}	–	335	–	252	–	$5t_{CK}-165$	ns
Data hold time after $\overline{RD}$	t_{DR}	0	–	0	–	0	–	ns
Data float delay after $\overline{RD}$	t_{DFR}	–	130	–	97	–	$2t_{CK}-70$	ns
Time from ALE to valid data input	t_{LD}	–	650	–	517	–	$8t_{CK}-150$	ns
Address to valid data input	t_{AD}	–	735	–	585	–	$9t_{CK}-165$	ns
Time from ALE to $\overline{RD}$ or $\overline{WR}$	t_{LW}	250	350	200	300	$3t_{CK}-50$	$3t_{CK}+50$	ns
Time from address to $\overline{RD}$ or $\overline{WR}$	t_{AW}	270	–	203	–	$4t_{CK}-130$	–	ns
Time from $\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	t_{WHLH}	60	140	43	123	$t_{CK}-40$	$t_{CK}+40$	ns
Data valid to $\overline{WR}$ transition	t_{DWX}	40	–	23	–	$t_{CK}-60$	–	ns
Data set-up time before $\overline{WR}$	t_{DW}	550	–	433	–	$7t_{CK}-150$	–	ns
Data hold time after $\overline{WR}$	t_{WD}	50	–	33	–	$t_{CK}-50$	–	ns
Address float delay after $\overline{RD}$	t_{AFR}	–	0	–	0	–	0	ns

Where:

$1/t_{CK}$ = 1,2 to 12 MHz (see Fig. 15 and Table 6)

t_{CY} = 12 t_{CK} (see Fig. 16 and DC characteristics)

AC CHARACTERISTICS (continued)

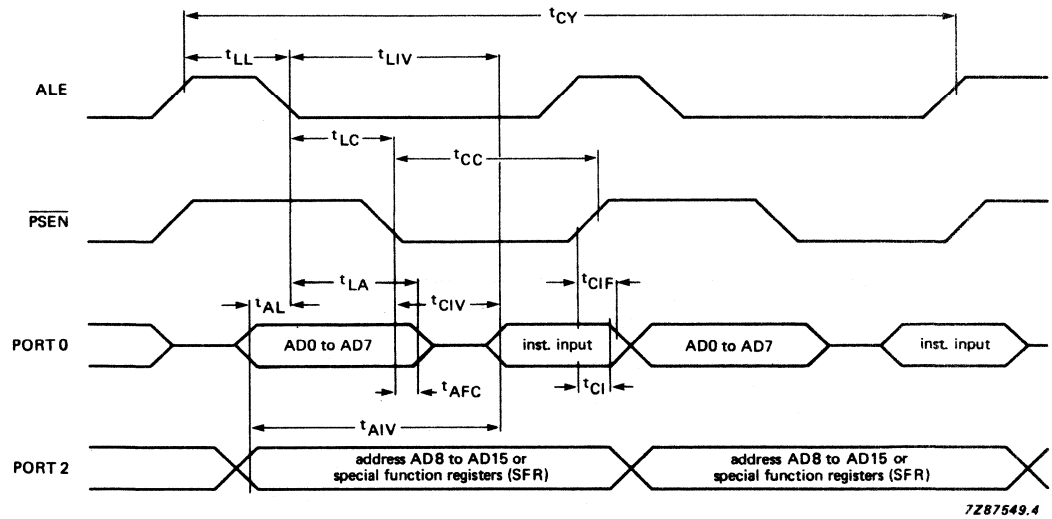


Fig. 16 Read from program memory.

DEVELOPMENT DATA

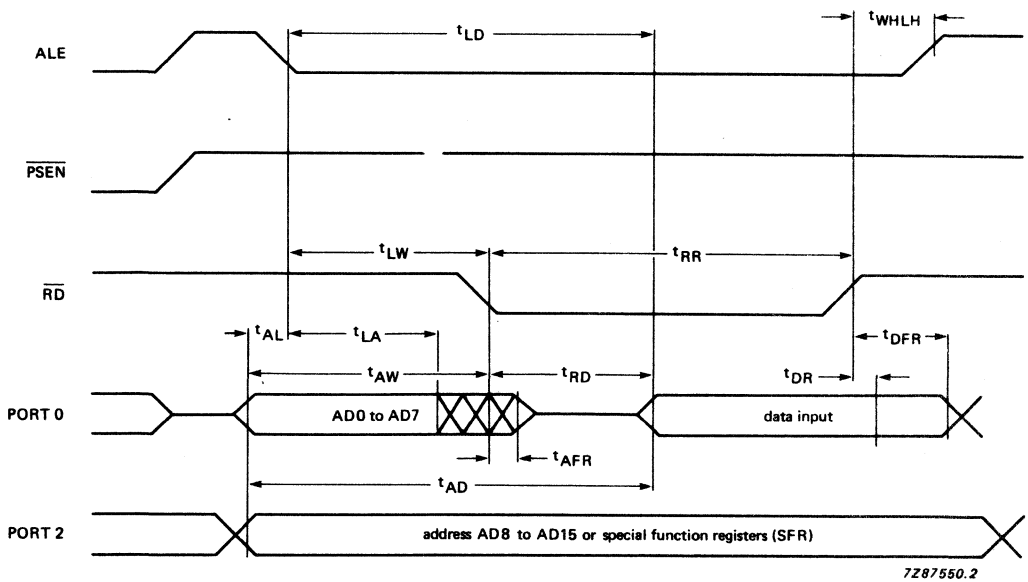


Fig. 17 Read from data memory.

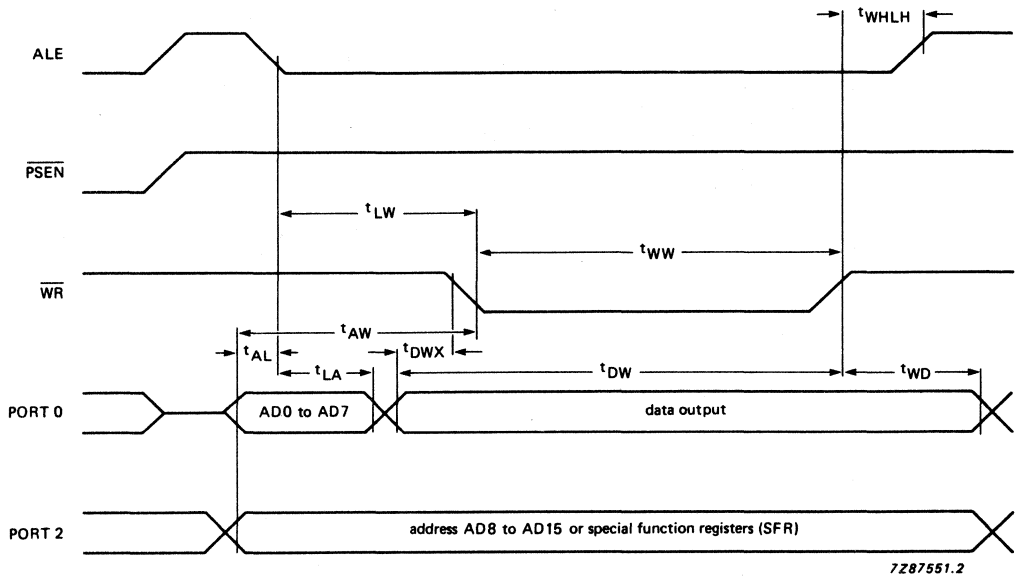


Fig. 18 Write to data memory.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C851 single chip microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C851 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term 'PCB83C851' is used to refer to both family members:

- PCB83C851: 4 K bytes mask-programmable ROM, 128 bytes RAM, 256 bytes EEPROM
- PCB80C851: ROM-less version of the PCB83C851

This device provides architectural enhancements that make it suitable for a variety of applications, specifically control systems.

The PCB83C851 contains a non-volatile 4 K x 8 read-only program memory; a volatile 128 x 8 read/write data memory; a 256 byte electrically erasable programmable read only memory (EEPROM); 32 I/O lines; two 16-bit timer/event counters (identical to the timers of the PCB80C51); a seven source, five-vector, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART; and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C851 can be expanded using standard TTL compatible memories and logic.

The PCB83C851 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The Idle mode freezes the CPU while allowing the RAM, timers, serial port and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte and 16 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 µs and 40% in 2 µs. Multiply and divide instructions require 4 µs.

FEATURES

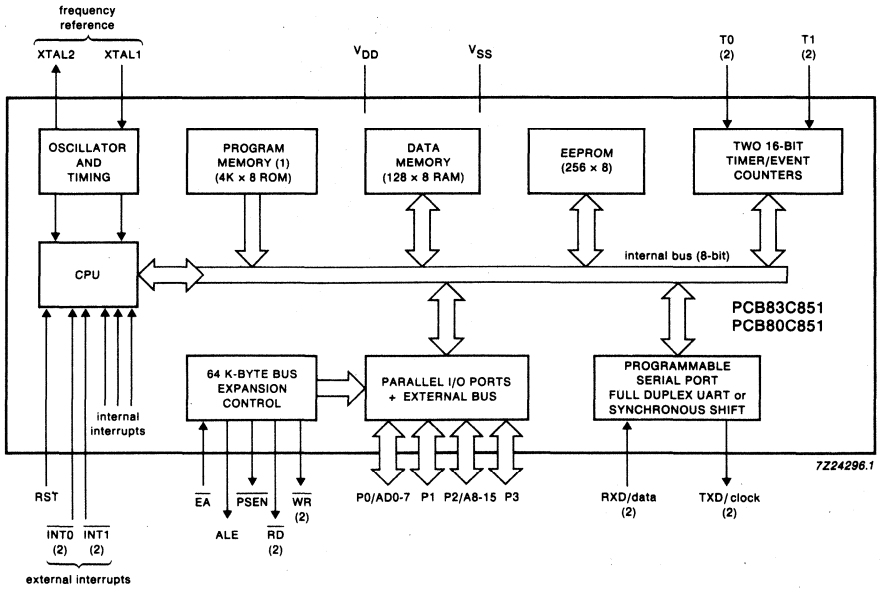
- PCB80C51 central processing unit
- 4 K x 8 ROM, expandable externally to 64 K bytes
- 128 x 8 RAM, expandable externally to 64 K bytes
- Four 8-bit I/O ports, 32 I/O lines
- Two 16-bit timer/event counters
- Full-duplex serial port
- Boolean processing
- On-chip oscillator
- Seven-source, five-vector interrupt structure with two priority levels
- 58% of the instructions are executed in 1 µs; multiply and divide in 4 µs; all others are executed in 2 µs (with a 12 MHz oscillator)
- Enhanced architecture with non-page-oriented-instructions, direct addressing, four 8-byte register banks, stack depth up to 128-bytes, multiply, divide, subtract and compare instructions
- ROM code protection (mask-programmable)
- Security mode, user dependent protection of the EEPROM contents
- Additional interrupt source (EEPROM) 'ORed' with serial interrupt

EEPROM

- Non-volatile 256 x 8 bit EEPROM (electrically erasable programmable read only memory)
- On-chip voltage multiplier for erase/write
- 10,000 erase/write cycles per byte
- 10 years non volatile data retention
- Infinite number of read cycles

PACKAGE OUTLINES

PCB/PCF83C851/80C851P: 40-lead dual in-line; plastic (SOT129)
PCB/PCF83C851/80C851WP: 44-lead plastic leaded chip carrier (PLCC); (SOT187AA, AGA).
PCB/PCF83C851/80C851H: 44-lead quad flat-pack; plastic (SOT205A)



(1) Not present in PCB/PCF80C851.
(2) Shared with a Port 3 line.

Fig.1 Block diagram (PCB/PCF83C851).

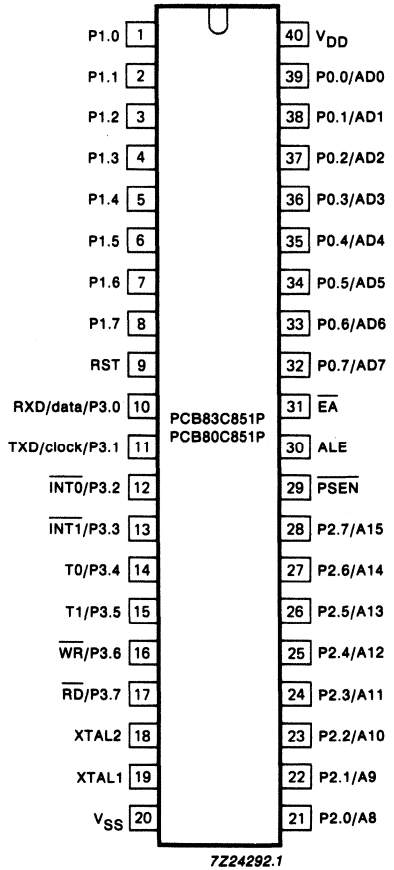


Fig.2(a) Pinning diagram (DIL versions).

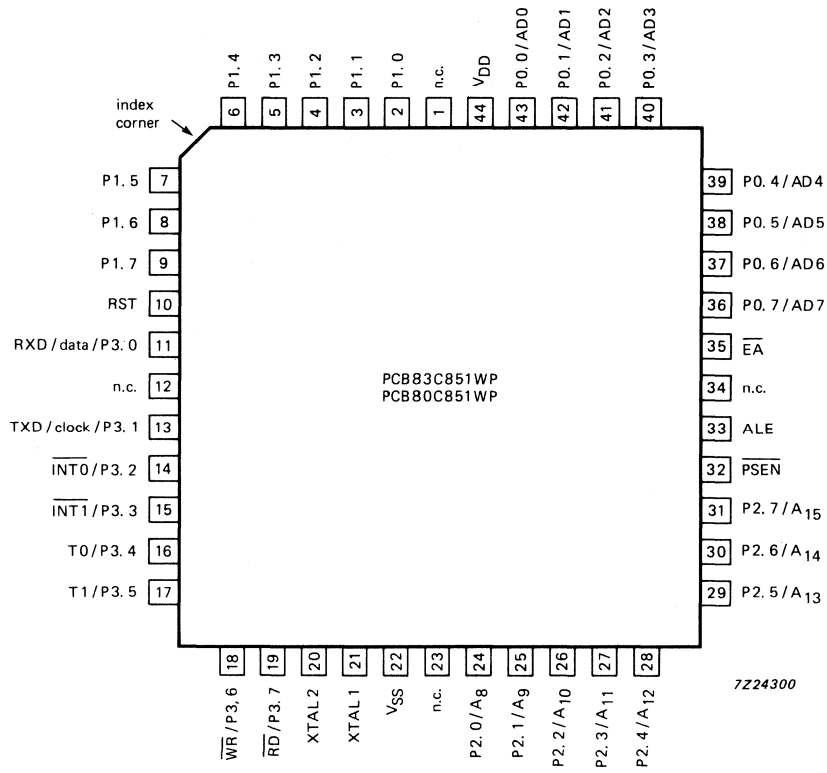


Fig.2(b) Pinning diagram (PLCC versions).

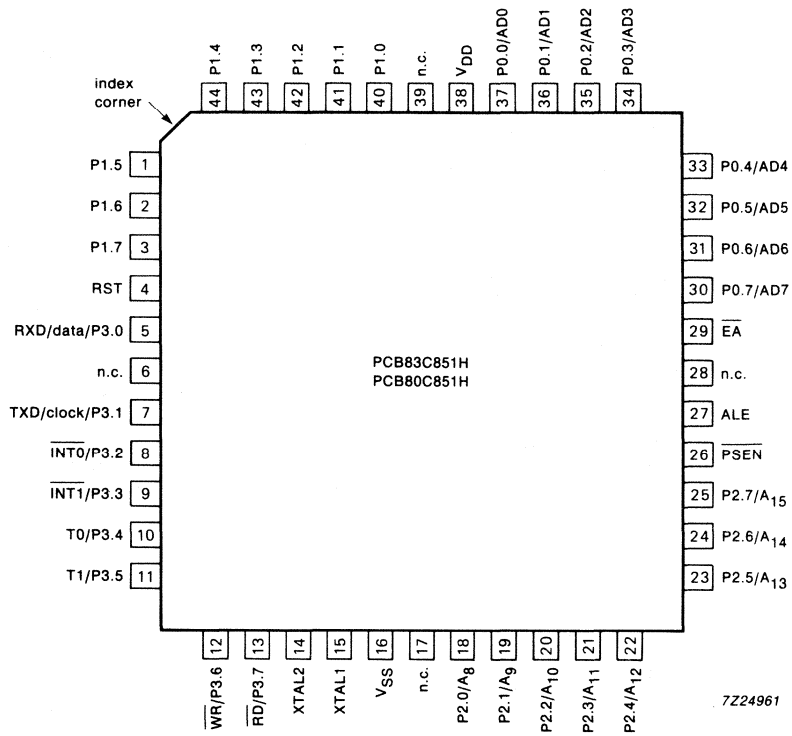


Fig.2(c) Pinning diagram (QFP versions).

PINNING (DIL versions)

PIN NO.	DESIGNATION	FUNCTION
1 - 8	P1.0 - P1.7	Port 1: 8-bit quasi bidirectional I/O port with internal pull-up. Port 1 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups.
9	RST	Reset: a high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down permits Power-on reset using only a capacitor connected to V_{DD}.
10 – 17	P3.0 – P3.7	Port 3: 8-bit quasi bidirectional I/O port. Port 3 has the following alternate functions:
10	P3.0/RXD	RXD/data: serial port receiver data input (asynchronous) or data input/output (synchronous).
11	P3.1/TXD	TXD/clock: serial port transmitter data output (asynchronous) or clock output (synchronous).
12	P3.2/$\overline{INT0}$	External interrupt 0 or gate control input for timer/event counter 0.
13	P3.3/$\overline{INT1}$	External interrupt 1 or gate control input for timer/event counter 1.
14	P3.4/T0	External input for timer/event counter 0.
15	P3.5/T1	External input for timer/event counter 1.
16	P3.6/$\overline{WR}$	External data memory write strobe.
17	P3.7/$\overline{RD}$	External data memory read strobe.
		Operation of an alternative function is automatic provided that the associated SFR bit is set HIGH.
18	XTAL2	Crystal input 2: output of the inverting amplifier that forms the oscillator; left open when an external oscillator is used (see Fig.10).
19	XTAL1	Crystal input 1: input to the inverting amplifier that forms the oscillator, and input from an external clock generator. Receives the external oscillator signal when an external oscillator is used (see Fig.10).
20	V_{SS}	Ground: circuit ground potential.
21 - 28	P2.0 - P2.7	Port 2: 8-bit quasi bidirectional I/O port. Port 2 is used during external memory accesses to output the high order byte of the external memory address if the address is 16 bits wide. If the address is 8 bits wide (data memory accesses only), Port 2 outputs the contents of the Port 2 special function register.
29	$\overline{PSEN}$	Program store enable output: read strobe to the external program memory. It is activated twice each machine cycle during fetches from external program memory. When executing out of external program memory, two activations of $\overline{PSEN}$ are skipped during each access to external data memory. $\overline{PSEN}$ is not activated (remains HIGH) during fetches from internal program memory. $\overline{PSEN}$ can sink/source 8 LSTTL inputs. It can drive CMOS inputs without an external pull-up.
29	ALE	Address latch enable output: latches the low byte of the address during access to external memory in normal operation. It is activated every six oscillator periods except during an external data memory access. ALE can sink/source 8 LSTTL inputs. It can drive CMOS inputs without an external pull-up.
31	$\overline{EA}$	External access input: When $\overline{EA}$ is held at a TTL HIGH level, the CPU executes out of the internal program memory (ROM), provided the program counter is less than 4096. When $\overline{EA}$ is held at a TTL LOW level, the CPU executes out of external program memory. The status of the $\overline{EA}$ pin can only be changed during Reset.
32 - 39	P0.7 - P0.0	Port 0: 8-bit bidirectional I/O port. It is also used as the multiplexed low-order address and data bus during access to external memory (during these accesses, it activates internal pull-ups). Port 0 can sink/source 8 LSTTL inputs.
40	V_{DD}	Power supply: + 5 V power supply pin during normal operation, Idle mode and Power-down mode. In Power-down mode, V_{DD} may be reduced to minimize circuit power consumption.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input voltage on any pin with respect to ground (V_{SS})	V_I	−0.5	+6.5	V
Input or output DC current on any single I/O pin	I_I, I_O	–	± 5	mA
Total power dissipation	P_{tot}	–	1	W
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range				
PCB version	T_{amb}	0	+ 70	°C
PCF version	T_{amb}	−40	+ 85	°C

DC CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = 0 to + 70 °C (PCB), −40 to + 85 °C (PCF); all voltages with respect to V_{SS} unless otherwise specified.

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Supply voltage		V_{DD}	4.5	5.5	V
Supply current					
operating	f_{OSC} = 12 MHz, (note 1)	I_{DD}	–	24	mA
idle mode	f_{OSC} = 12 MHz, (note 2)	I_{ID}	–	5	mA
power-down current	$2V < V_{DD} < V_{DD}$max, (note 3)	I_{PD}	–	100	µA
Inputs					
LOW level input voltage (except $\overline{EA}$)		V_{IL}	−0.5	$0.2V_{DD}$−0.1	V
LOW level input voltage $\overline{EA}$		V_{IL1}	−0.5	$0.2V_{DD}$−0.3	V
HIGH level input voltage (except RST and XTAL1)		V_{IH}	$0.2V_{DD}$+0.9	V_{DD}+0.5	V
HIGH level input voltage (RST and XTAL1)		V_{IH1}	$0.7V_{DD}$	V_{DD}+0.5	V
Input current logic 0 (Ports 1,2 and 3)	V_I = 0.45 V	$-I_{LI}$	–	50	µA
Input current logic 1 to 0 transition (Ports 1,2 and 3)	V_I = 2.00 V	$-I_{TL}$	–	650	µA
Input leakage current (Port 0, $\overline{EA}$)	$0.45 < V_I < V_{DD}$	$\pm I_{LI}$	–	10	µA
Outputs					
LOW level output voltage (Ports 1,2 and 3)	I_{OL} = 1.6 mA, (note 4)	V_{OL}	–	0.45	V
Low level output voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA, (note 4)	V_{OL1}	–	0.45	V
HIGH level output voltage (Ports 1,2 and 3)	$-I_{OH}$ = 60 µA	V_{OH}	2.4	–	V
	$-I_{OH}$ = 25 µA	V_{OH}	$0.75V_{DD}$	–	V
	$-I_{OH}$ = 10 µA	V_{OH}	$0.9V_{DD}$	–	V

DC CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
HIGH level output voltage (Port 0 in external Bus mode, ALE, $\overline{PSEN}$)	(note 5)				
	$-I_{OH} = 400\ \mu A$	V_{OH1}	2.4	–	V
	$-I_{OH} = 150\ \mu A$	V_{OH1}	$0.75V_{DD}$		V
	$-I_{OH} = 40\ \mu A$	V_{OH1}	$0.9V_{DD}$		V
RST pull-down resistor		R_{RST}	50	150	kΩ
Capacitance of I/O Buffer	frequency = 1 MHz, T_{amb} = 25 °C	$C_{I/O}$	–	10	pF
EEPROM					
Erase/write cycles	(note 6)	NE/W	10000	–	cyles
Erase/write cycle time		$t_{e/w}$	20	100	ms
Erase time		t_e	10	100	ms
Write time		t_w	10	100	ms
Data retention time	T_{amb} = + 55 °C	t_s	10	–	years

Notes to the DC characteristics

1. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10$ ns; $V_{IL} = V_{SS} + 0.5V$; $V_{IH} = V_{DD} - 0.5$; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = V_{DD}.
2. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10$ ns; $V_{IL} = V_{SS} + 0.5V$; $V_{IH} = V_{DD} - 0.5$; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}.
3. The power-down current is measured with all output pins disconnected; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = XTAL1 = V_{SS}.
4. Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make a 1-to-0 transition during bus operations. In the most adverse condition (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In this event it may be required to qualify ALE with a Schmitt-trigger, or use an address latch with a Schmitt trigger STROBE input.
5. Capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{DD}$ specification when the address bits are stabilizing.
6. Number of erase/write cycles for each EEPROM byte.

AC CHARACTERISTICS

V_{DD} = 5 V ± 10%, V_{SS} = 0 V. T_{amb} = 0 to + 70 °C (PCB version); T_{amb} = −40 to + 85 °C (PCF version). CL = 100 pF for Port 0, ALE and $\overline{PSEN}$; CL = 80 pF for all other outputs; unless otherwise specified. $t_{CK} = 1/f_{OSC}$; $t_{CY} = 12t_{CK}$.

PARAMETER	SYMBOL	f_{osc} =12 MHz		f_{osc} = VARIABLE		UNIT
		MIN.	MAX.	MIN.	MAX.	
External program memory (see Fig.15)						
ALE pulse duration	t_{LL}	127	–	$2t_{CK}-40$	–	ns
Address set-up time to ALE	t_{AL}	28	–	$t_{CK}-55$	–	ns
Address hold time after ALE	t_{LA}	48	–	$t_{CK}-35$	–	ns
Time from ALE to valid instruction input	t_{LIV}	–	233	–	$4t_{CK}-100$	ns
Time from ALE to control pulse $\overline{PSEN}$	t_{LC}	43	–	$t_{CK}-40$	–	ns
Control pulse duration $\overline{PSEN}$	t_{CC}	205	–	$3t_{CK}-45$	–	ns
Time from $\overline{PSEN}$ to valid instruction input	t_{CIV}	–	145	–	$3t_{CK}-105$	ns
Input instruction hold time after $\overline{PSEN}$	t_{CI}	0	–	0	–	ns
Input instruction float delay after $\overline{PSEN}$ (Note 1)	t_{CIF}	–	59	–	$t_{CK}-25$	ns
Address to valid instruction input	t_{AIV}	–	312	–	$5t_{CK}-105$	ns
Address float time to $\overline{PSEN}$	t_{AFC}	–	10	–	10	ns
External data memory (see Figs 16 and 17)						
ALE pulse duration	t_{LL}	127	–	$2_{CK}-40$	–	ns
Address set-up time to ALE	t_{AL}	28	–	$t_{CK}-55$	–	ns
Address hold time after ALE	t_{LA}	48	–	$t_{CK}-35$	–	ns
$\overline{RD}$ pulse duration	t_{RR}	400		$6t_{CK}-100$	–	ns
$\overline{WR}$ pulse duration	t_{WW}	400		$6t_{CK}-100$	–	ns
$\overline{RD}$ to valid data input	t_{RD}	–	252	–	$5t_{CK}-165$	ns
Data hold time after $\overline{RD}$	t_{DR}	0	–	0	–	ns
Data float delay after $\overline{RD}$	t_{DFR}	–	97	–	$2t_{CK}-70$	ns
Time from ALE to valid data input	t_{LD}	–	517	–	$8t_{CK}-150$	ns
Address to valid data input	t_{AD}	–	585	–	$9t_{CK}-165$	ns
Time from ALE to $\overline{RD}$ or $\overline{WR}$	t_{LW}	200	300	$3t_{CK}-50$	$3t_{CK}+50$	ns
Time from address to $\overline{RD}$ or $\overline{WR}$	t_{AW}	203	–	$4t_{CK}-130$	–	ns
Time from $\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{WHLH}	43	123	$t_{CK}-40$	$t_{CK}+40$	ns
Data valid to $\overline{WR}$ transition	t_{DWX}	23	–	$t_{CK}-60$	–	ns
Data set-up time before $\overline{WR}$	t_{DW}	433	–	$7t_{CK}-150$	–	ns
Data hold time after $\overline{WR}$	t_{WD}	33	–	$t_{CK}-50$	–	ns
Address float delay after $\overline{RD}$	t_{AFR}	–	0	–	0	ns

Note to the AC Characteristics

1. Interfacing the PCB83C851 to devices with float times up to 75 ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

Philips Components

Data sheet	
status	Product specification
date of issue	October 1990

PCD3310 family
Pulse and DTMF dialler with redial

FEATURES

- Pulse and DTMF dialling
- 23-digit capacity for redial operation (cursor method)
- Memory clear and electronic notepad
- Mixed-mode dialling: start with PD and end with DTMF dialling
- Dual redial buffers for PABX and public calls
- Four extra function keys; program, flash, redial, PD to DTMF (mixed dialling)
- DTMF timing:
  manual dialling - minimum duration for bursts and pauses
  re-dialling - calibrated timing
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3.58 MHz (tv colour burst) crystal or piezo resonator
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

GENERAL DESCRIPTION

The PCD3310 family are single-chip silicon gate CMOS integrated circuits with on-chip oscillators suitable for use with 3.58 MHz crystals. They are dual-standard dialling circuits for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either DP or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial and notepad facilities.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time. For data communication mix mode dialling is also possible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage		2.5	-	6.0	V
V_{DDO}	standby supply voltage		1.8	-	6.0	V
I_{DDO}	low standby current (on hook)	V_{DDO} = 1.8 V	-	-	2	µA
	operating currents	V_{DD} = 3.0 V				
I_{DDC}	conversation mode		-	-	150	µA
I_{DDP}	pulse dialling mode		-	-	200	µA
I_{DDF}	DTMF dialling mode		-	-	0.9	µA
	DTMF output voltage level		-	192	-	mV
$V_{HG(rms)}$	HIGH group		-	150	-	mV
$V_{LG(rms)}$	LOW group					
ΔV_G	pre-emphasis of group		-	2.1	-	dB
THD	total harmonic distortion		-	–25	-	dB
Tamb	operating ambient temperature range		–25	-	+ 70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3310XP*	20	DIL	plastic	SOT146
PCD3310XT*	28	SO28	plastic	SO28; SOT136A

* When ordering 'X' is replaced by one of the letters A, C, E, F, G, H or nothing.

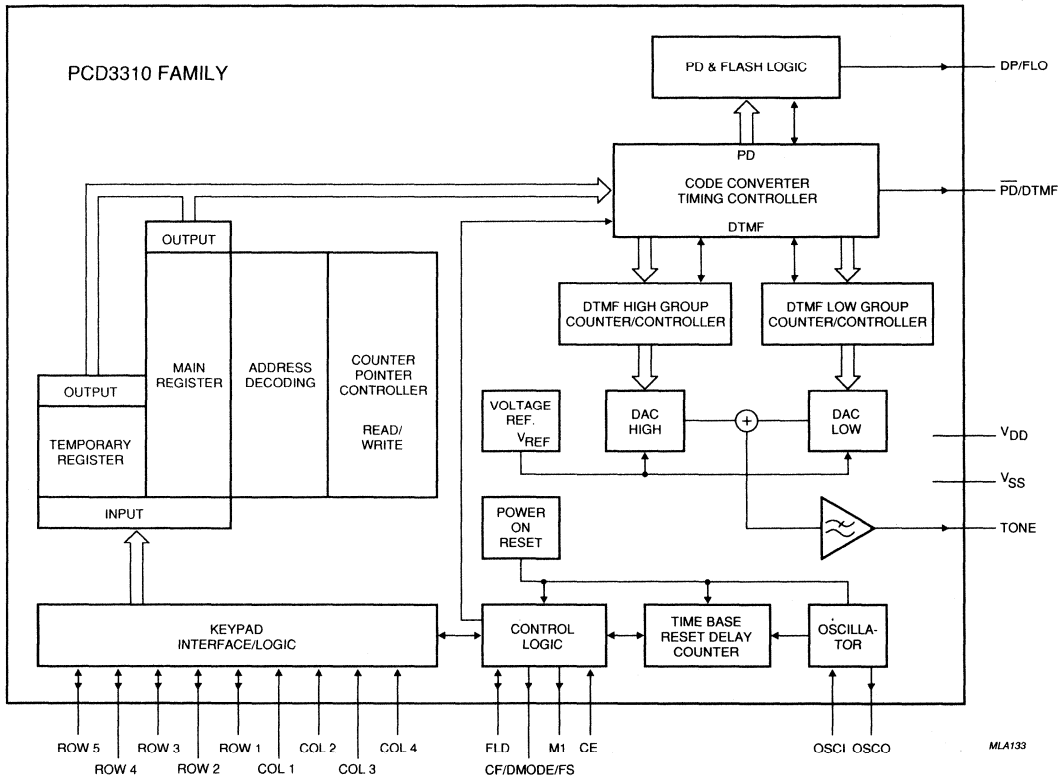


Fig.1 Block diagram.

Table 1 The PCD3310 family of ICs.

PCD3310	P/T dialler with redial, notepad, 4 x 5 keypad, flash, mark/space ratio 2:1, PABX register, automatic access pause control access to the cursor method.
PCD3310A	item PCD3310 with 3:2 mark/space ratio
PCD3310C	item PCD3310 with dialling mode output
PCD3310E	item PCD3310 with also 20 Hz pulse dialling
PCD3310F	item PCD3310 with DTMF timing of 60/90 ms
PCD3310G	item PCD3310 during switch over to data mode the '*' and '#' keys do not send out their corresponding tones
PCD3310H	item PCD3310 M1 replaced by M2

PCD3310 FAMILY SURVEY

FUNCTION	PCD3310	PCD3310A	PCD3310C	PCD3310E	PCD3310F	PCD3310G	PCD3310H
Redial key	R	R	R	R	R	R	R
Notepad keys; note 1	P/R	P/R	P/R	P/R	P/R	P/R	P/R
Mixed mode entry PD-DTMF + tone PD-DTMF no tone	 * # A-D >	 * # A-D >	 * # A-D >	 * # A-D >	 * # A-D >	 A-D > * #	 * # A-D >
Keypad (4x5, A-D)	3 x 5	3 x 5	3 x 5	3 x 5	3 x 5	3 x 5	3 x 5
Pulse dial; break/make 10 Hz, t_{id} = 840 ms 20 Hz, t_{id} = 504 ms	 67, 33	 60, 40	 67, 33	 67, 33 34, 17	 67, 33	 67, 33	 67, 33
DTMF dial: tone/pause (ms) mute hold-over	 70, 70 80	 70, 70 80	 70, 70 80	 70, 70 80	 60, 90 100	 70, 70 80	 70, 70 80
Flash (ms)	100+	100+	100+	100+	100+	100+	100+
Pin 15 (SOT146) Pin 20 (SO28; SOT136A)	CF CF	CF CF	DMODE DMODE	FS FS	CF CF	CF CF	CF CF
Memory main, data Memory PABX	23 5	23 5	23 5	23 5	23 5	23 5	23 5
SOT146 package SO28/SOT136A package	20 28	20 28	20 28	20 28	20 28	20 28	20 -

Notes to the Family survey

1. P = program, R = dial.
2. PCD3310H only available in DIL package.

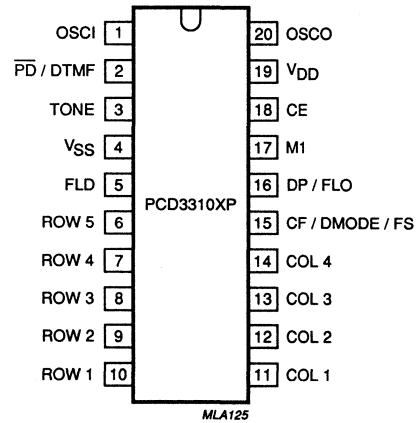


Fig.2 Pinning diagram; PCD3310XP.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input
$\overline{PD}$/DTMF	2	select pin; pulse or DTMF dialling
TONE	3	single or dual tone frequency output
V_{SS}	4	negative supply
FLD	5	flash duration control input/output
ROW 5	6	scanning row keyboard input/output
ROW 4	7	scanning row keyboard input/output
ROW 3	8	scanning row keyboard input/output
ROW 2	9	scanning row keyboard input/output
ROW 1	10	scanning row keyboard input/output
COL 1	11	sense column keyboard input
COL 2	12	sense column keyboard input
COL 3	13	sense column keyboard input
COL 4	14	sense column keyboard input
CF/DMODE/FS	15	confidence tone output, dialling mode output, frequency select
DP/FLO	16	dialling pulse and flash output
M1	17	muting output
CE	18	chip enable input
V_{DD}	19	positive supply
OSCO	20	oscillator output

Note: COL1 to COL4 have internal pull-ups.

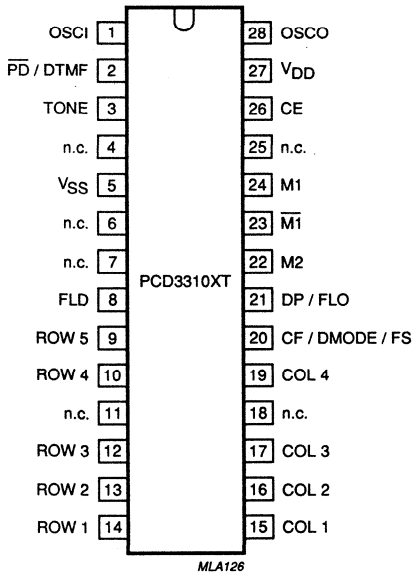


Fig.3 Pinning diagram for PCD3310XT.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{OSCI}$	1	oscillator input
$\overline{PD}$/DTMF	2	select pin; pulse or DTMF dialling
TONE	3	single or dual tone frequency output
n.c.	4	not connected
V_{SS}	5	negative supply
n.c.	6	not connected
n.c.	7	not connected
FLD	8	flash duration control input/output
ROW 5	9	scanning row keyboard input/output
ROW 4	10	scanning row keyboard input/output
n.c.	11	not connected
ROW 3	12	scanning row keyboard input/output
ROW 2	13	scanning row keyboard input/output
ROW 1	14	scanning row keyboard input/output
COL 1	15	sense column keyboard input
COL 2	16	sense column keyboard input
COL 3	17	sense column keyboard input
n.c.	18	not connected
COL 4	19	sense column keyboard input
CF/DMODE/FS	20	confidence tone output, dialling mode output, frequency select
DP/FLO	21	dialling pulse and flash output
$\overline{M2}$	22	strobe; active HIGH during transmission
$\overline{M1}$	23	inverted mute output
M1	24	muting output
n.c.	25	not connected
CE	26	chip enable input
V_{DD}	27	positive supply
OSCO	28	oscillator output

Note: COL1 to COL4 have internal pull-ups.

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the DC characteristics. To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters. If V_{DD} drops below the minimum standby supply voltage of 1.8 V the power-on reset circuit inhibits re-dialling after hook-off. The power-on reset signal has the highest priority; it blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the circuit for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3.58 MHz crystal or ceramic resonator between the OSCI and OSCO pins.

Recommended resonator type:

- 3.58 MHz PXE - Murata; CSA 3.58MG310VA.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the device.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) and Temporary WriteAddress Counter (TWAC) which point to the last entered digit (see Fig.6). The keyboard input is inhibited, but data previously entered is saved in the redial register as long as V_{DD} is higher than $V_{DDO\ (min)}$. The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on.

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or re-dialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for longer than time period t_{rd} (see Fig.10a, Fig.10b and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system changes to the static standby state. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

PD mode

If $\overline{PD}$/DTMF = V_{SS} the pulse mode is selected. Entries of non-numeric keys are neglected, they are neither stored in the redial register nor transmitted.

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each non-function key activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations. Harmonic content is filtered out thus meeting the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual key depression time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

Mixed mode

When the $\overline{PD}$/DTMF pin is open-circuit the mixed mode is selected. After activation of CE or FL (Flash) the circuit starts as a pulse dialler and remains in this state until a non-numeric key (A, B, C, D, *, # or >) is activated. The circuit then changes to DTMF dialling for data communication and remains in this state until FL is activated or after a static standby condition when CE is re-activated.

A connection between the $\overline{PD}$/DTMF pin and V_{DD} also initiates DTMF dialling. Chip enable, FL or a connection of $\overline{PD}$/DTMF pin to V_{SS} sets the circuit back to pulse dialling.

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 5 of the circuit are connected to the keyboard as shown in Fig.4. All keyboard entries are debounced on both the leading and trailing edges for approximately time period t_e as shown in Fig.11. Each entry is tested for validity. When a key is depressed, keyboard scanning starts and only returns to the sense mode after release of that key.

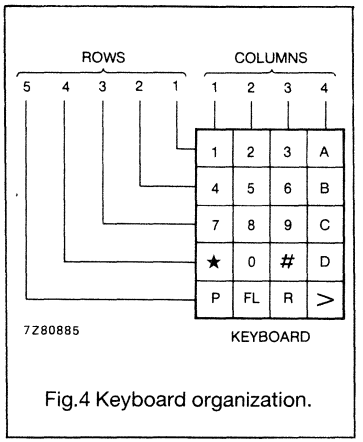


Fig.4 Keyboard organization.

Row 5 of the keyboard contains the following special function keys:

- P memory clear and programming (notepad)
- FL flash or register recall
- R redial
- > change of dial mode from PD to DTMF in mixed dialling mode

In pulse dialling mode the valid keys are the 10 numeric keys (0 to 9). The non-numeric keys (A, B, C, D, *, #) have no effect on the dialling or the redial storage. Valid function keys are P, R and FL.

In DTMF mode all non-function keys are valid. They are transmitted as a dual tone combination and at the same time stored in the redial register. Valid function keys are P, L and R.

In mixed mode all key entries are valid and executed accordingly.

Flash duration control (FLD)

Flash (or register recall) is activated by the FL key and can be used in DTMF and pulse dialling modes. Pressing the FL key will produce a timed line-break of 100 ms (min.) at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. The flash pulse duration (t_{FL}) is calibrated and can be prolonged with an external resistor and capacitor connected to the FLD input/output (see Fig.5). The flash pulse resets the Read Address Counter (RAC). Later redial is possible (see redial procedure with the "Flash" inserted telephone number). The counter of the reset delay time is held during the period of t_{FL}.

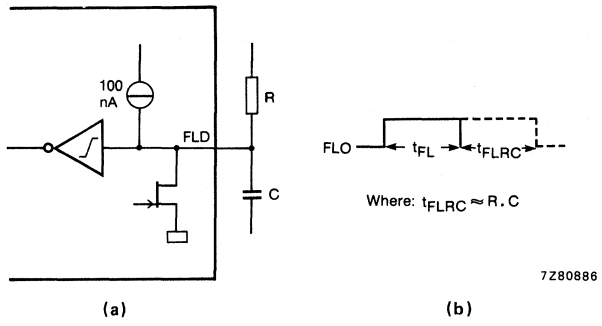


Fig.5 Flash pulse duration setting.

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter. Hence, the total harmonic distortion of the DTMF tones meets the CEPT CS 203 recommendations. The tone output has following states:

- tone OFF; 3-state
- tone ON; the associated frequencies are superimposed on a DC level of 1/2 V_{DD}.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS} and Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

Table 1 Frequency tolerance of the output tones for DTMF signalling; f_{XTAL} = 3.579545 MHz.

ROW/ COLUMN	STANDARD FREQUENCY (Hz)	TONE OUTPUT FREQUENCY (Hz)	FREQUENCY DEVIATION	
			%	Hz
Row 1	697	607.90	+ 0.13	+ 0.90
Row 2	770	770.46	+ 0.06	+ 0.46
Row 3	852	850.45	−0.18	−1.55
Row 4	941	943.23	+ 0.24	+ 2.23
Col 1	1209	1206.45	−0.21	−2.55
Col 2	1336	1341.66	+ 0.42	+ 5.66
Col 3	1477	1482.21	+ 0.35	+ 5.21
Col 4	1633	1638.24	+ 0.32	+ 5.25

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output becomes active HIGH for the period of tone transmission and remains at this level until the end of hold-over time. It is also active HIGH during flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD3310P it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break or make time in pulse dialling, or during tone ON/OFF in DTMF dialling. It is an open drain p-channel output.

DIALLING PROCEDURES
(see Figs.8 to 10)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig.6). By entering the first valid digit, the Temporary Write Address Counter (TWAC) will be set to the first address, the decoded digit will be stored in the register and the TWAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. The first 5 valid entries have no effect on the main register and its associated Write Address Counter. After the sixth valid digit is entered TWAC indicates an overflow condition. The data from the temporary register will be copied into the 5 least significant places of the main register and TWAC into the WAC. All following digits (including the sixth digit) will be stored in the main register (a total of not more than 23). If more than 23 digits are entered redial will be inhibited. If not more than 5 digits are entered only the temporary register and the associated TWAC are affected. Allentries are debounced on both the leading and trailing edges for at least time period t_e as shown in Fig.11. Each entry is tested for validity before being stored in the redial register.

- In DTMF mode all non-function keys are valid
- In PD mode only numeric keys are valid

Simultaneous to their acceptance and corresponding to the selected mode (PD, DTMF or mixed), the entries are transmitted as PD pulse-trains or as DTMF frequencies in accordance with postal requirements. Non-numeric entries are neglected during pulse dialling, they are neither stored nor transmitted.

Re-dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The circuit is in the conversation mode. If "R" is the first keyboard entry the circuit starts re-dialling the contents of the temporary register. If the overflow flag of the TWAC was set in the previous dialling, the re-dialling continues in the main register. If the flag was not set, the number residing in the temporary register will only be redialled until the temporary read and write registers are equal.

Before pressing "R" a dialling sequence with up to 4 digits is possible. If the digits are equal to the corresponding ones in the main register, then redial starts in the main register until the last digit stored is transmitted.

Timing in the DTMF mode is calibrated for both tone bursts and pauses.

In mixed mode only the first part entered (the pulse dialled part of the stored number) can be redialled.

During redial keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of re-dialling. No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory clear ("P" without successive data entry)
- Memory overflow (more than 23 valid data entries)

Notepad

The redial register can also be used as a notepad. In conversation mode a number with up to 23 digits can be entered and stored for re-dialling. By activating the program key (P) the WAC and TWAC pointers are reset. This acts like a memory clear (redial is inhibited). Afterwards, by entering and storing any digits, re-dialling will be possible after flash or hook on and off.

During notepad programming the numbers entered will neither be transmitted nor is the mute active, only the confidence tone is generated.

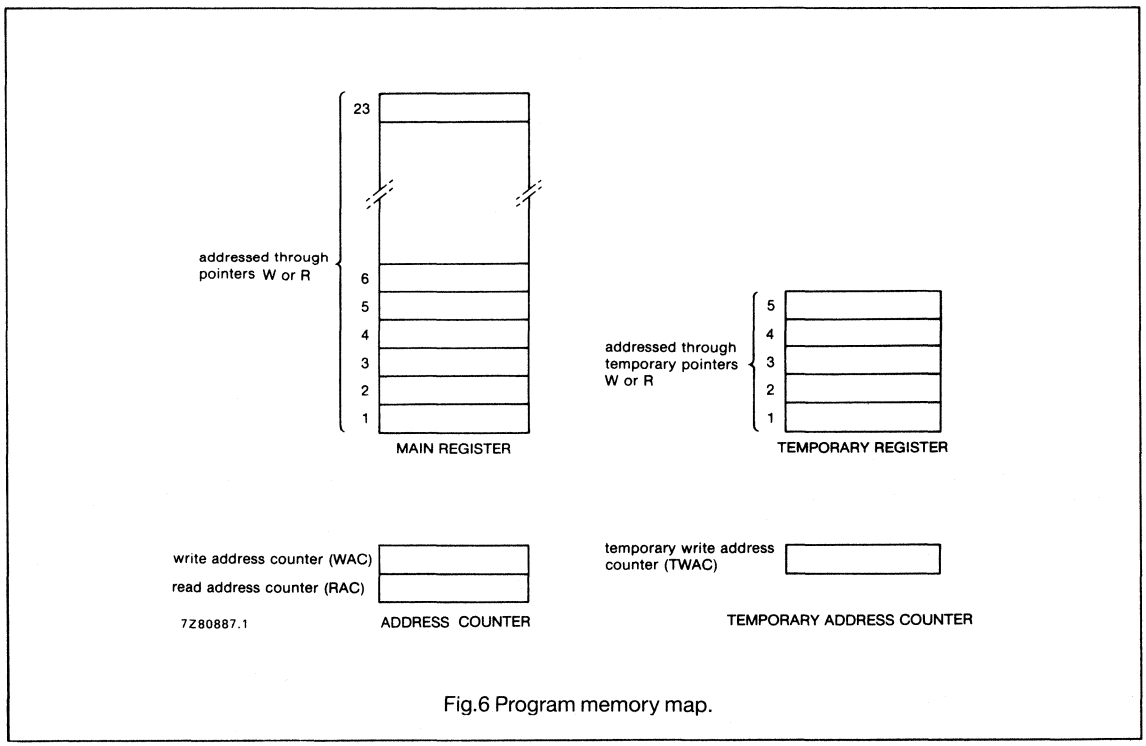


Fig.6 Program memory map.

Note to Fig.6

(1). If [access digit(s) + external number] ≤ 23 digits.

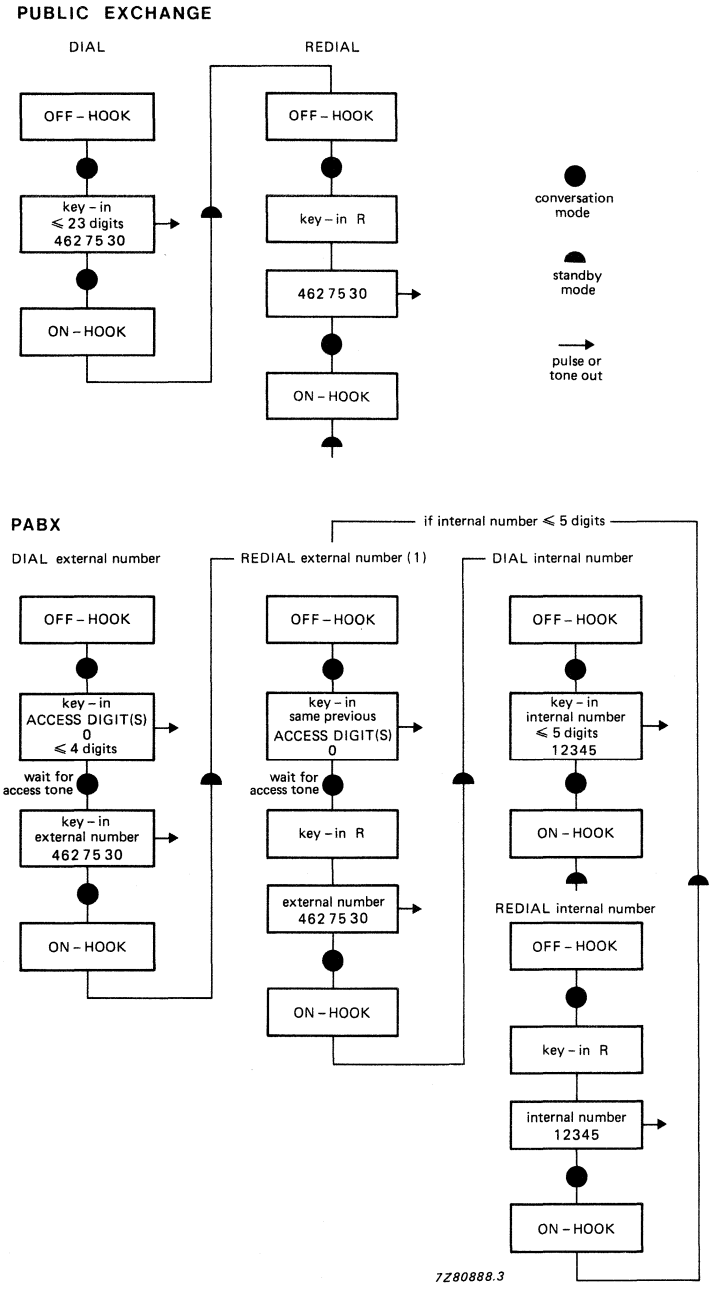


Fig.7 PD or DTMF dialling mode.

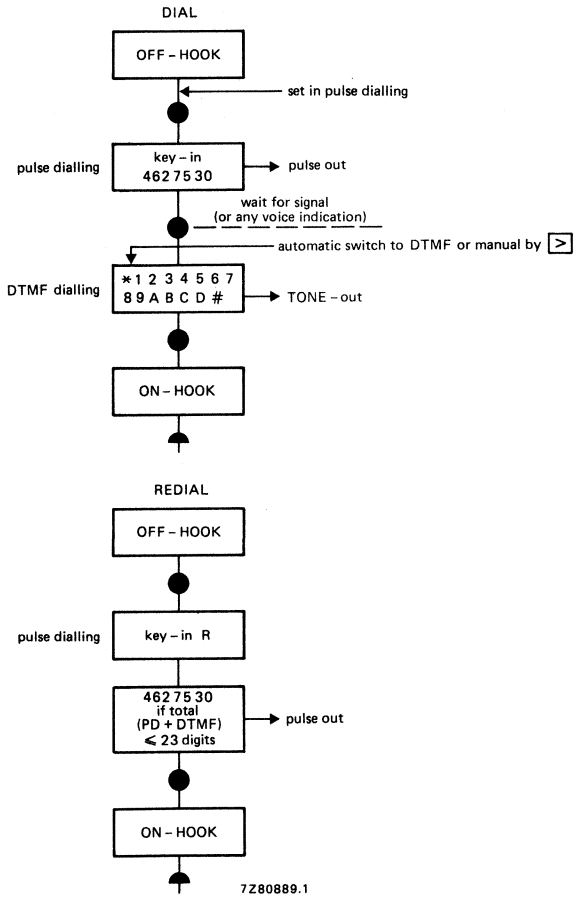


Fig.8 PD/DTMF mixed-mode dialling.

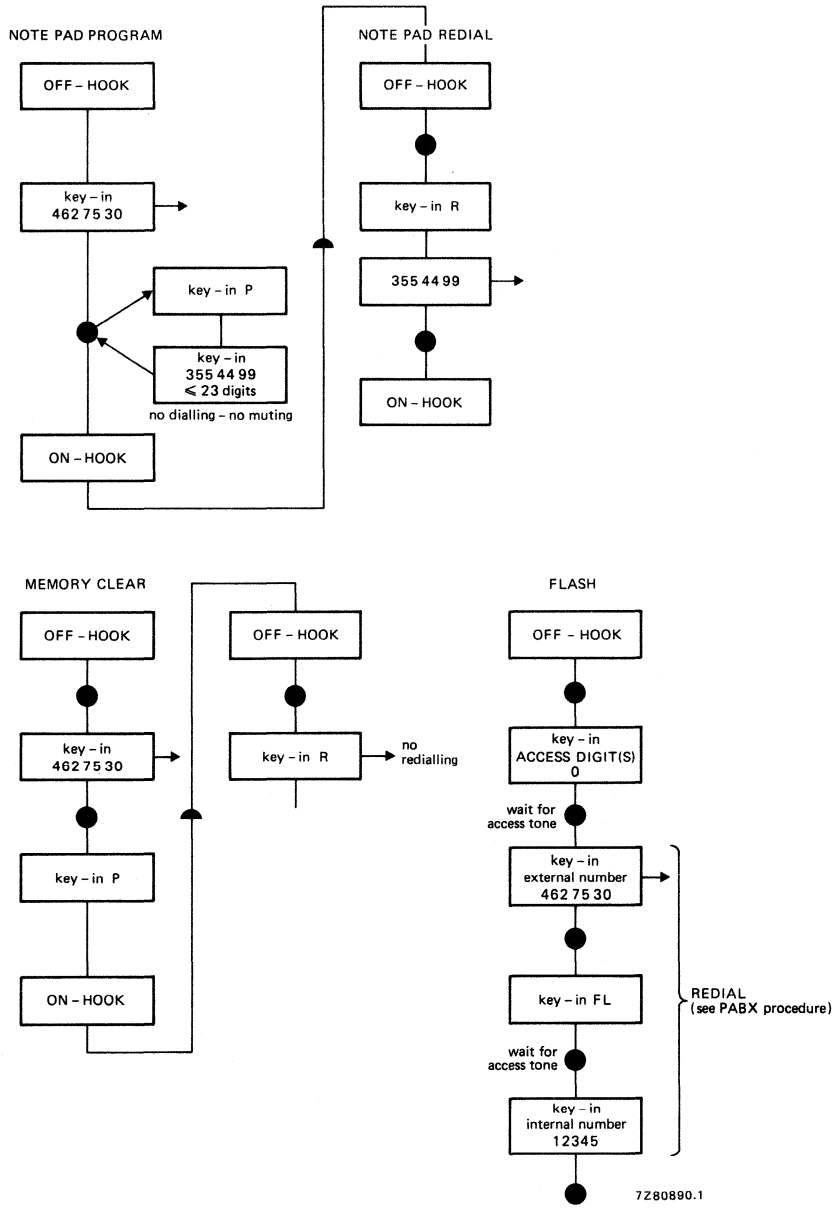


Fig.9 Notepad, memory clear, flash; independent of dialling mode

TIMING

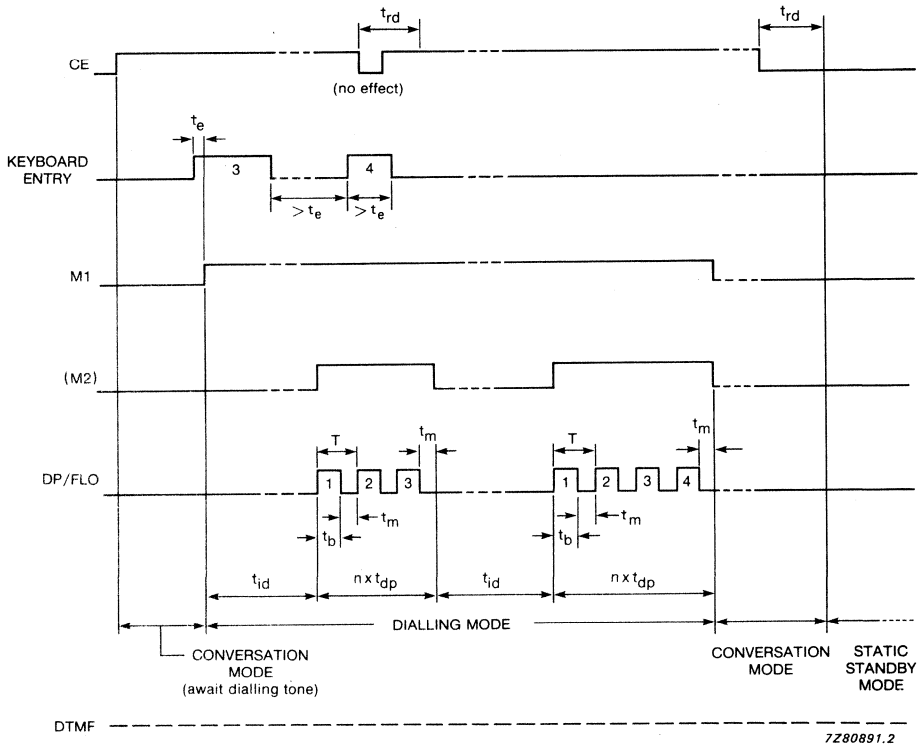


Fig.10a Timing diagram for pulse dialling ($\overline{PD}$/DTMF = V_{SS})

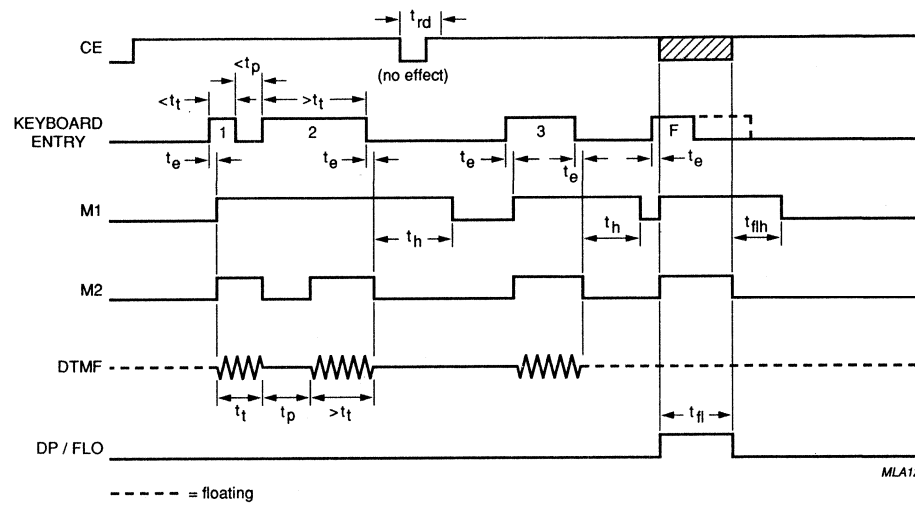


Fig.10b Timing diagram for DTMF dialling ($\overline{PD}$/DTMF = V_{DD})

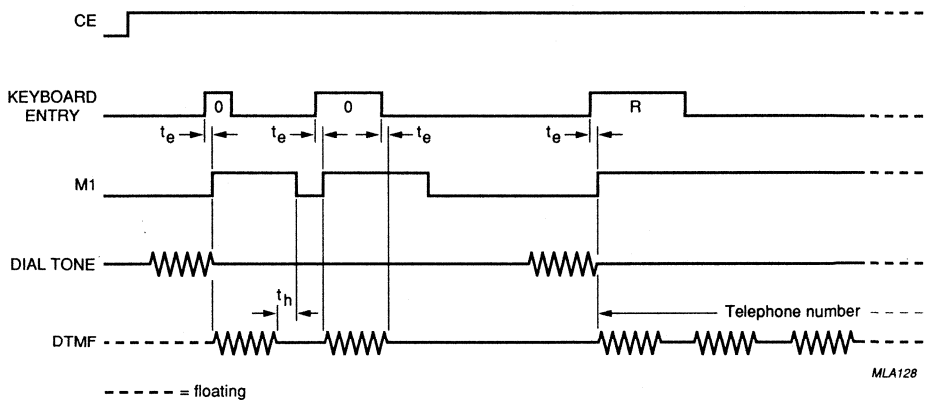


Fig.11 Timing diagram showing REDIAL where PABX access digits are the first keyboard entries in DTMF dialling mode.

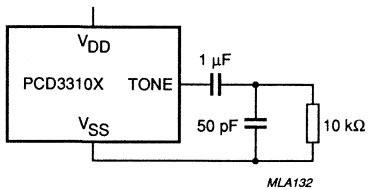


Fig.12 Tone output test circuit.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	−0.8	8	V
I_{DD}	supply current		50	mA
$\pm I_I, \pm I_O$	DC current into any input or output		10	mA
V_I	all input voltages	−0.8	V_{DD} + 0.8	V
P_{tot}	total power dissipation	-	300	mW
P_o	power dissipation per output	-	50	mW
T_{stg}	storage temperature range	−65	+ 150	°C
T_{amb}	operating ambient temperature range	−25	+ 70	°C

DC CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3.579545 MHz; T_{amb} = −25 to + 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating supply voltage		2.5	-	6.0	V
V_{DDO}	standby supply voltage		1.8	-	6.0	V
	Operating supply current					
I_{DDC}	conversation mode	oscillator ON	-	-	150	µA
I_{DDP}	pulse dialling or flash		-	-	200	µA
I_{DDF}	DTMF dialling	tone ON	-	0.6	0.9	mt
I_{DDF}	DTMF dialling	tone OFF	-	-	200	µA
I_{DDO}	standby supply current	V_{DD} = 1.8 V oscillator OFF; note 1	-	-	2	µA
Inputs						
V_{IL}	input voltage LOW (any pin)		0	-	0.3 V_{DD}	V
V_{IH}	input voltage HIGH (any pin)		0.7 V_{DD}	-	V_{DD}	V
$\lvert I_{IL} \rvert$	input leakage current; $\overline{CE}$		-	-	1	µA
Keyboard inputs						
R_{KON}	keyboard ON resistance		-	-	2	kΩ
R_{KOFF}	keyboard OFF resistance		1	-	-	MΩ
Outputs						
	output sink current	$V_{OL} = V_{SS}$ + 0.5 V				
I_{OL}	M1, $\overline{M1}$, DP/FLO, CF, FLD		0.7	-	-	mA
I_{OL}	$\overline{PD}$/DTMF	note 2	-	-	1	mA
	output source current	$V_{OH} = V_{DD}$ − 0.5 V				
$-I_{OH}$	M1, $\overline{M1}$, DP/FLO, CF, M2		0.6	-	-	mA
$-I_{OH}$	$\overline{PD}$/DTMF	note 2	-	-	1	mA
$-I_{OH}$	FLD	note 3	-	60	-	nA
Timing and frequency						
t_{on}	clock start-up time		-	4	-	ms
t_e	debounce time		-	12	-	ms
t_{rd}	reset delay time		-	160	-	ms
Tone output (see Fig.12)						
	DTMF output voltage levels	V_{DD} = 2.5 to 6 V				
$V_{HG(rms)}$	HIGH group		158	192	205	mV
$V_{LG(rms)}$	LOW group		125	150	160	mV
$\Delta f/f$	frequency deviation		−0.6	-	+ 0.6	%
V_{DC}	DC voltage level		-	1/2 V_{DD}	-	V
$\lvert Z_O \rvert$	output impedance		-	0.1	0.5	kΩ
ΔV_G	pre-emphasis of group		1.85	2.1	2.35	dB
THD	total harmonic distortion	T_{amb} = 25 °C, note 4	-	−25	-	dB

Notes to the DC characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. < |10 mA| dynamic current to set/reset $\overline{PD}$/DTMF pin (mixed mode).
3. Flash inactive; $V_{OH} = V_{SS}$.
4. Related to the level of the LOW group frequency component (CEPT CS 203).

TYPE NUMBER DEPENDENT CHARACTERISTICS

PCD3310

Confidence tone output (CF)

The confidence tone output pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

When any key is activated a square-wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	redialling	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms

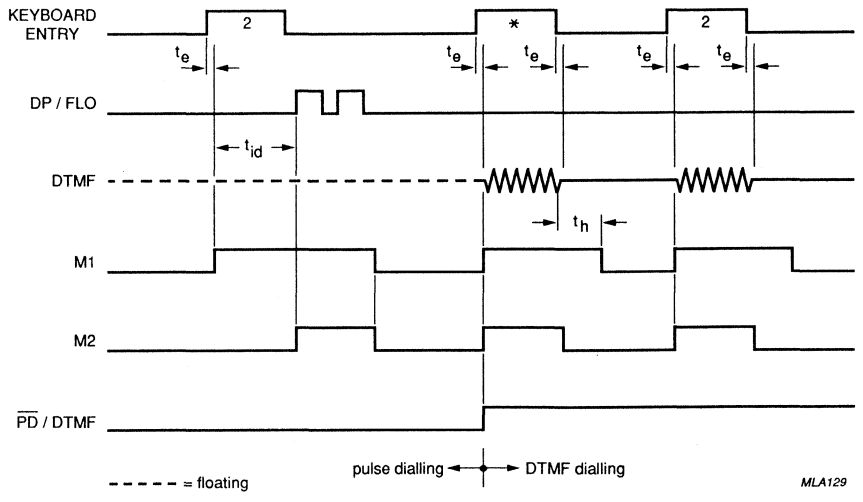


Fig.13 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310A

Confidence tone output (CF)

The confidence tone output pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

When any key is activated a square-wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	redialling	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	59	60	61	ms
t_m	make time	39	40	41	ms

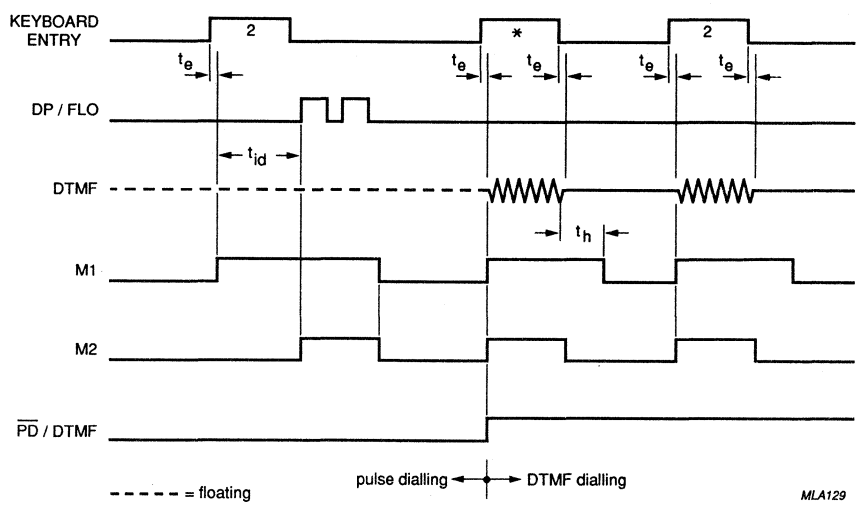


Fig.14 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310C

Dialling mode output (DMODE)

The dialling mode output is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

The DMODE output represents the actual dialling status of the dialler. In pulse mode the output is LOW and in DTMF mode the output is HIGH.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	redialling	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms

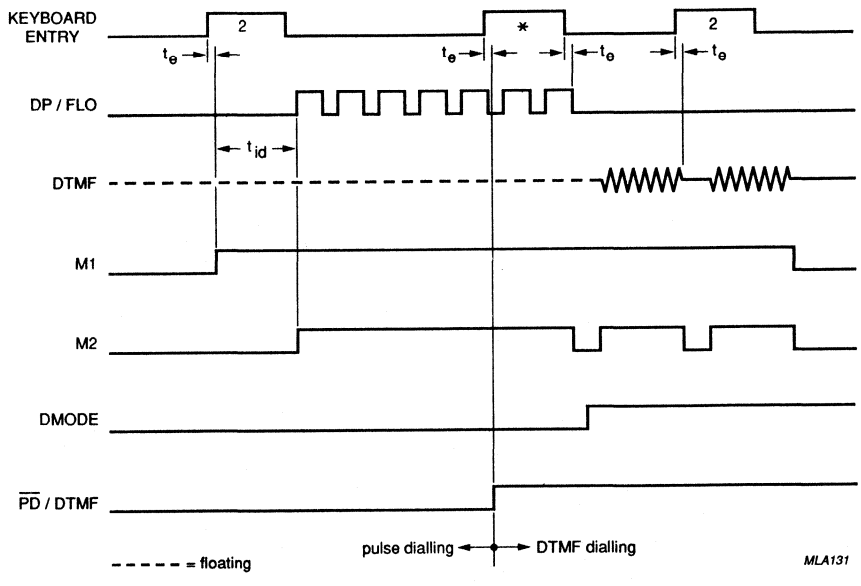


Fig.15 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310E

Pulse dialling frequency select (FS)

The frequency select pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT146 package.

If FS = V_{SS}; 10 Hz dialling selected. If FS = V_{DD}; 30 HZ dialling selected.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	retailing	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling @ 10 Hz					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms
Pulse dialling @ 20 Hz					
f_{dp}	dialling pulse frequency	19.6	20	20.8	Hz
t_{id}	inter-digit pause	496	504	512	ms
t_b	break time	33	34	35	ms
t_m	make time	16	17	18	ms

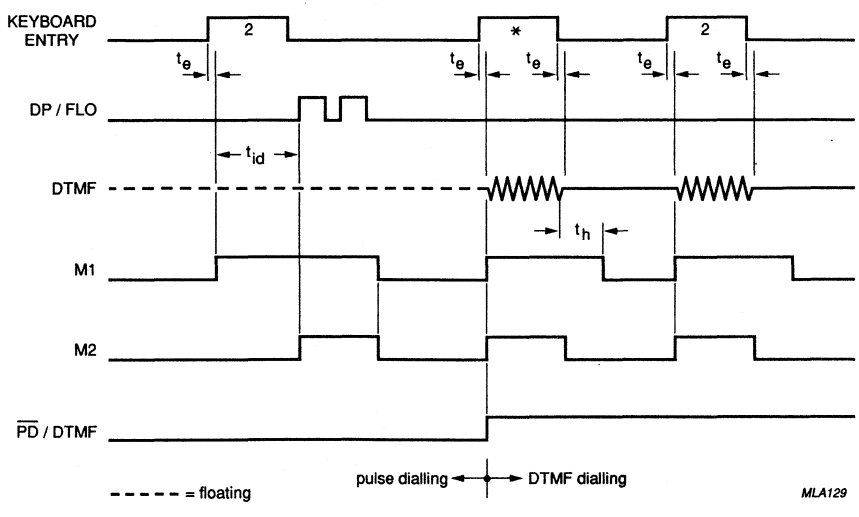


Fig.16 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310F

Confidence tone output (CF)

The confidence tone output pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

When any key is activated a square-wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t	manual dialling	59	-	-	ms
t_p		89	-	-	ms
t_t	retailing	59	60	61	ms
t_p		89	90	91	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	99	100	101	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms

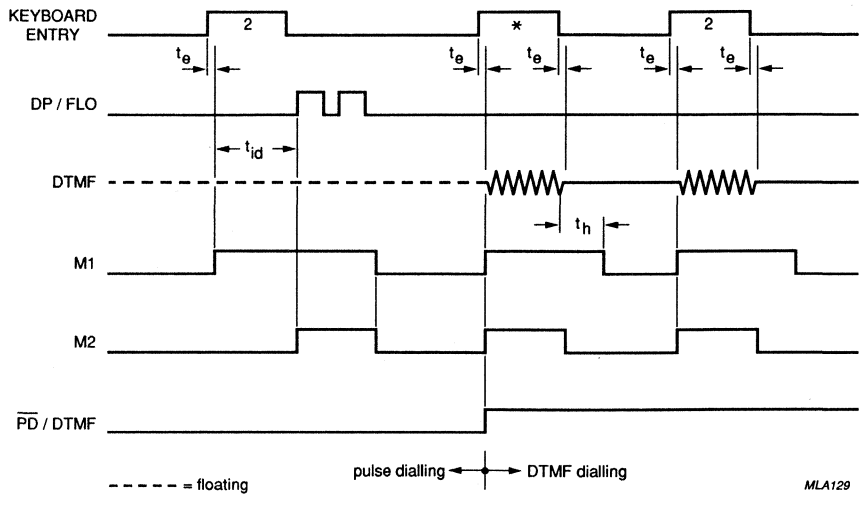


Fig.17 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310G

Confidence tone output (CF)

The confidence tone output pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

When any key is activated a square-wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

In mixed mode dialling the switch-over from pulse to DTMF mode can be activated by the * and # keys without sending out its corresponding frequencies when activated for the first time.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	retailing	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms

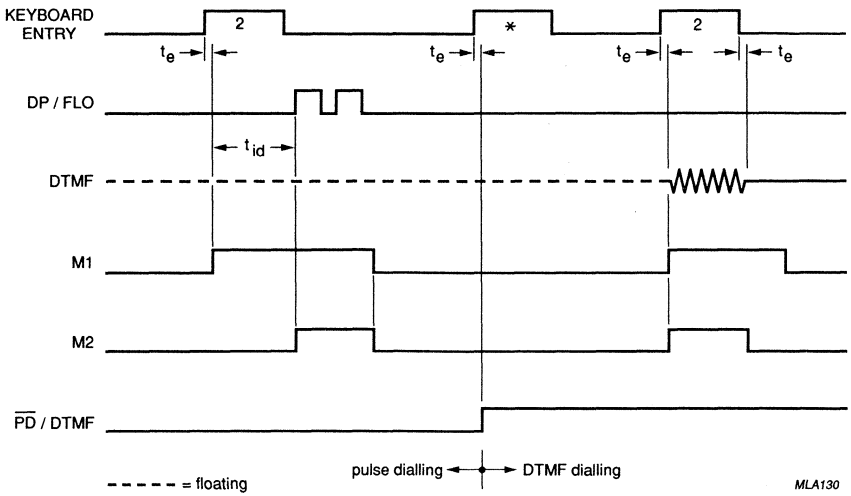


Fig.18 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

APPLICATION INFORMATION

1. Automatic line compensation obtained by connecting R6 to V_{SS}.
2. The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA 1060/61.

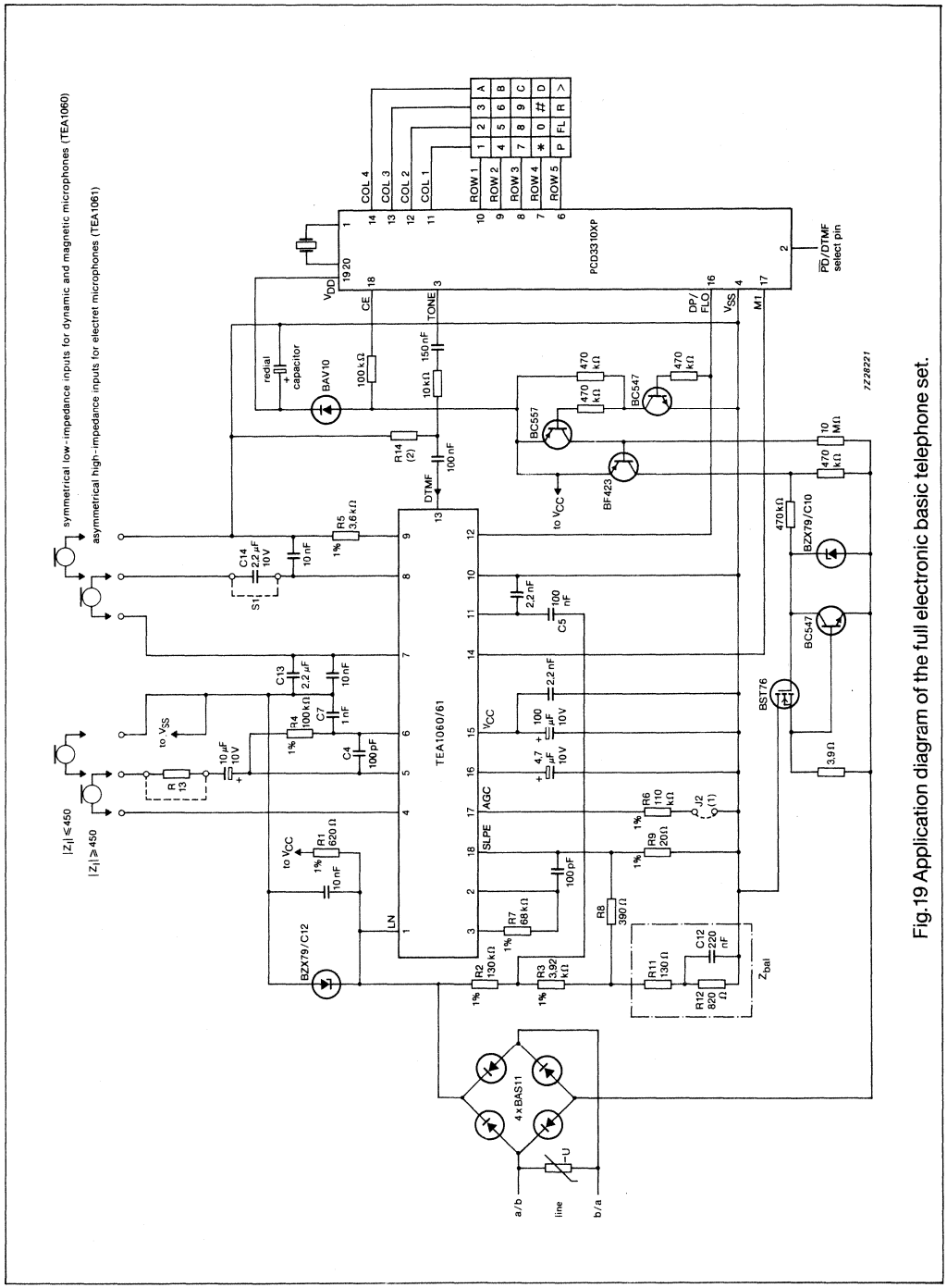


Fig.19 Application diagram of the full electronic basic telephone set.

DTMF/MODEM/MUSICAL-TONE GENERATORS

GENERAL DESCRIPTION

The PCD3311C and PCD3312C are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C-bus).

With their on-chip voltage reference the PCD3311C and PCD3312C provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT T/CS46-03 (= former CS203) recommendations.

In addition to the standard DTMF frequencies the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C-bus compatible
- Mode select input (selection of parallel or serial data input)
- MODEM and melody tone generators

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	0,9	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (RMS values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	−25	–	dB
Operating ambient temperature range	T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

PCD3311CP: 14-lead DIL; plastic (SOT27).
PCD3311CT: 16-lead mini-pack; plastic (SO16L; SOT162A).
PCD3312CP: 8-lead DIL; plastic (SOT97).
PCD3312CT: 8-lead mini-pack; plastic (SO8L; SOT176C).

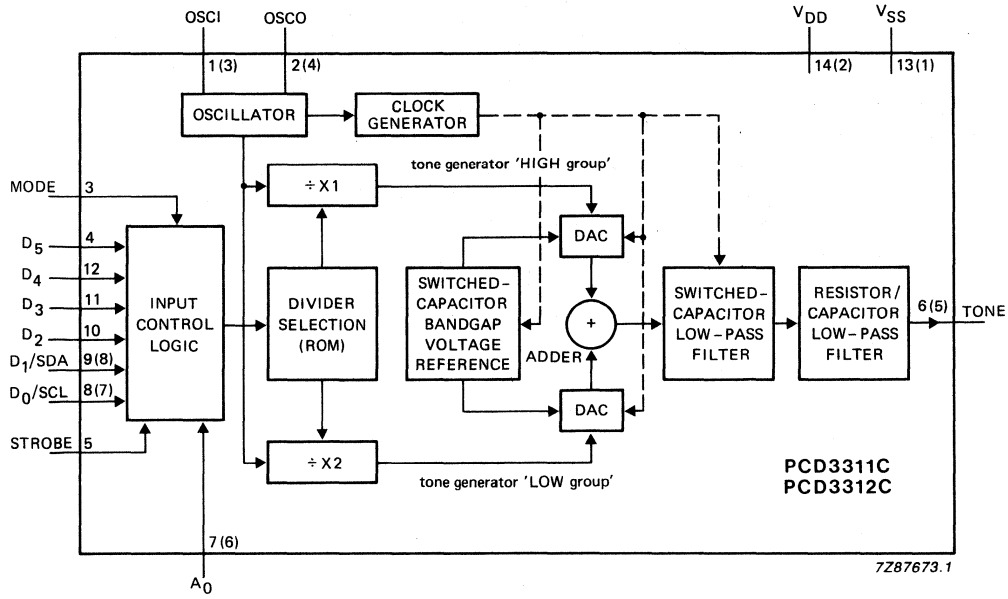


Fig. 1 Block diagram; the pin numbers in parenthesis refer to the PCD3312C.

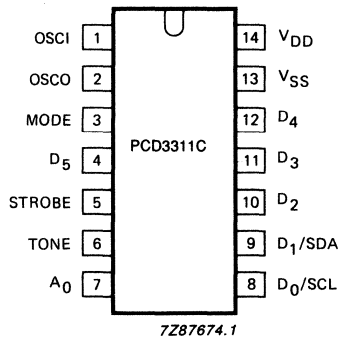


Fig. 2 Pinning diagram for the PCD3311CP.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
5	STROBE	strobe input; used for the loading of data in the parallel mode
6	TONE	frequency output for single or dual tones
7	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
8	D_0/SCL	parallel data input* or serial clock line (I^2C-bus)
9	D_1/SDA	parallel data input* or serial data line (I^2C-bus)
10	D_2	parallel data inputs*
11	D_3	
12	D_4	
13	V_{SS}	negative supply
14	V_{DD}	positive supply

* MODE = HIGH.

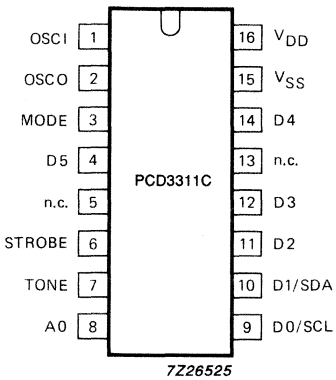


Fig. 3 Pinning diagram for the PCD3311CT.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
6	STROBE	strobe input; used for the loading of data in the parallel mode
7	TONE	frequency output for single or dual tones
8	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
9	D_0/SCL	parallel data input* or serial clock line (I^2C-bus)
10	D_1/SDA	parallel data input* or serial data line (I^2C-bus)
11	D_2	
12	D_3	parallel data inputs*
14	D_4	
15	V_{SS}	negative supply
16	V_{DD}	positive supply
5; 13	n.c.	not connected

* MODE = HIGH.

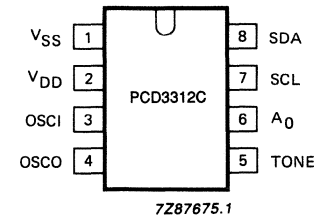


Fig. 4 Pinning diagram for the PCD3312C.

PINNING

1	V_{SS}	negative supply
2	V_{DD}	positive supply
3	OSCI	oscillator input
4	OSCO	oscillator output
5	TONE	frequency output for single or dual tones
6	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
7	SCL	serial clock line (I^2C bus)
8	SDA	serial data line (I^2C bus)

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311C and PCD3312C is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode (only for the PCD3311C), or, when connected to V_{SS} or left open, data can be received via the serial I^2C-bus (for both PCD3311C and PCD3312C).

Parallel mode can only be obtained for the PCD3311 by setting MODE input HIGH.

FUNCTIONAL DESCRIPTION (continued)

Data inputs (D_0, D_1, D_2, D_3, D_4 and D_5)

Inputs D_0 and D_1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D_2 to D_5 have internal pull-down. D_5 and D_4 are used to select between DTMF dual, DTMF single, MODEM and melody tones (see Table 1). D_3 to D_0 select the combination of the tones for DTMF or single-tone itself.

Table 1 D_5 and D_4 in accordance with the selected application

D_5	D_4	application
0	0	DTMF single tones; standby; melody tones
0	1	DTMF dual tones (all 16 combinations)
1	0	MODEM tones; standby; melody tones
1	1	melody tones

1 = H = HIGH voltage level
0 = L = LOW voltage level

Note: Tables 2, 3, 4 and 5 show all input codes and their corresponding output frequencies.

Strobe input (STROBE, only for the PCD3311C)

This input (with internal pull-down) allows the loading of parallel data into D_0 to D_5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained for the PCD3311C by setting MODE input LOW.

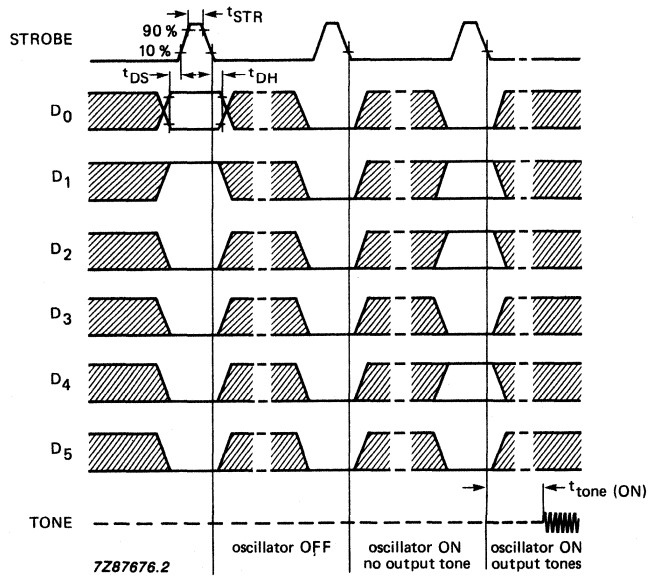


Fig. 5 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D_0 and D_1 respectively. For the PCD3311C the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I²C-bus specification (see "CHARACTERISTICS OF THE I²C-BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A_0)

A_0 is the slave address input and it identifies the device when up to two PCD3311C or PCD3312C devices are connected to the same I²C bus. In any case A_0 must be connected to V_{DD} or V_{SS}.

I²C bus data configuration (see Fig. 6)

The PCD3311C and PCD3312C are always slave receivers in the I²C-bus configuration (R/$\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode for the PCD3311C as well as for the PCD3312C, where the least significant bit is selectable by hardware on input A_0 and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 2, 3, 4, and 5). D_6 and D_7 are don't care (X) bits.

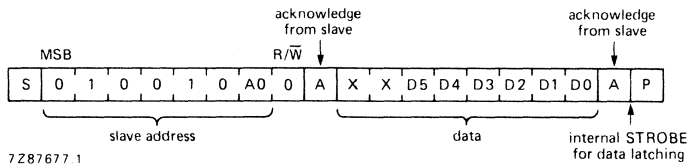


Fig. 6 I²C-bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS46-03 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling; Tables 4 and 5 for the modem and melody tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

Table 2 Input data for control (no output tone; TONE in 3-state)

D_5	D_4	D_3	D_2	D_1	D_0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

1 = H = HIGH voltage level
0 = L = LOW voltage level
X = don't care

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for DTMF

D_5	D_4	D_3	D_2	D_1	D_0	HEX	symbol	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Table 4 Input data for MODEM frequencies

D_5	D_4	D_3	D_2	D_1	D_0	HEX	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz	remarks
1	0	0	1	0	0	24	1300	1296,94	−0,24	−3,06	V.23
1	0	0	1	0	1	25	2100	2103,14	+ 0,15	+ 3,14	
1	0	0	1	1	0	26	1200	1197,17	−0,24	−2,83	Bell 202
1	0	0	1	1	1	27	2200	2192,01	−0,36	−7,99	
1	0	1	0	0	0	28	980	978,82	−0,12	−1,18	V.21
1	0	1	0	0	1	29	1180	1179,03	−0,08	−0,97	
1	0	1	0	1	0	2A	1070	1073,33	+ 0,31	+ 3,33	Bell 103
1	0	1	0	1	1	2B	1270	1265,30	−0,37	−4,70	
1	0	1	1	0	0	2C	1650	1655,66	+ 0,34	+ 5,66	V.21
1	0	1	1	0	1	2D	1850	1852,77	+ 0,15	+ 2,77	
1	0	1	1	1	0	2E	2025	2021,20	−0,19	−3,80	Bell 103
1	0	1	1	1	1	2F	2225	2223,32	−0,08	−1,68	

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level
0 = L = LOW voltage level

Table 5 Input data for melody tones

D_5	D_4	D_3	D_2	D_1	D_0	HEX	note	standard frequency Hz*	tone output frequency Hz**
1	1	0	0	0	0	30	D#5	622,3	622,5
1	1	0	0	0	1	31	E5	659,3	659,5
1	1	0	0	1	0	32	F5	698,5	697,9
1	1	0	0	1	1	33	F#5	740,0	741,1
1	1	0	1	0	0	34	G5	784,0	782,1
1	1	0	1	0	1	35	G#5	830,6	832,3
1	1	0	1	1	0	36	A5	880,0	879,3
1	1	0	1	1	1	37	A#5	932,3	931,9
1	1	1	0	0	0	38	B5	987,8	985,0
1	1	1	0	0	1	39	C6	1046,5	1044,5
1	1	1	0	1	0	3A	C#6	1108,7	1111,7
1	0	1	0	0	1	29	D6	1174,7	1179,0
1	1	1	0	1	1	3B	D#6	1244,5	1245,1
1	1	1	1	0	0	3C	E6	1318,5	1318,9
1	1	1	1	0	1	3D	F6	1396,9	1402,1
0	0	1	1	1	0	0E	F#6	1480,0	1482,2
1	1	1	1	1	0	3E	G6	1568,0	1572,0
1	0	1	1	0	0	2C	G#6	1661,2	1655,7
1	1	1	1	1	1	3F	A6	1760,0	1768,5
0	0	0	1	0	0	04	A#6	1864,7	1875,1
0	0	0	1	0	1	05	B6	1975,5	1970,0
1	0	0	1	0	1	25	C7	2093,0	2103,1
1	0	1	1	1	1	2F	C#7	2217,5	2223,3
0	0	0	1	1	0	06	D7	2349,3	2358,1
0	0	0	1	1	1	07	D#7	2489,0	2470,4

* Standard scale based on A4 = 440 Hz.

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level

0 = L = LOW voltage level

DEVELOPMENT DATA

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

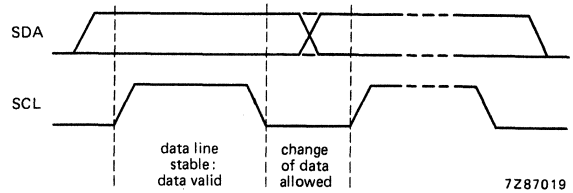


Fig. 7 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

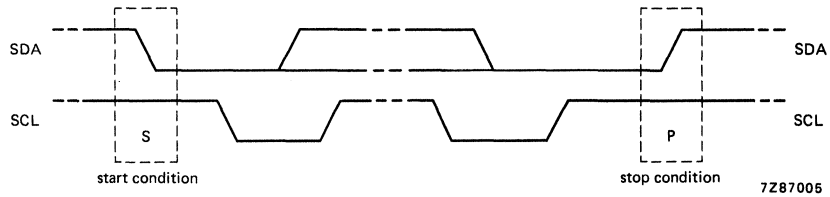


Fig. 8 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

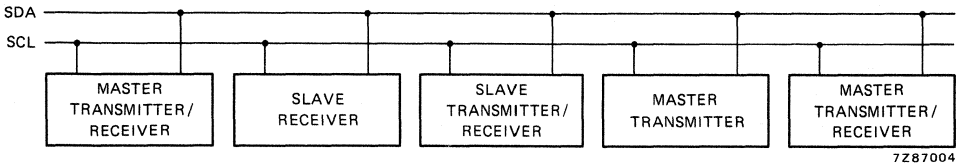


Fig. 9 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

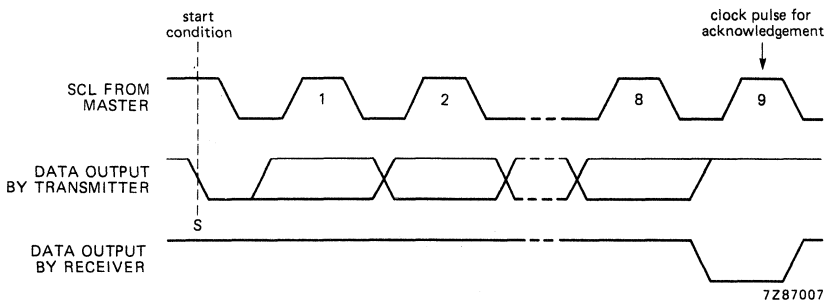


Fig. 10 Acknowledgement on the I^2C-bus.

CHARACTERISTICS OF THE I²C-BUS (continued)

Timing specifications

Within the I²C-bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 11.

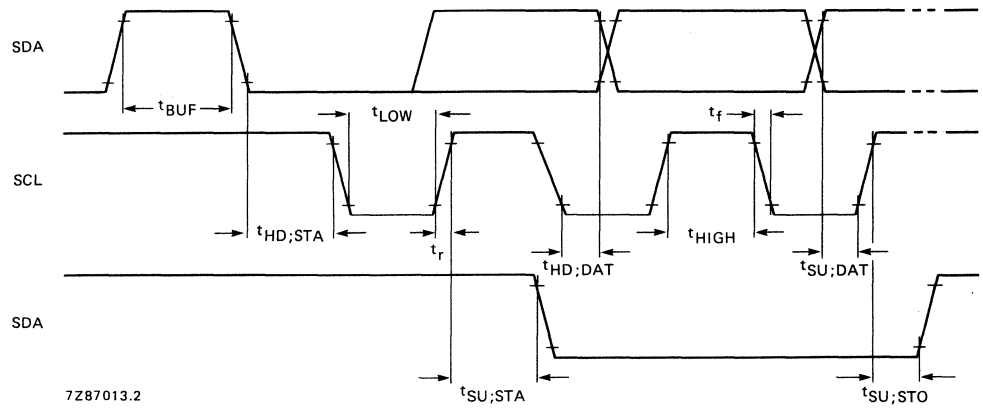


Fig. 11 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

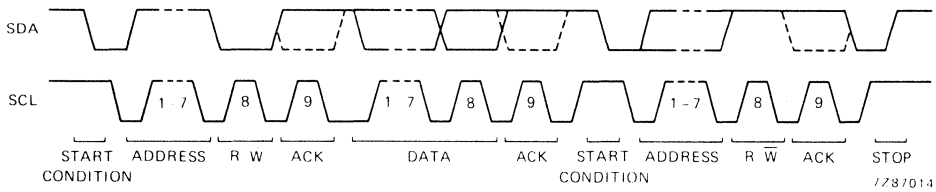


Fig. 12 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 13.

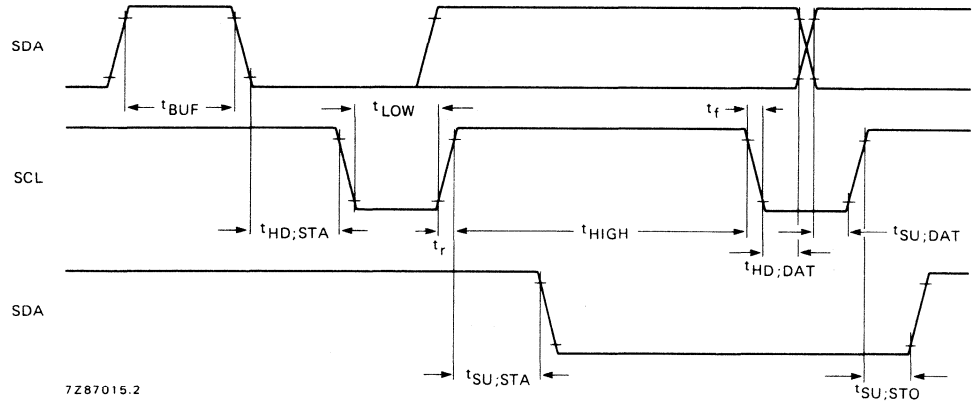


Fig. 13 Timing of the low-speed mode.

DEVELOPMENT DATA

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

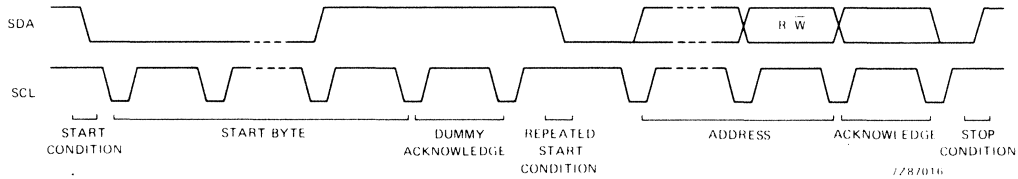


Fig. 14 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
DC input current (any input)	$\pm I_I$	–	10	mA
DC output current (any output)	$\pm I_O$	–	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Power dissipation per output	P_O	–	50	mW
Total power dissipation per package	P_{tot}	–	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 50 Ω;
T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	–	50	100	μA
single output tone	I_{DD}	–	0,5	0,8	mA
dual output tone	I_{DD}	–	0,6	0,9	mA
Static standby current oscillator OFF; note 1	I_{DDO}	–	–	3	μA
Inputs/outputs (SDA)					
D_0 to D_5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
D_2 to D_5; MODE; STROBE; A_0					
Pull-down input current V_I = V_{DD}	$-I_{IL}$	30	150	300	nA
SCL (D_0); SDA (D_1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Clock frequency (see Fig. 11)	f_{SCL}	–	–	100	kHz
Input capacitance; V_I = V_{SS}	C_I	–	–	7	pF
Allowable input spike pulse width	t_I	–	–	100	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 15)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
DC voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	–25	–	dB
modem tone, note 3	THD	–	–29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D_0/SCL and D_1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS46-03).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

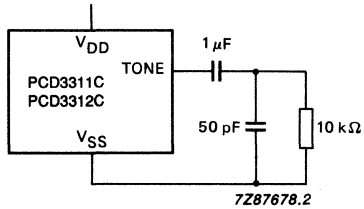


Fig. 15 TONE output test circuit.

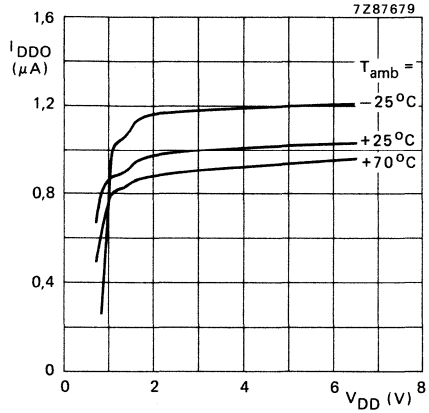


Fig. 16 Standby supply current as a function of supply voltage; oscillator OFF.

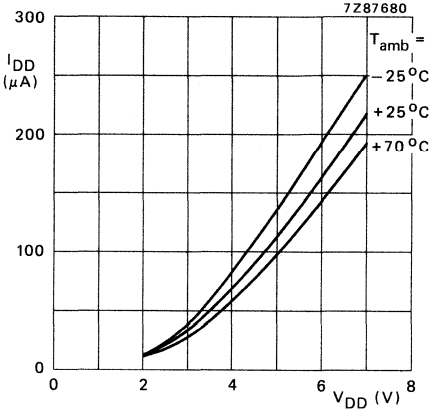


Fig. 17 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

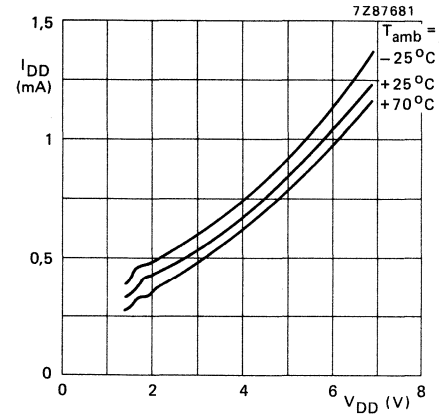


Fig. 18 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

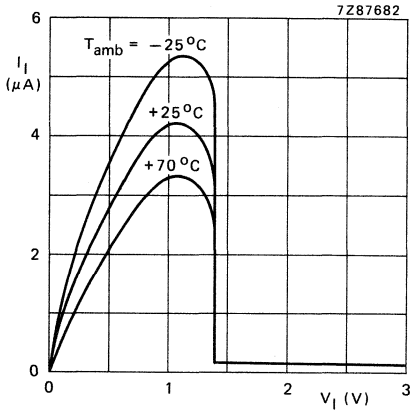


Fig. 19 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

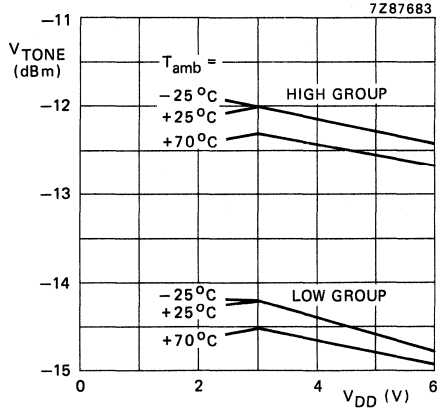


Fig. 20 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

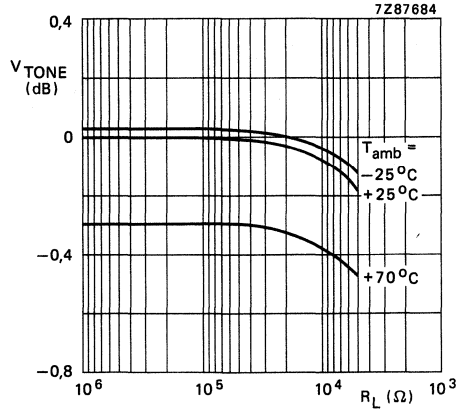


Fig. 21 Dual tone output voltage level as a function of output load resistance.

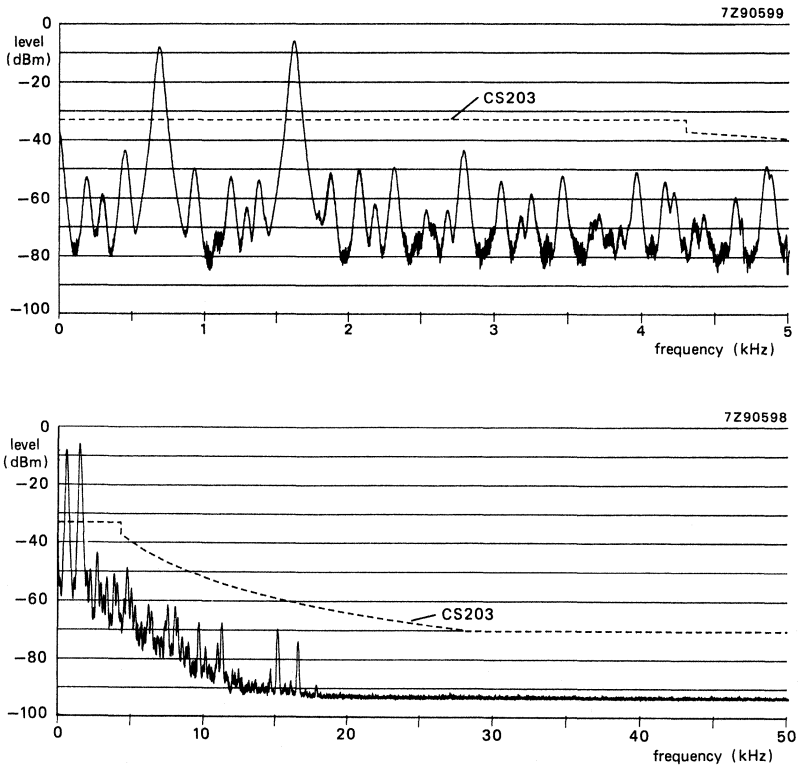


Fig. 22 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

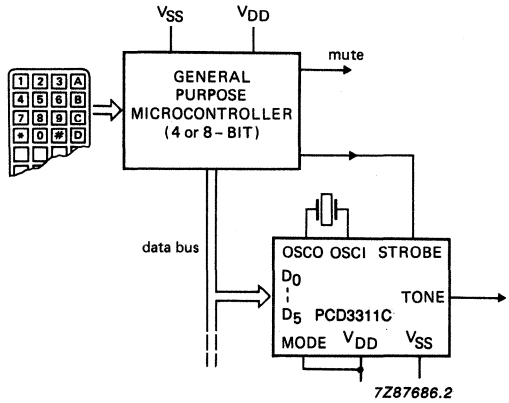


Fig. 23 PCD3311C driven by a microcontroller with parallel data bus.

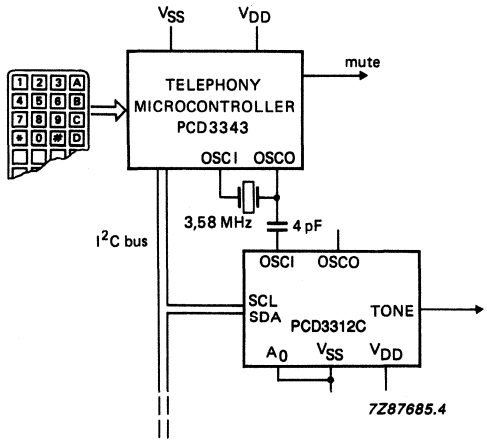
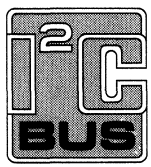


Fig. 24 PCD3312C driven by telephony microcontroller PCD3343 with serial I/O (I^2C-bus).
The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes. The same application is possible with the PCD3311C with MODE = V_{SS}.



Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CMOS MICROCONTROLLER FOR TELEPHONE SETS

GENERAL DESCRIPTION

The PCD3315 is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD33XX family. It has special on-chip features for application in telephone sets. For further detailed information, see PCD33XX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 1536 ROM bytes
- 160 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles
- Clock frequency 100 kHz to 10 MHz
- Single supply voltage from 1,8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3315P: 28-lead DIL; plastic (SOT117).
PCD3315T: 28-lead mini-pack; plastic (SO28; SOT136A).

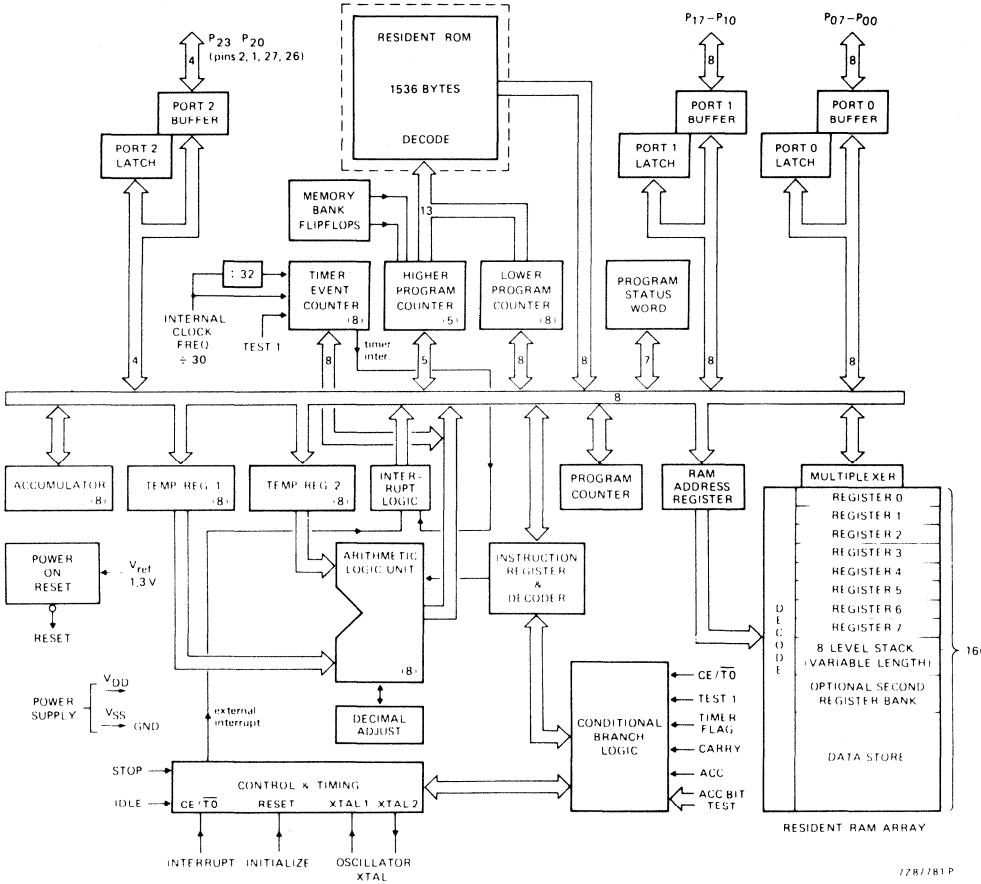
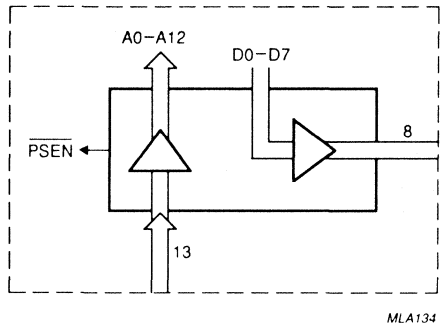


Fig. 1 Block diagram; PCD3315.



(a)

Fig. 1a Replacement of dotted part in Fig. 1, for the PCD3301B 'Piggy-back' version.

PINNING

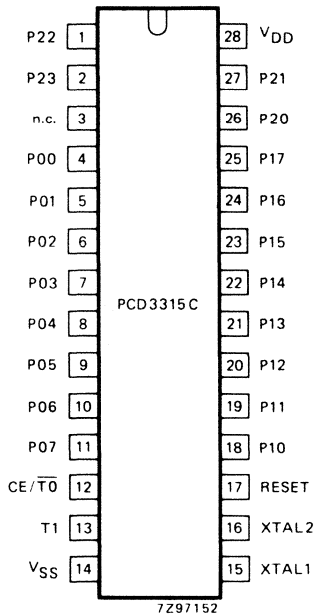


Fig. 2 Pinning diagram: PCD3315.

PIN DESIGNATION

3	n.c.	not connected
4-11	P00-P07	**Port 0**: 8-bit quasi-bidirectional I/O port.
12	CE/$\overline{T0}$	**Interrupt/Test 0**: external interrupt input (sensitive to positive-going edge edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
13	T1	**Test 1**: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
14	V_{SS}	**Ground**: circuit earth potential.
15	XTAL 1	**Crystal input**: connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
16	XTAL 2	connection to the other side of the timing component.
17	RESET	**Reset input**: used to initialize the processor (active HIGH), or output of power-on-reset circuit.
18-25	P10-P17	**Port 1**: 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P20-P23	**Port 2**: 4-bit quasi-bidirectional I/O port.
28	V_{DD}	**Power supply**: 1,8 V to 6 V.

D.C. CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 50 Ω; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating	V_{DD}	1,8	–	6	V
STOP mode for RAM retention	V_{DD}	1,0	–	6	V
Supply current					
operating					
at V_{DD} = 3 V	I_{DD}	–	350	–	μA
IDLE mode					
at V_{DD} = 3 V	I_{DD}	–	150	–	μA
STOP mode (note 1)					
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 1,8 V; T_{amb} = 55 °C	I_{DD}	–	–	5	μA
at V_{DD} = 1,8 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O					
Switching level	V_{RESET}	–	1,2	–	V
Sink current					
at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 3 V; V_O = 0,4 V	I_{OL}	0,6	1,5	–	mA
Pull-up output source current HIGH					
at V_{DD} = 3 V; $V_O = 0{,}9V_{DD}$	$-I_{OH}$	10	–	–	μA
at V_{DD} = 3 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	200	μA
Push-pull output source current HIGH					
at V_{DD} = 3 V; $V_O = V_{DD}$−0,4 V	$-I_{OH}$	0,6	1,5	–	mA

Note 1

Crystal connected between XTAL 1 and XTAL 2; pin 2 pulled to V_{DD} via 5,6 kΩ resistor; CE and T1 at V_{SS}.

PULSE DIALLER CIRCUITS WITH REDIAL

GENERAL DESCRIPTION

The PCD332XC family comprises seven CMOS pulse dialler circuits with redial. Each circuit converts 3 x 4 matrix keyboard entries into correctly-timed line current interruptions. For redial, the last-dialled number (up to 23 digits) is stored in an on-chip RAM. A RAM overflow is handled by inhibiting the redial but manual dialling of more than 23 digits still can be made. The circuits include a delayed reset for line power breaks to ensure correct operation.

Most ICs of the family regenerate an access pause during redial. Insertion of the access pause during the original entry is either automatic or via the '*' key. Termination of the regenerated access pause during redial is via the '#' key, after a built-in delay or controlled by an external tone recognizer. Other differences between the circuits are selections of pulse dialling frequency, mark/space ratio, regenerated access pause duration, mute, hold/access pause output control and oscillator frequency.

Features

- Operating supply voltage range: 2.0 to 6.0 V
- Static supply voltage (with redial memory data retention): down to 1.5 V
- Low operating supply current: typ. 60 μA
- Low static standby supply current: typ. 0.65 μA
- On-chip RAM capacity: 23 keyboard entries (digits and access pauses)
- Redial inhibited after memory overflow
- Manual dialling can continue beyond 23 keyboard entries (excess entries are stored at lower RAM addresses)
- (Re)dialling procedure is not affected by line interruptions shorter than the reset delay time (if the supply voltage does not fall below the static standby voltage)
- Line interruptions longer than the reset delay time are regarded as on-hook situations
- Hold facility for lengthening the inter-digit period
- On-chip oscillator for 3.58 MHz crystal (type for ceramic resonator is also available)
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard
- Pull-up or pull-down circuits at all inputs except CE
- Electrostatic discharge protection at all inputs
- High input noise immunity
- Test mode in which the dialling frequency is increased.

The PCD332XC family of ICs comprises the following types:

PCD3320C dialler with several mute signals
PCD3321C dialler with two automatic access pauses
PCD3322C variant of PCD3320C
PCD3324C dialler with one automatic access pause
PCD3325C dialler with manual access pause control
PCD3326C variant of PCD3321C
PCD3327C variant of PCD3325C for ceramic resonator with automatic reset of access pause

functional survey	PCD . . .						
	3320C	3321C	3322C	3324C	3325C	3326C	3327C
Number of pins	18	18	18	18	18	18	18
Dialling frequency 10 Hz	●	●	●	●	●	●	●
selectable with F01, F02 16, 20 Hz		●		●	●	●	●
Mark/space ratio 3 : 2	●	●	●	●	●	●	●
selectable with M/S 2 : 1		●		●	●		●
Access pauses repeated during redial		●		●	●	●	●
Manual insertion of access pauses		●		●	●	●	●
Automatic access pause insertion							
1 max				●			
2 max		●				●	
Access pause duration 32 x T_{DP}		●		●		●	●
selectable with APD 64 x T_{DP}						●	
not automatically terminated					●		
$\overline{M1}$, inverted mute output	●		●				
M2, strobe output			●				
M3, AND function of mute (M1) and inverted dialling pulse (DP) outputs	●						
HOLD, dialling-interrupt input	●		●				
APO + HOLD, internally connected		●		●	●	●	●

T_{DP} = dialling pulse period

* PCD3327C for ceramic resonator

Features common to all PCD332XC family

OSC IN, OSC OUT: on-chip oscillator input and output
C1 to C3: column keyboard inputs with on-chip pull-up
R1 to R4: row keyboard outputs with on-chip pull-down
CE: chip enable input
DP: dialling pulse output to external line-switching transistor or relay
M1: mute output

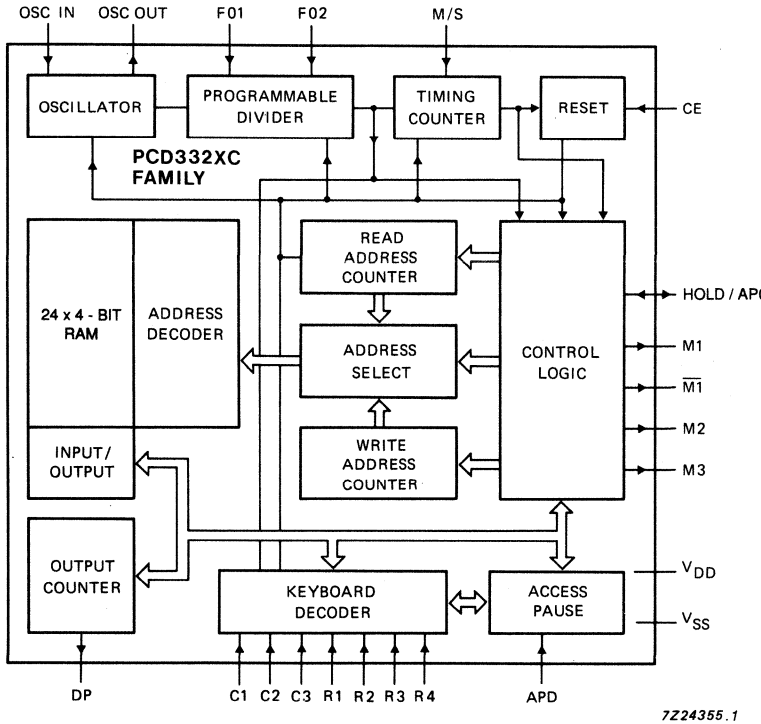


Fig.1 Block diagram.

DEVELOPMENT DATA

PACKAGE OUTLINES

PCD3320CP PCD3321CP PCD3322CP PCD3324CP PCD3325CP PCD3326CP PCD3327CP	18-lead DIL; plastic (SOT102G).
PCD3320CD PCD3321CD	18-lead DIL; ceramic (SOT133B).
PCD3321CT PCD3322CT PCD3327CT	20-lead mini-pack; plastic (SOT163A).
PCD3327U:	uncased chip in tray.

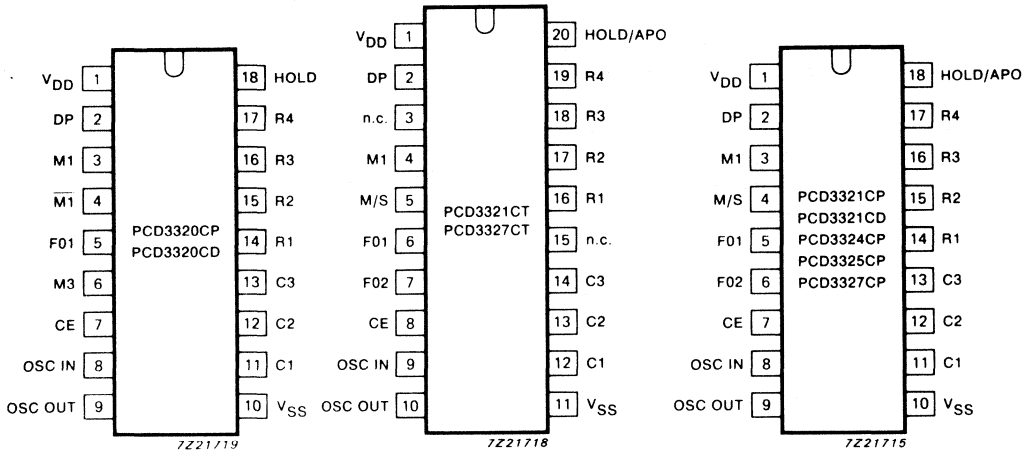
PINNING

pin	purpose	PCD . . .						
		3320C	3321C	3322C	3324C	3325C	3326C	3327C
Supplies								
V_{DD}	positive supply	●	●	●	●	●	●	●
V_{SS}	negative supply	●	●	●	●	●	●	●
Inputs								
M/S	controls mark/space ratio of the line pulses		●		●	●		●
F01	define the dialling pulse frequency	●	●	●	●	●	●	●
F02			●		●	●	●	●
CE	Chip enable: used to initialize the system, to select between operating and static standby mode and to handle line power breaks	●	●	●	●	●	●	●
C1	keyboard column inputs with on-chip pull-up	●	●	●	●	●	●	●
C2								
C3								
ADP	Access Pause Duration: selects the maximum duration of an access pause if no external APR appears						●	
R1	keyboard row outputs with on-chip pull-down	●	●	●	●	●	●	●
R2								
R3								
R4								
HOLD	interrupts dialling after completion of the current digit or immediately during an inter-digit pause	●		●				
Outputs								
DP	Dialling Pulse: drive of the external switching transistor or relay	●	●	●	●	●	●	●
M1	Muting: normally used for muting during the dialling sequence	●	●	●	●	●	●	●
$\overline{M1}$	inverted output of M1	●		●				

pin	purpose	PCD . . .						
		3320C	3321C	3322C	3324C	3325C	3326C	3327C
M2	strobe; HIGH during pulsing of each digit, LOW during an inter-digit pause			●				
M3	AND-function with $\overline{DP}$ and M1 as inputs; for direct drive of a switching transistor for dialling pulses and muting	●						
Oscillator								
OSC IN OSC OUT	input and output of the on-chip oscillator	● ●	● ●	● ●	● ●	● ●	● ●	● ●
Input/outputs								
HOLD/APO	The HOLD and APO features are connected together at this pin, normally an output pin but can be forced as an input		●		●	●	●	●

DEVELOPMENT DATA

PINNING (continued)



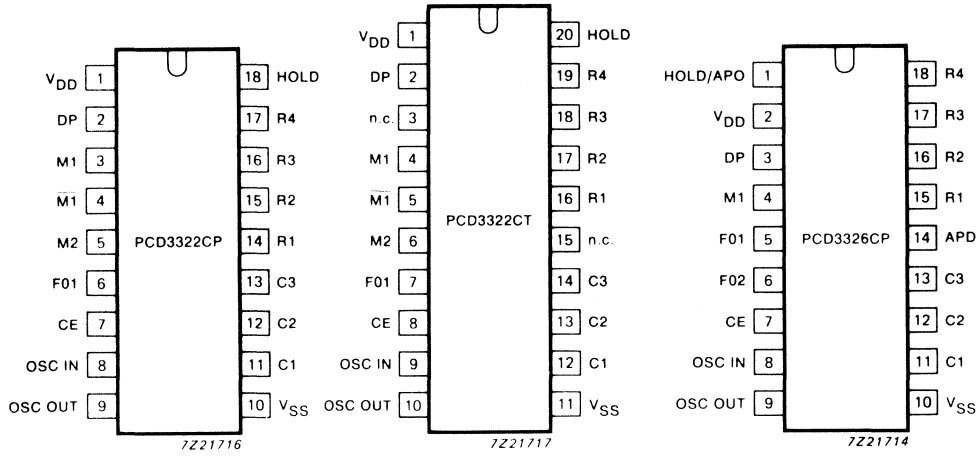


Fig.2 Pinning diagrams.

FUNCTIONAL DESCRIPTION

Clock oscillator (OSC IN, OSC OUT)

The time base for the circuit is a crystal-controlled on-chip oscillator which is completed by the connection of a crystal between the OSC IN and OSC OUT pins (a ceramic resonator may be used with the PCD3327C). Alternatively, the OSC IN pin can be driven by an external clock signal.

Clock divider (F01, F02)

The oscillator is followed by a frequency divider, the division ratio of which can be set externally (F01, F02) to provide one of four chip system clocks, i.e. three 'normal' clock frequencies and one higher frequency for testing.

Other frequencies can also be obtained by driving OSC IN, as previously stated.

Chip enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped at reset, excepting the WRITE ADDRESS COUNTER (WAC). The keyboard input is prohibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

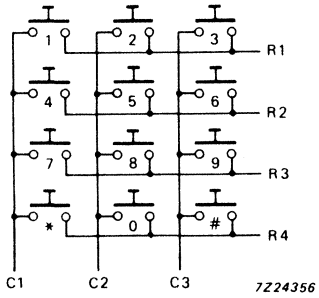
Debouncing keyboard entries (C1 to C3; R1 to R4)

The column keyboard inputs to the integrated circuits(Cn) and the row keyboard outputs (Rn) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig.3, or to a double contact keyboard with a common left open contact (see Fig.4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input. Any other input combinations are not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig.5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for five or six clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been left open for four or five clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the leading edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 codes are written into the RAM, memory overflow results and the access keycodes replace the data in the lower-numbered locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly-timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset (see 'Access Pause System'). During redial, no keyboard entry will be accepted and stored in the RAM. But, when all numbers stored in the RAM have been pulsed out, new keyboard entries will be accepted and stored in the RAM position after the last digit code of the original entry and converted into correctly-timed dialling pulses.



* Access pause set.
\# Redial or access pause reset.

Fig.3 Single contact keyboard.

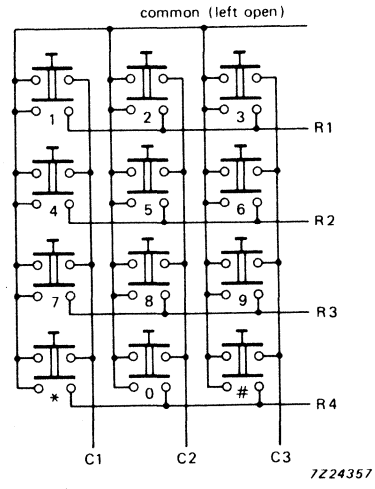


Fig.4 Double contact keyboard.

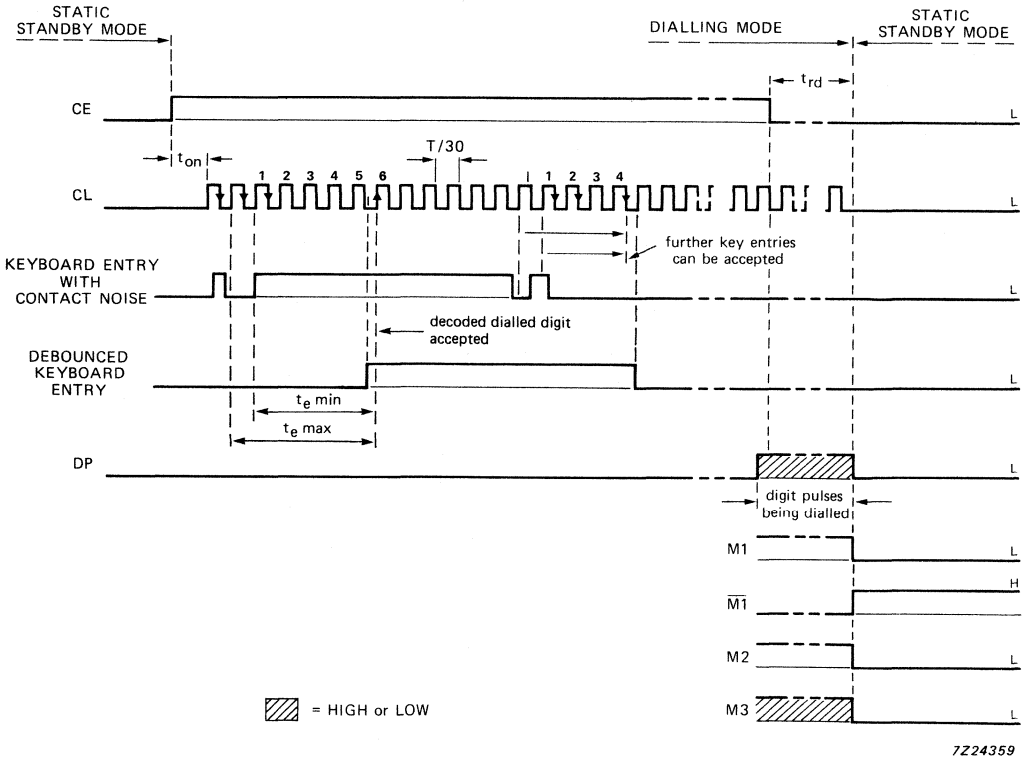


Fig.5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig.6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and ten clock pulse periods later a prepulse with a duration of ten clock pulse periods (t_d) appears at outputs M1 and M3. This prepulse ensures that if a polarized muting relay with two stable positions is used it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

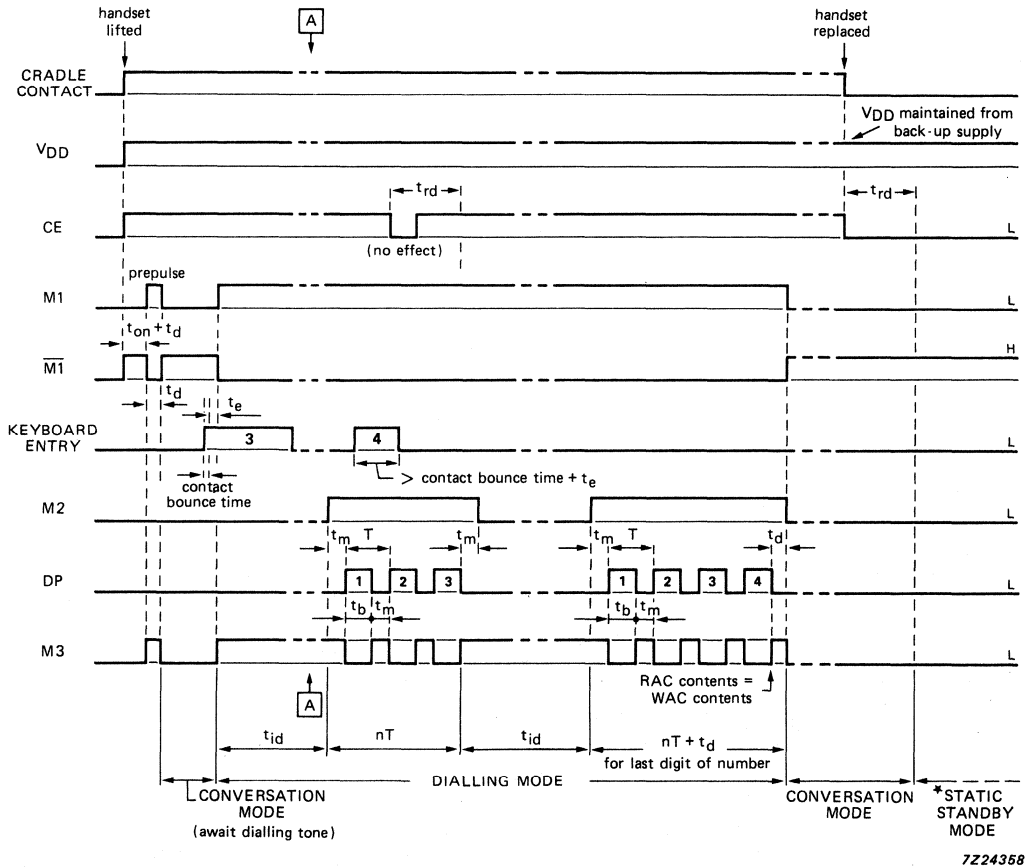
- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (see Fig.7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes high, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

DEVELOPMENT DATA

Dialling sequence (continued)

Referring to Fig.6, when the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH, the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at outputs DP and M3. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1.6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above the level V_{DD0} = 1.5 V, which is detected by the power-on reset circuit.



* Oscillator off; all registers reset; keyboard input inhibited; number stored in RAM until $V_{DD} < 1.5$ V.

Fig.6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts).

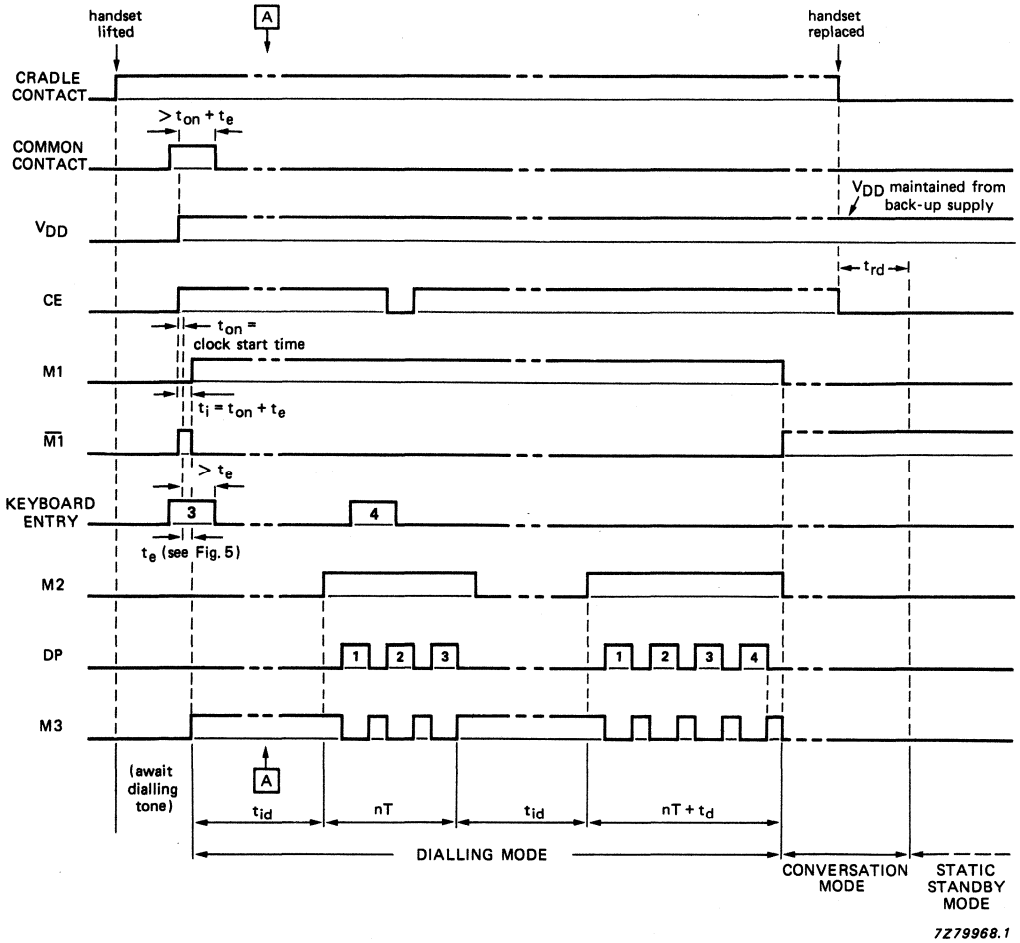


Fig.7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig.6 for pulse timings after point A.

Hold function (HOLD)

As shown in Fig.8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM to be converted into dialling pulses on M3 and DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

HOLD can be controlled by the Access Pause Output (see section "Access pause system).

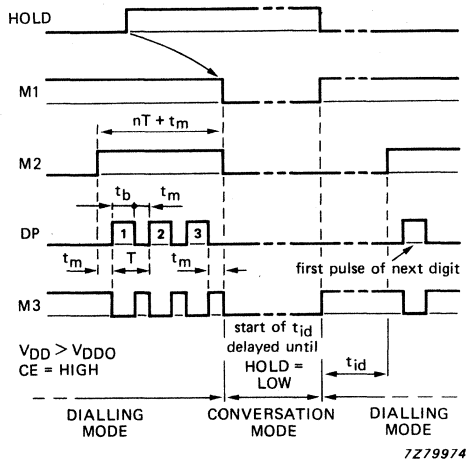


Fig.8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses.

Access pause system (HOLD/APO)

The PCD3320C and PCD3322C only have the HOLD input and therefore these devices cannot reproduce the access pauses during redial (the access pause system is disabled). In all the other devices the HOLD input is internally connected to the APO output. This pin (HOLD/APO) can be used as an output, or forced as an input (e.g. by an external tone recognizer). Access pauses can be stored at appropriate positions in the RAM during the original entry of a number. As soon as the access pause code is read from the RAM, the access pause output (HOLD/APO) goes HIGH and dialling is interrupted.

DEVELOPMENT DATA

Storing access pauses during dialling

Access pauses can be stored by one or both of the following ways:

- Manually by pressing the access pause key (*). The number of access pauses that can be stored in this way is limited only by the capacity of the RAM (digits + access pauses $\leqslant 23$).
- In some ICs of the family an access pause is stored automatically in the RAM (see Fig.9) during the original entry after all the digits so far entered have been transmitted (when M1 goes LOW, see Fig.6). The maximum number of access pause codes that can be entered in this manner is either one or two, depending on the type of IC.

Note: that when access pauses are manually inserted into ICs with automatic insertion of access pauses, the circuit automatically adds an access pause code after the number. This increases the RAM digit-count by one and reduces the maximum number of digits to 22 (including actual access pauses). The same would happen if the maximum number of access pauses for automatic entry is not reached before the end of the number.

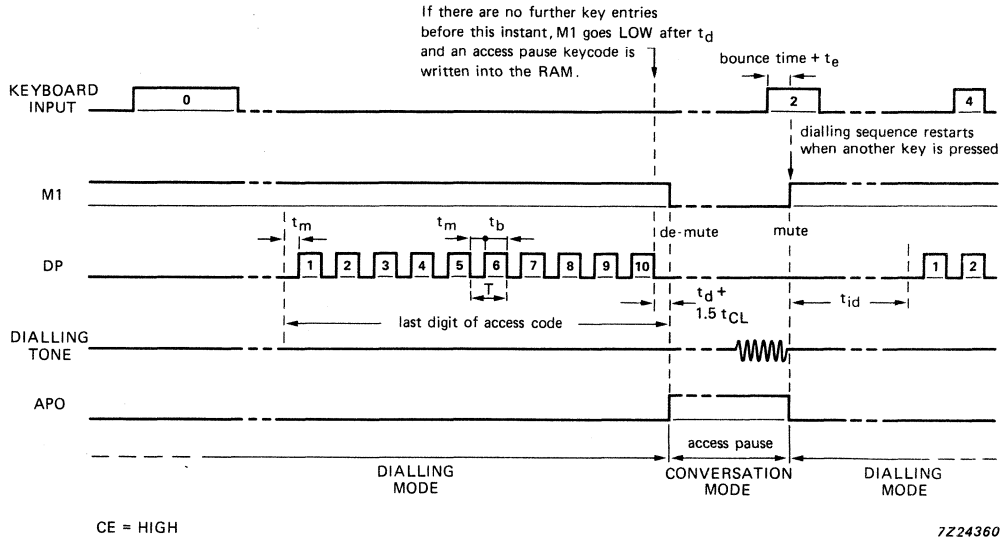


Fig.9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Terminating access pauses during redial (APD)

If APO is connected to HOLD, there are three ways of terminating access pauses during redial (see Fig.10):

- Manually by pressing the redial key before t_{ap} expires.
- Automatically if the built-in time t_{ap} expires; APO, and also HOLD, then go LOW so that the next digit will be dialled. With the Access Pause Delay (APD) select input, t_{ap} can be set to one of two values. With ICs that do not terminate access pauses in this way, t_{ap} is virtually infinity.
- By forcing HOLD/APO LOW (e.g. with an external tone recognizer).

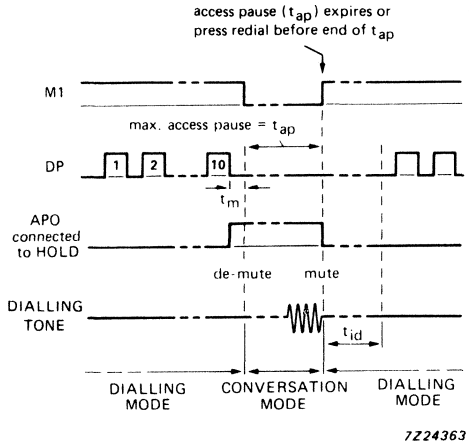
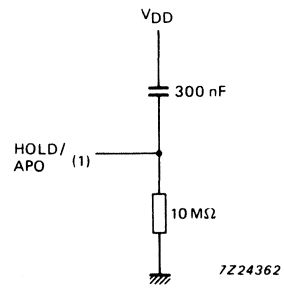


Fig.10 Timing diagram showing access pause reset.

For types with automatic reset of the access pause it is possible to lengthen the access pulse duration with external components (see Fig.11).



(1) $\Delta t_{ap} \approx 2$ s.

Fig.11 External circuit required to lengthen the access pause for ICs with automatic reset of the access pause.

FAMILY RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	−0.5	8.0	V
Voltage on any pin		V_I	V_{SS}−0.3	V_{DD} + 0.3	V
Operating ambient temperature range		T_{amb}	−25	+ 70	°C
Storage temperature ramge		T_{stg}	−55	+ 125	°C

FAMILY CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters f_{osc} = 3.58 MHz and R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage	T_{amb} = −25 to + 70 °C	V_{DD}	2.0	3.0	6.0	V
Standby supply voltage (note 1)	T_{amb} = −25 to + 70 °C	V_{DDO}	1.5	–	6.0	V
Operating supply current	CE = V_{DD}; notes 2 and 3	I_{DD}	–	60	120	μA
	V_{DD} = 6 V; CE = V_{DD}; notes 2 and 3	I_{DD}	–	200	400	μA
Standby supply current	CE = V_{SS}; note 2	I_{DDO}	–	0.65	2.0	μA
	V_{DD} = 1.8 V; T_{amb} = −25 to + 70 °C	I_{DDO}	–	–	2	μA
Input voltage LOW	1.8 V ⩽ V_{DD} ⩽ 6 V	V_{IL}	–	–	0.3 x V_{DD}	V
Input voltage HIGH	1.8 V ⩽ V_{DD} ⩽ 6 V	V_{IH}	0.7 x V_{DD}	–	–	V
CE input leakage current						
LOW	CE = V_{SS}	$-I_{IL}$	–	–	50	nA
HIGH	CE = V_{DD}	I_{IH}	–	–	50	nA
M/S pull-up input current	V_I = V_{SS}	$-I_{IL}$	30	100	300	nA
F01, F02, HOLD/APO APD pull-down input current	V_I = V_{DD}	I_{IH}	30	100	300	nA
Matrix keyboard operation						
Keyboard current	Cn connected to Rn; CE = HIGH	I_K	–	30	–	μA
Keyboard 'ON' resistance	contact 'ON'; note 4	R_{KON}	–	–	2	kΩ
Keyboard 'OFF' resistance	contact 'OFF'; note 4	R_{KOFF}	1	–	–	MΩ

DEVELOPMENT DATA

FAMILY CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Matrix keyboard operation (continued)						
Outputs R_1 to R_4						
sink current		I_O	–	3	–	mA
source current		$-I_O$	–	40	–	μA
Outputs M1, $\overline{M1}$, M2, M3, DP						
sink current	V_{OL} = 0.5 V	I_{OL}	0.7	2.0	4.0	mA
source current	V_{OH} = 2.5 V	$-I_{OH}$	0.65	1.8	3.6	mA
Outputs HOLD/APO						
source current	V_{OH} = 2.5 V	$-I_{OH}$	0.7	2.0	4.0	mA

Notes to family characteristics

1. V_{DDO} = 1.5 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between OSC IN and OSC OUT pins < 3 pF.
4. Guarantees correct keyboard operation.

FAMILY TIMING DATA

V_{DD} = 3 V; V_{SS} = 0 V; f_{osc} = 3.58 MHz

parameter	conditions	symbol	min.	typ.	max.	unit
Clock start-up time	CE: from V_{SS} to V_{DD} note 1	t_{on}	–	4	–	ms

Note to family timing data

1. Stray capacitance between OSC IN and OSC OUT < 3 pF.

DEVELOPMENT DATA

FAMILY CURVES

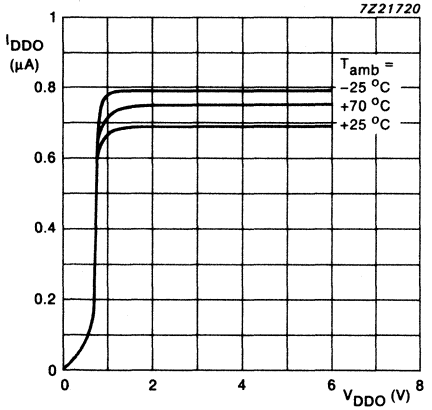


Fig.12 Standby supply current as a function of standby supply voltage.

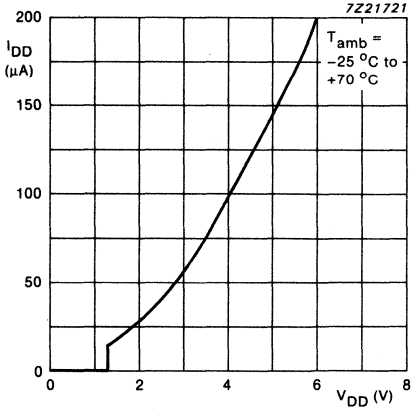


Fig.13 Operating supply as a function of operating supply voltage.

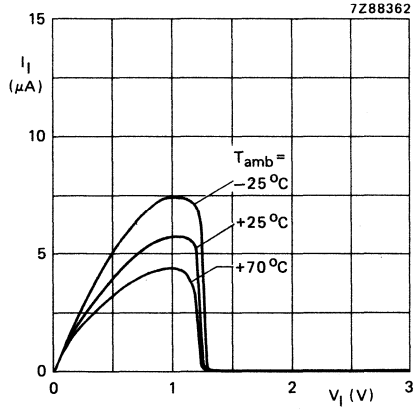


Fig.14 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

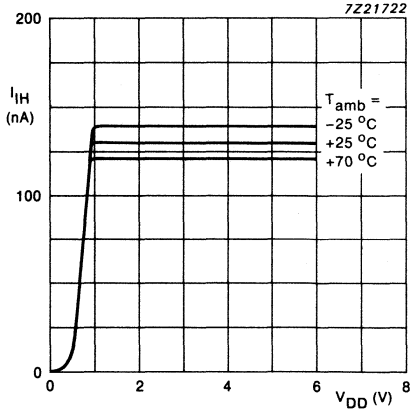


Fig.15 Pull-down input current as a function of supply voltage, $V_I = V_{DD}$.

FAMILY CURVES (continued)

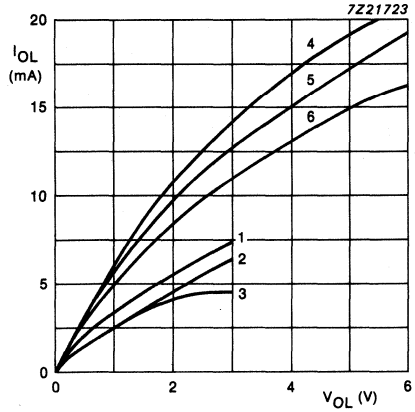


Fig.16 Output (N-channel) sink characteristics for M1, $\overline{M1}$, M2, M3 and DP.

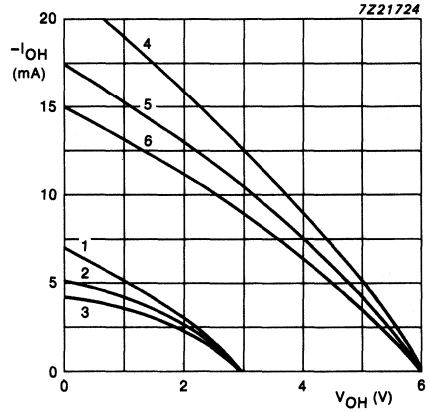


Fig.17 Output (P-channel) source characteristics for M1, $\overline{M1}$, M2, M3 and DP.

Key to Figs 16 and 17

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	curve 1	curve 4
+25 °C	curve 2	curve 5
+70 °C	curve 3	curve 6

CHARACTERISTICS PER TYPE

PCD3320C specification

Inputs that are not available are defined internally as follows:
F02 = APD = LOW and M/S = HIGH

Outputs not available are M2 and APO.

Features additional to the common family specification are:

$\overline{M1}$	inverted mute output
M3	AND-function of mute (M1) and inverted dialling pulse (DP) outputs
HOLD	input that interrupts dialling

Redial of the last entered number is possible up to 23 digits; access pauses are not generated. Mark/space ratio is 3:2.

Using the F01 input it is possible to select either normal mode (F01 = LOW) or test mode (F01 = HIGH). In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

PCD3320C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.58 MHz

parameter	conditions	symbol	FO1 = LOW (dialling)	unit
Dialling pulse frequency	note 1	f_{DP}	10.13	Hz
Dialling pulse period; $1/f_{DP}$	see Fig. 6 and 7	T_{DP}	98.7	ms
Clock pulse frequency; $30 \times f_{DP}$		f_{CLK}	303.9	Hz
Break time; $3/5 \times T_{DP}$	see Fig. 6	t_b	59.2	ms
Make time; $2/5 \times T_{DP}$	see Fig. 6	t_m	39.5	ms
Inter-digit pause; $8 \times T_{DP}$	see Figs 6 and 7	t_{id}	790	ms
Reset delay time; $1.6 \times T_{DP}$	see Figs 5, 6 and 7	t_{rd}	158	ms
Prepulse duration; $1/3 \times T_{DP}$	see Figs 6 and 7	t_d	33	ms
Debounce time;				
min. $5/30 \times T_{DP}$	see Fig. 5	$t_{e\,min}$	16.45	ms
max. $6/30 \times T_{DP}$	see Fig. 5	$t_{e\,max}$	19.74	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22	ms

DEVELOPMENT DATA

Note to the PCD3320C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.

CHARACTERISTICS PER TYPE (continued)

PCD3321C specification

The PCD3321C is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for Private Automatic Branch Exchange (PABX) systems. Two access pauses can be stored automatically during the original entry of a number, or several made via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are defined internally as follows:

APD = LOW

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02 — inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

HOLD/APO — input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)

M/S — input for M/S ratio selection to 3:2 or 2:1

PCD3321C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10.13	15.54	19.42	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	98.7	64.4	51.5	ms
Clock pulse frequency; 30 x f_{DP}		f_{CL}	303.9	466.1	582.6	Hz
Break time; 3/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_b	59.2	38.6	30.9	ms
Make time; 2/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_m	39.5	25.8	20.6	ms
Break time; 2/3 x T_{DP}	M/S = LOW note 4	t_b	65.8	42.9	34.3	ms
Make time; 1/3 x T_{DP}	M/S = LOW note 4	t_m	32.9	21.5	17.2	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	790	515	412	ms
Reset delay time; 1.6 x T_{DP}		t_{rd}	158	103	82.4	ms
Access pause time; 32 x T_{DP}-t_m-$1/f_{CL}$		t_{ap}	3.12	2.03	1.63	s

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Prepulse duration; 1/3 x T_{DP}		t_d	33.0	21.5	17.2	ms
Debounce time; min. 5/30 x T_{DP}		$t_{e\ min}$	16.45	10.70	8.58	ms
max. 6/30 x T_{DP}		$t_{e\ max}$	19.74	12.88	10.30	ms
Initial data time (typ.); $t_{on} + t_e$		t_i	22.0	16.0	13.5	ms

Notes to the PCD3321C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

DEVELOPMENT DATA

CHARACTERISTICS PER TYPE (continued)

PCD3322C specification

Inputs that are not available are defined internally as follows:

F02 = APD = LOW and M/S = HIGH

Outputs not available are M3 and APO.

Features additional to the common family specification are:

$\overline{M1}$	inverted mute output
M2	strobe; HIGH during pulsing of a digit, LOW during an inter-digit pause
HOLD	input that interrupts dialling

Redial of the last entered number is possible up to 23 digits; access pauses are not generated. Mark/space ratio is 3:2.

Using the F01 input it is possible to select either normal mode (F01 = LOW) or test mode (F01 = HIGH). In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

PCD3322C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.58 MHz

parameter	conditions	symbol	F01 = LOW (dialling)	unit
Dialling pulse frequency	note 1	f_{DP}	10.13	Hz
Dialling pulse period; $1/f_{DP}$	see Figs 6 and 7	T_{DP}	98.7	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	303.9	Hz
Break time; 3/5 x T_{DP}	see Fig.6	t_b	59.2	ms
Make time; 2/5 x T_{DP}	see Fig. 6	t_m	39.5	ms
Inter-digit pause; 8 x T_{DP}	see Figs 6 and 7	t_{id}	790	ms
Reset delay time; 1.6 x T_{DP}	see Figs 5,6 and 7	t_{rd}	158	ms
Prepulse duration; 1/3 x T_{DP}	see Figs 6 and 7	t_d	33	ms
Debounce time;				
min. 5/30 x T_{DP}	see Fig. 5	$t_{e\ min}$	16.45	ms
max. 6/30 x T_{DP}	see Fig. 5	$t_{e\ max}$	19.74	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22	ms

Note to the PCD3322C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.

PCD3324C specification

The PCD3324C is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for PABX systems. One access pause can be stored automatically during the original entry of a number, or several made via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

APD = LOW

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.
HOLD/APO	input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)
M/S	input for M/S ratio selection to 3:2 or 2:1.

DEVELOPMENT DATA

CHARACTERISTICS PER TYPE (continued)

PCD3324C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency $1/T_{DP}$	note 1	f_{DP}	10.13	15.54	19.42	Hz
Dialling pulse period: $1/f_{DP}$		T_{DP}	98.7	64.4	51.5	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	303.9	466.1	582.6	Hz
Break time; 3/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_b	59.2	38.6	30.9	ms
Make time; 2/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_m	39.5	25.8	20.6	ms
Break time; 2/3 x T_{DP}	M/S = LOW note 4	t_b	65.8	42.9	34.3	ms
Make time; 1/3 x T_{DP}	M/S = LOW note 4	t_m	32.9	21.5	17.2	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	790	515	412	ms
Reset delay time ; 1.6 x T_{DP}		t_{rd}	158	103	82.4	ms
Access pause time; 32 T_{DP}-t_m-$1/f_{CL}$		t_{ap}	3.12	2.03	1.63	s
Prepulse duration; 1/3 x T_{DP}		t_d	33.0	21.5	17.2	ms
Debounce time; min. 5/30 x T_{DP}		$t_{e\ min}$	16.45	10.70	8.58	ms
max. 6/30 x T_{DP}		$t_{e\ max}$	19.74	12.88	10.30	ms
Initial data entry time (typ.) $t_{on} + t_e$		t_i	22.0	16.0	13.5	ms

Notes to the PCD3324C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

PCD3325C specification

The PCD3325C is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for PABX systems. Access pauses can be stored via the keyboard during the original entry of a number (there is no automatic storage of access pauses). The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either via the keyboard or with an external dial tone recognizer.

Inputs that are not available are defined internally as follows:

APD = LOW

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.
HOLD/APO	input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected).
M/S	input for M/S ratio selection to 3:2 or 2:1.

CHARACTERISTICS PER TYPE (continued)

PCD3325C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10.13	15.54	19.42	Hz
Dialling pulse perid; $1/f_{DP}$		T_{DP}	98.7	64.4	51.5	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	303.9	466.1	582.6	Hz
Break time; 3/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_b	59.2	38.6	30.9	ms
Make time; 2/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_m	39.5	25.8	20.6	ms
Break time; 2/3 x T_{DP}	M/S = LOW note 4	t_b	65.8	42.9	34.3	ms
Make time; 1/3 x T_{DP}	M/S = LOW note 4	t_m	32.9	21.5	17.2	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	790	515	412	ms
Reset delay time; 1.6 x T_{DP}		t_{rd}	158	103	82.4	ms
Prepulse duration; 1/3 x T_{DP}		t_d	33.0	21.5	17.2	ms
Debounce time min. 5/30 x T_{DP}		$t_{e\ min}$	16.45	10.70	8.58	ms
max. 6/30 x T_{DP}		$t_{e\ max}$	19.74	12.88	10.30	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22.0	16.0	13.5	ms

DEVELOPMENT DATA

Notes to the PCD3325C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

PCD3326C specification

The PCD3326C includes many additional features that make it ideal for PABX systems. Two access pauses can be stored automatically during the original entry of a number, or several stored via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

M/S = HIGH

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.
HOLD/APO	input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)
APD	input for selecting access pause duration.

CHARACTERISTICS PER TYPE (continued)

PCD3326C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10.13	15.54	19.42	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	98.7	64.4	51.5	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	303.9	466.1	582.6	Hz
Break time; 3/5 x T_{DP}	note 2	t_b	59.2	38.6	30.9	ms
Make time; 2/5 x T_{DP}	note 2	t_m	39.5	25.8	20.6	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	790	515	412	ms
Reset delay time; 1.6 x T_{DP}		t_{rd}	158	103	82.4	ms
Access pause time	APD = LOW;					
32 x T_{DP}-t_m-$1/f_{CL}$	or n.c.; note 3	t_{ap}	3.12	2.03	1.63	s
64 x T_{DP}-t_m-$1/f_{CL}$	APD = HIGH	t_{ap}	6.28	4.09	3.28	s
Prepulse duration; 1/3 x T_{DP}		t_d	33.0	21.5	17.2	ms
Debounce time;						
min. 5/30 x T_{DP}		$t_{e\ min}$	16.45	10.70	8.58	ms
max. 6/30 x T_{DP}		$t_{e\ max}$	19.74	12.88	10.33	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22.0	16.0	13.5	ms

Notes to the PCD3326C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.
2. Mark/space ratio = 3:2.
3. In the n.c. (not connected) condition, the input is drawn to the LOW state by the internal pull-down current.

PCD3327C specification

The PCD3327C contains an oscillator with sufficient gain to provide oscillation when using an inexpensive 455 kHz ceramic resonator. Two additional capacitors are required as shown in Fig.18. Alternatively, the OSC IN pin may be driven from an external 455 kHz clock signal.

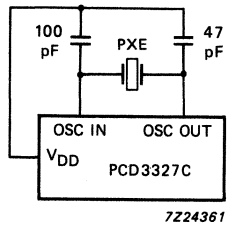


Fig.18 PCF3327 oscillator circuit.

This IC is pin-compatible with the DF320 and MT4320 types and includes additional features that make it ideal for PABX systems. The circuit allows several access pauses to be stored via the keyboard and regenerates the access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

APD = LOW

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02 — inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

HOLD/APO — input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected).

M/S — input for M/S ratio selection to 3:2 or 2:1.

DEVELOPMENT DATA

CHARACTERISTICS PER TYPE (continued)

PCD3327C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 455 kHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10.3	15.8	19.7	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	97	63	51	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	309	474	592	Hz
Break time; 3/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_b	58	38	30	ms
Make time; 2/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_m	39	25	20	ms
Break time; 2/3 x T_{DP}	M/S = LOW note 4	t_b	65	42	34	ms
Make time; 1/3 x T_{DP}	M/S = LOW note 4	t_m	32	21	17	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	776	506	405	ms
Reset delay time; 1.6 x T_{DP}		t_{rd}	155	101	81	ms
Access pause time; 32 x T_{DP}-t_m-$1/f_{CL}$		t_{ap}	3.12	2.03	1.63	s
Prepulse duration; 1/3 x T_{DP}		t_d	32	21	17	ms
Debounce time; min. 5/30 x T_{DP}		$t_{e\ min}$	16.18	10.54	8.45	ms
max. 6/30 x T_{DP}		$t_{e\ max}$	19.41	12.66	10.13	ms
Initial data entry time (typ.); t_{on} + t_e		t_i	22.0	16.0	13.5	ms

Notes to the PCD3327C timing data

1. f_{DP} is 10 Hz when a 441.6 PXE ceramic resonator is used.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

CMOS REPERTORY DIALLER TELEPHONE SET CONTROLLER

GENERAL DESCRIPTION

The PCD3341 is a low threshold voltage IC fabricated in CMOS. It is designed to control display, redial and repertory dialling in a telephone set. The IC has two dialling modes; pulse dialling (PD) and dual tone multi-frequency (DTMF). The architecture of the PCD3341 is identical to that of the PCD3343. It comprises an 8-bit CPU, 224 RAM bytes and 3K ROM bytes (the ROM is already programmed).
The operating supply voltage is 2,5 to 6,0 V with a low current consumption in all operating modes: standby, conversation and dialling modes.
Up to 18 digits and 2 manual access pauses can be stored for redial, extended redial and direct dial purposes together with on-chip storage for 10 repertory numbers.
For expansion of the system the PCD3341 provides a two wire serial input/output port, in accordance with the I^2C bus specifications, to control the DTMF tone generator, LCD drivers and additional RAMs for additional repertory numbers.

Features

- Pulse dialling
- DTMF dial control of tone generator PCD3312
- Redial
- Extended redial
- Electronic notepad
- Direct dialling (emergency call)
- On-chip storage for 10 repertory dial numbers
- 18-digit capacity for each autodial memory
- Flash or register recall
- Access pause generation and termination
- Manual reset of autodial RAM
- On-chip power-on reset
- Programmed for improved noise immunity
- Extention possible with external RAM for up to 110 repertory dial numbers
- Uses standard 4 x 4 keyboard (single or double contact)
- Additional 10-digits first in first out memory, for infinite long numbers control an LCD via the I^2C bus.
- Four extra function keys: program/autodial, flash, redial, access pause
- Keyboard expansion possible for 10 separated repertory dialled numbers
- Automatic recognition of PABX-digits; resulting in an access pause insertion
- Hold input and access pause output (APO) to adjust the duration of the access pause and facilitate use of tone recognizers
- Six diode or strap functions: mark-to-space ratio, tone burst time, inter-digit pause time, access pause time, normal or expanded keyboard, normal or direct dialling

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DD}	min. 1,8	V
Operating currents at V_{DD} = 3 V			
conversation mode	I_{DDC}	typ. 270	μA
dialling mode	I_{DDD}	typ. 600	μA
Standby supply current at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	typ. 1,2	μA
Crystal frequency	f	3,58	MHz
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINES

PCD3341P: 28-lead DIL; plastic (SOT117).
PCD3341T: 28-lead mini-pack; plastic (SO28; SOT136A).

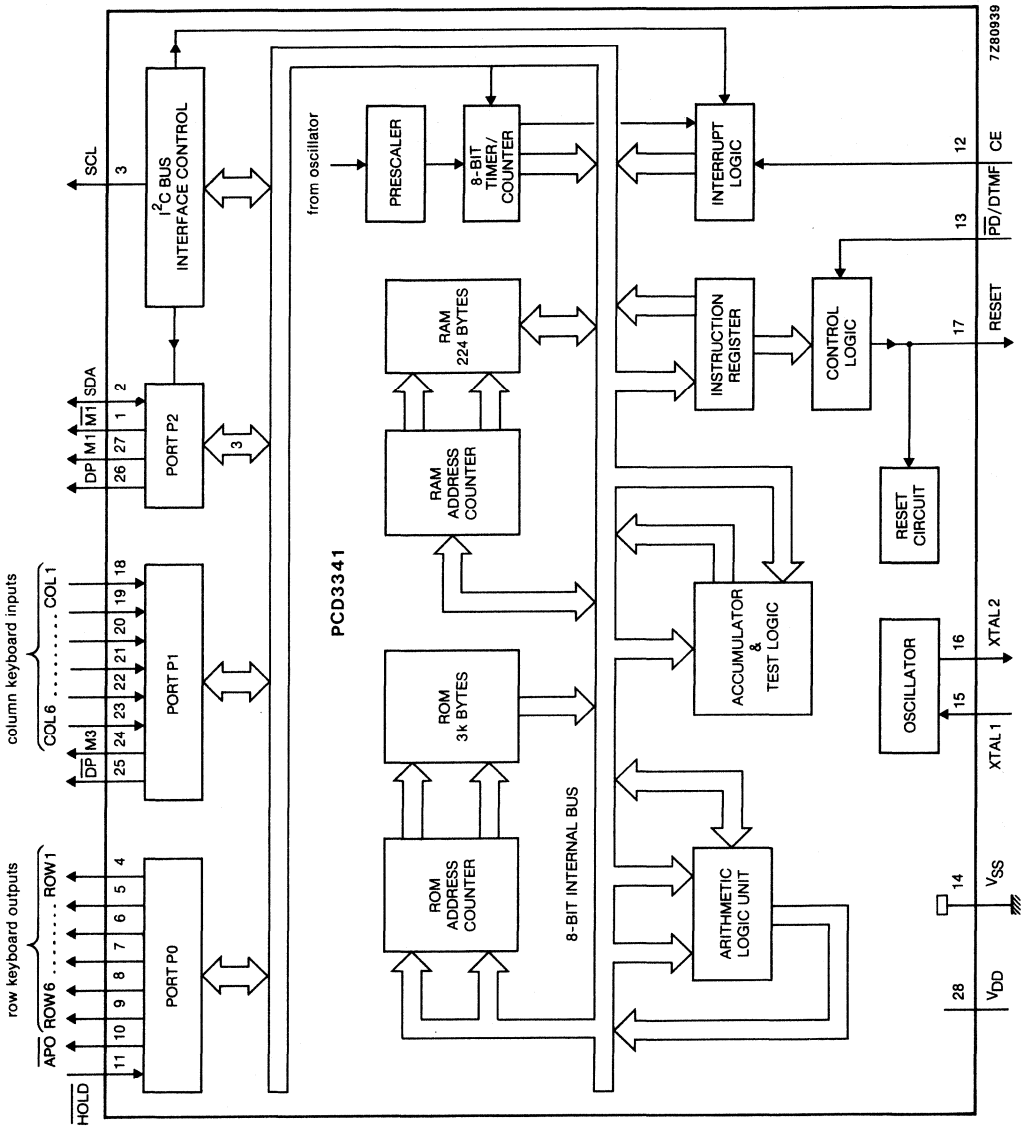


Fig. 1 Block diagram.

DEVELOPMENT DATA

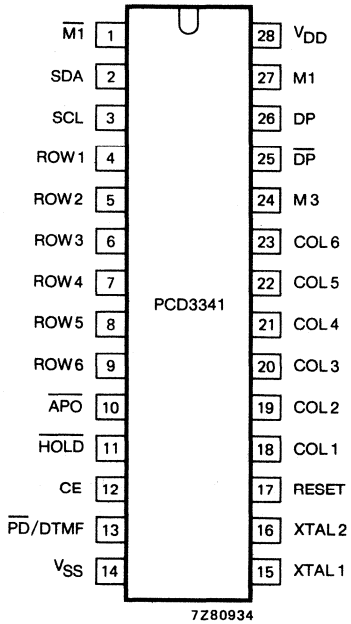


Fig. 2 Pinning diagram.

PINNING

1	$\overline{M1}$	inverted output of M1
2	SDA	serial data
3	SCL	serial clock
4	ROW 1	scanning row keyboard outputs
5	ROW 2	
6	ROW 3	
7	ROW 4	
8	ROW 5	
9	ROW 6	
10	$\overline{APO}$	access pause output
11	$\overline{HOLD}$	hold input
12	CE	chip enable input
13	$\overline{PD}$/DTMF	input to select pulse or DTMF dialling
14	V_{SS}	negative supply
15	XTAL 1	input to on-chip oscillator
16	XTAL 2	output from on-chip oscillator
17	RESET	reset input/output
18	COL 1	sense column keyboard inputs
19	COL 2	
20	COL 3	
21	COL 4	
22	COL 5	
23	COL 6	
24	M3	muting output
25	$\overline{DP}$	inverted pulse dialling output
26	DP	pulse dialling output
27	M1	muting output
28	V_{DD}	positive supply

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

Power supply must be retained for data storage.

Clock oscillator (XATL 1; XTAL 2)

The time base for the PCD3341 is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between XTAL 1 and XTAL 2. The oscillator starts when V_{DD} reaches the operating voltage level and CE = HIGH. The output XTAL 2 can be used to drive the oscillator input of the PCD3312.

Chip Enable (CE)

This active HIGH input is used to initialize part of the system, to select the operational or standby mode and to handle line power breaks.

Pulse dialling outputs (DP; $\overline{DP}$)

DP output drives an external switching transistor or relay in pulse dialling mode. This output is also used to pulse out a calibrated FLASH pulse (recall register) of 90 ms duration as soon as the keyboard input FLASH is activated by depressing the key F. The FLASH function acts like CE with respect to redial.

Muting outputs (M1; $\overline{M1}$; M3)

M1 output is used for muting during the dialling sequence. For pulse dialling M1 goes HIGH with the first inter-digit pause and remains active for 33 or 40 ms (mark-to-space selection) following the last break pulse after the last digit held in store has been transmitted. In DTMF dialling, input $\overline{PD}$/DTMF is HIGH. M1 is HIGH as long as two out of the eight frequency signals are sent, then remains HIGH for an additional 80 ms (hold-over time).
$\overline{M1}$ output is the inverted output of M1.
M3 output is an AND function with $\overline{DP}$ and M1 as input, used for direct drive of a switching transistor for dialling pulses and muting.

Hold input ($\overline{HOLD}$); **access pause output** ($\overline{APO}$)

The hold input suspends dialling after completion of the current digit, or in pulse dialling during an inter-digit pause.
The hold function facilitates an extra time delay during dialling under control of external circuits (dialling tone recognizer). In the hold state ($\overline{HOLD}$ = LOW) the muting output is also LOW, thus the IC is in the conversation mode. The $\overline{HOLD}$ input can be controlled by the access pause output (APO) directly or indirectly via a dialling tone recognizer (see Fig. 3). The tone recognizer automatically terminates access pauses upon receipt of the access tone, regardless of whether this occurs during or after the access pause time (t_{ap}). The $\overline{APO}$ output will go LOW when an access pause is recognized.

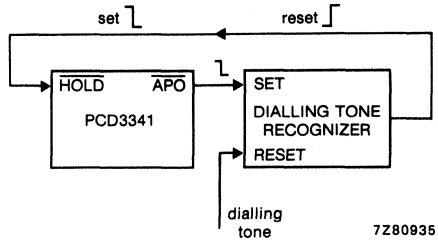


Fig. 3 Automatic variation of length of an access pause under control of a dialling tone recognizer.

Serial data (SDA); **serial clock** (see Fig. 8)

The serial I/O lines SDA and SCL are used to control the PCD3312 in the DTMF dialling mode, additional RAMs (PCD8570) for repertory dialling and LCD drivers (PCF8577). Both outputs require external pull-up resistors.

Keyboard inputs/outputs (COL 1 to 6; ROW 1 to 6)

The sense column inputs COL 1 to COL 6 and the scanning row outputs ROW 1 to ROW 6 are directly connected to a 4 x 4 single contact keyboard matrix. The keyboard organization is shown in Fig. 4.
In pulse dialling mode the valid keys are the 10 numeric keys (0 to 9). The 6 non-numeric keys (A, B, C, D, *, #) have no effect on the dialling.
In DTMF dialling mode the 10 numeric keys and the 6 non-numeric keys are valid. On-chip repertory dialling uses the 10 numeric numbers (no external RAM).
With extended repertory dialling 10 extra keys (M1 to M10) are used (on-chip or external RAM).
Row 5 of the keyboard contains the following special function keys:

- P memory clear and programming (notepad)
- FL flash or register recall
- R redial
- AP manual access pause entry

Diode options (ROW 6)

Row 6 is added to the keyboard matrix to provide the following selections:

Mark-to-space ratio (M/S)
OFF M/S 3:2
ON M/S 2:1

Tone burst time (t_{tb})
OFF t_{tb} = 70 ms
ON t_{tb} = 100 ms

Inter-digit pause (IDP)
OFF IDP = 900 ms
ON IDP = 500 ms

Access pause time (t_{ap})
OFF t_{ap} = 1,5 s (DTMF); 3 s (PD)
ON t_{ap} = 2,5 s (DTMF); 5 s (PD)

Keyboard expansion (EKB)
OFF normal keyboard
ON expanded keyboard

Normal/direct call (N/D)
OFF normal call mode
ON direct call (emergency)

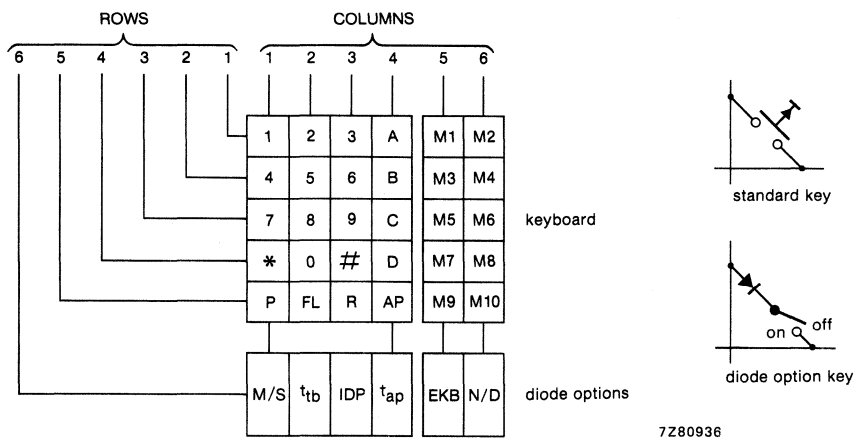


Fig. 4 Keyboard organization.

FUNCTIONAL DESCRIPTION (continued)

Dialling mode selection input ($\overline{PD}$/DTMF)

This input selects the dialling mode:

- $\overline{PD}$/DTMF = LOW selects pulse dialling
- $\overline{PD}$/DTMF = HIGH selects DTMF dialling

Reset input/output (RESET)

When the reset input is active HIGH it can be used to initialize the IC.
In normal application this is achieved by the CE input.
Reset is also an output of the internal power-on-reset circuit, which generates a reset pulse if V_{DD} drops below 1,3 V (typ.).

OPERATION

The PCD3341 has 3 operating modes:

- Standby
- Conversation
- Dialling

Standby mode

When the chip enable input (CE) is LOW the IC is disabled. In the standby mode the only current drawn is from a back up supply (battery or line powered), for memory retention, holding up to 13 call numbers for repertory and redialling.

Conversation mode

After the handset is lifted CE is activated and V_{DD} rises to the working voltage. M1 muting is inactive and speech or dial tone can be heard. With the oscillator operating the chip is ready to accept keyboard entries. Current consumption is $< 300\ \mu A$.

Dialling mode

The dialling mode starts with first valid keyboard entry when it initiates:

- a normal call of a newly dialled number
  or
- a repertory or redialling cycle of previously entered and stored numbers

The current consumption is $< 600\ \mu A$.

Pulse dialling ($\overline{PD}$/DTMF = LOW)

The keyboard entry initiates a recall from a previously stored number or is a simultaneous keying-in and pulsing-out activity, with storing for possible later recall. If in the recalled number or at keying-in the keys *, #, A, B, C, D keys are used these digits will not be transmitted. Normally, keying-in is faster than pulsing-out (fed from the redial register). Pulsing sequences start with M1 going HIGH followed by an inter-digit pause of 900 or 500 ms duration (diode option IDP), followed by a sequence of pulses corresponding to the present digit in store. Each pulse starts with a mark (line break) followed by space (line make).
The pulse period is 100 ms with a mark-to-space ratio of 3:2 or 2:1 (diode option). After transmission os a digit, the next digit will be processed again starting with an inter-digit pause. The pulsing is suspensed if $\overline{HOLD}$ goes LOW. It will be terminated if the current memory content has been transmitted or the handset is replaced (CE = LOW $< t_{rd}$). The pulses are available on the DP line. After completion of the number string M1 goes LOW and the circuit changes from dialling mode to conversation mode.

Dual Tone Multi Frequency dialling ($\overline{PD}$/DTMF = HIGH)

The PCD3341 converts keyboard inputs into serial data, via the I^2 bus lines SDA and SCL, suitable for control of the PCD3312 DTMF tone generator. These tones are transmitted with minimum tone burst durations of 70, 70 ms. The maximum tone burst duration is equal to the key depression time. With redial and repertory dialling tones are automatically fed at a rate of 70, 70 ms. After dialling the muting output goes LOW after a hold-over time of 80 ms and the circuit is switched to the conversation mode.

SYSTEM EXTENSION

The PCD3341 can control the extensions of a telephone set via its I²C bus. Both in DTMF dialling and pulse dialling, an extended repertory dialler provides more than 10 stored on-chip numbers and the indication on a L.C. display of all keys pressed (programming or dialling procedure).
The following ICs can be used in combination with the PCD3341:

- PCD3312 DTMF generator
- PCD8570 256 x 8 static CMOS RAM
- PCF8577 2 LCD drivers in LCD module

DTMF dialling

By using a PCD3312 DTMF generator with I²C bus interface, the PCD3341 may be extended to Dual Tone Multi Frequency dialling applications. This is selected when the input pin $\overline{PD}$/DTMF = HIGH. DTMF dialling is much faster than pulse dialling. Each keypad digit corresponds to a unique combination of two frequencies; one from a group of 4 high frequencies, and one from a group of 4 low frequencies. Both frequencies are applied simultaneously to the line.
The PCD3341 is capable of directly driving the PCD3312 oscillator.

Repertory dialling

If more than 10 stored numbers are required repertory dialling can be extended by the I²C bus lines and external CMOS RAMs (PCD8570) with serial interface. With a RAM capacity of 256 x 8 bits another 20 stored numbers can be added. A maximum of 5 external RAMs can be served by the PCD3341 directly. This provides a telephone with a total capacity of 110 (100) stored numbers.
The number of external RAMs connected on the I²C bus lines is automatically checked by the PCD3341 at initial turn-on.
To identify each RAM, the PCD8570 has 3 hardware address pins (A2, A1, A0) which allows a maximum of 8 RAMs to be connected.

Table 1 Repertory number organisation

PCD8570 address			Keyboard digit(s)	
A2	A1	A0	Without EKB	With EKB
0	0	0	10 to 29	00 to 19
0	0	1	30 to 49	20 to 39
0	1	0	50 to 69	40 to 59
0	1	1	70 to 89	60 to 79
1	0	0	90 to 99	80 to 99
PCD3341			00 to 09	M1 to M10

Display

To display the dialled phone number or programmed number the PCD3341 provides the signals to control a LC Display module using two PCD8577 duplex drivers. These signals are fed via the I²C bus lines.
In the dialling and programming modes the digits are displayed from right to left in the sequence entered by the keyboard. The access pause is indicated by the bar. If the number of digits exceeds 16, they drop out on the left side of the display.

OPERATING PROCEDURE

Initialization

At the first application of the standby power supply, the PCD3341 will clear the RAM in order to avoid a wrong content.
By lifting the handset the buffer capacitor for V_{DD} is charged to the operating voltage. CE will than be activated. Within start-up time the oscillator starts and the initialization program begins.

Automatic access pause setting

Before the start procedure, the system can also be initialized by setting the access pause system (e.g. for PABX applications). The circuit will automatically insert an access pause after recognition of access of a number within a digit group. This (or these) digit(s) must be programmed. Up to a maximum of 3 digits per group can be programmed.
The procedure is as follows:

- Depress and hold pushbutton P
- Press and release pushbutton R
- Enter 1, 2 or 3 digits as access digit for first group
- Release pushbutton P (only if no second group is required)
- Press and release pushbutton R
- Enter 1, 2 or 3 digits for second group
- Release pushbutton P

Apart from the procedure that automatically detectes and insertes access pause(s), a telephone number with up to 2 additional manually inserted access pauses can be dialled or programmed, by pressing button AP. In DTMF dialling mode each access pause has a duration of 1,5 or 2,5 seconds. In PD mode each access pause has a duration of 3 or 5 seconds.

DEVELOPMENT DATA

Data entry

The debounce keyboard entries are written into the on-chip CMOS RAM in consecutive order.

Dialling

If the first pushbutton pressed is 0 to 9 in pulse dialling or 0-9, A to D, *, # in DTMF dialling, digits are entered into the redial register after initial clearing. During the data entry the circuit starts with the transmission of the call and is unaffected by the speed of entry. Transmission continues as long as further data input has to be processed. Up to 18 digits can be stored in the redial register. After the main store overflows, a 10 digit First-In First-Out register (FIFO) takes over as buffer. After transmitting the first digit of the FIFO register this position is automatically cleared to provide space for the storage of new data. In this way, the total number that can be transmitted is unlimited, provided the key-in rate is not excessive. However, if the FIFO register overflows (more than 10 digits in store) further input will be ignored.

Redial

If the first digit entered is "REDIAL" R, the stored number in the redial register will be recalled and transmitted.
If the current content is less than 18 digits, new digits entered are appended automatically to the redial number. After the 18th digit has been entered the FIFO register will take over as previously described in the dialling section.

OPERATING PROCEDURE (continued)

Extended Redial

The dialled number is saved in the extended redial buffer if pushbutton P is the last key pressed before the handset is replaced.
By pressing and releasing pushbutton P followed by pressing and releasing pushbutton R, will cause the extended redial register to be recalled and transmitted in the same manner as by redial. If less than 18 digits are contained in the extended redial register, digits can be added until the total content is 18. After the 18th digit the FIFO register will take over as before. The original number is not affected by the new digits

Direct call/Emergency call

This is a diode option usually operated by a turn key switch. If set the programmed number will be dialled by pressing ANY key. In normal mode the turn key switch is positioned OFF with the diode option OFF.
Programmed is achieved by lifting the handset, depressing the P pushbutton with key in the OFF position, then turning the key switch to ON position (diode option ON). The required telephone number is now entered. Pushbutton P can now be released and the handset replaced.
After programming, the key switch can remain in the ON position (activating emergency call) or be switched off (normal mode). If the key switch is the ON position, emergency calling is possible by removing the handset and pressing ANY pushbutton.

Repertory dialling

The PCD3341 has an on-chip CMOS RAM to store up to ten 18 digit numbers, and can be extended up to 100 (110) numbers using external CMOS RAMs with 2-line serial interface. The circuit automatically checks the number of external RAMs. If no external RAM is connected the on-chip repertory is limited to 10 numbers. In this application the standard keypad (0 to 9) and one digit address can be used. With the diode option EKB (expanded keyboard) ON the extended keypad matrix (M1 to M10) can be used to access the on-chip repertory. If external RAMs are connected the capacity of the repertory can be increased up to 100 (110) numbers. In this application the standard keypad (0 to 9) and/or the extended keypad (M1 to M10) can be used to access the repertory (see Table 1).
Programming is possible only after the handset is lifted and no pushbutton is operated before P.
Programming is achieved by pushbutton P being continually depressed, entering the repertory address of one or two digits, followed by the number (including access digits) then releasing pushbutton P.
The designated telephone number, including access digits, is dialled after pressing pushbutton P followed by the address. With extended keypad a single address pushbutton is required. After transmission of the repertory sequence, it is possible to manually enter additional digits (see redial).

Successive repertory dialling during a call (chain dialling)

It is possible to dial more than one repertory number during one single telephone call.
The following procedures are possible:

- Redial, extended redial or a repertory number followed by new digits
- Repertory number followed by one or more repertory numbers
- Normal dial, redial or extended redial followed by one or more repertory numbers

Note pad

Note pad provides the facility to store a number during conversation mode without dialling and muting. This number will be stored in the extended redial register and recalled with the extended redial procedure.
The programming procedure is as follows:

- Depress and release pushbutton P
- Depress and release pushbutton P
- Enter the telephone number
- Depress and release pushbutton P

If a wrond number is entered, correction is achieved by re-starting the programming procedure.

Memory clear

A built-in manually total clear facilitates resetting of the autodial RAM after servicing, maintenance or telephone set delivery.
The procedure is as follows:

- Hook-on, depress and keep depressed keys 2, 5, 8, 0
- Hook-off, release keys 2, 5, 8, 0

Table 2 Display indications

procedure	key procedure	display indication
Programming automatic access pauses after access digits	$\bar{P}$R00R9	Pr–00–9
dialling	004627530	00–4627530
redial	R	r=00–4627530
Extended redial		
programming	004627530P	00–4627530P
dialling	PR	Pr=00–4627530
emergency redial		
programming	N/D OFF, $\bar{P}$, N/D ON(+ TN)	PH–00–4627530
dialling	N/D ON any key	H=00–4627530
repertory programming	$\bar{P}$12004627530	P12–00–4627530
programming	$\bar{P}$12004627530	P12–00–4627530
dialling	P12	P12=00–4627530
repertory with extended keyboard		
programming	$\bar{P}$ M1 004627530	PM1–00–4627530
dialling	M1	M1=00–4627530
note pad programming	PP0080808P	7530PP00–808080P
note pad dialling	PR	00–808080
error	incorrect key procedure	≡

Where: TN = telephone number
P = depress and release pushbutton P
$\bar{P}$ = depress pushbutton P continually during programming
R = depress and release pushbutton R

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute maximum System (IEC 134)

Supply voltage range (pin 28)	V_{DD}		−0,8 to 8	V
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I	V_{SS} −0,8 V to V_{DD}	+ 0,8	V
Total power dissipation	P_{tot}	max.	500	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,57954 MHz; R_S = 50 Ω max.; T_{amb} = 25 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	3	6,0	V
Operating supply current					
conversation mode (CE = 1)	I_{DDC}	–	270	–	μA
dialling mode (CE = 1)	I_{DDD}	–	600	–	μA
Standby supply voltage (CE = 0)	V_{DDO}	1,8	3	6,0	V
Standby supply current (CE = 0)	I_{DDO}	–	–	2,5	μA
RESET I/O					
Switching level					
at $V_{DD} < V_{RESET}$	V_{RESET}	–	1,3	1,5	V
Sink current					
at $V_{DD} < V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	–	V
Input leakage current; CE					
at $V_I = V_{SS}$ to V_{DD}	$-I_{IL}$	–	–	100	nA
at CE = 1	I_{IL}	–	–	1	μA
Keyboard contact resistance					
Keyboard ON	R_{KON}	–	–	1	kΩ
Keyboard OFF	R_{KOFF}	100	–	–	kΩ
Outputs					
M1, $\overline{M1}$, M3, DP, $\overline{DP}$					
Output sink current					
at V_{OL} = 0,4 V	I_{OL}	–	1,5	–	mA
Output source current					
at V_{OH} = 2,6 V (push-pull)	$-I_{OH}$	–	1,5	–	mA
SDA, SCL					
Output sink current					
at V_{OL} = 0,4 V	I_{OL}	1,5	–	–	mA
Output source leakage current					
at V_{OH} = 0 to V_{DD} (open drain)	$-I_{OH}$	–	–	1	μA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Inputs/Outputs					
COL 1 to 6, ROW 1 to 6, $\overline{HOLD}$, $\overline{APO}$					
Output sink current at V_{OL} = 0,4 V	I_{OL}	0,6	1,5	–	mA
Output source current at V_{OH} = 2,6 V	$-I_{OH}$	25	–	–	μA
Output source current at $V_{OH} = V_{SS}$	$-I_{OH}$	–	–	200	μA
TIMING (see Figs. 5, 6 and 7)					
Clock start-up time	t_{ON}	–	–	10	ms
Oscillator period	C_P	–	–	0,279	μs
Pulse dialling ($\overline{PD}$/DTMF input LOW; M/S diode OFF)					
Mark-to-space ratio 3:2					
Dialling pulse frequency	f_{DP}	–	9,94	–	Hz
Dialling pulse period	t_{DP}	–	100,6	–	ms
Break time	t_b	–	60,3	–	ms
Make time	t_m	–	40,3	–	ms
Mark-to-space ratio 2:1 (M/S diode ON)					
Dialling pulse frequency	f_{DP}	–	9,94	–	Hz
Dialling pulse period	t_{DP}	–	100,6	–	ms
Break time	t_b	–	67	–	ms
Make time	t_m	–	33,5	–	ms
Access pause					
t_{ap} diode OFF	t_{ap}	–	3	–	s
t_{ap} diode ON	t_{ap}	–	5	–	s
Mute hold-over time during access pause	t_h	–	1	–	s
Inter-digit pause					
IDP diode OFF	t_{id}	–	892	–	ms
IDP diode ON	t_{id}	–	496	–	ms
Reset delay time	t_{rd}	–	160,9	180	ms
Reset delay time during access pause	t_{rd}	–	302	320	ms
Debounce time	t_e	13,5	–	–	ms
Flash pulse duration	t_{FL}	–	94	–	ms

parameter	symbol	min.	typ.	max.	unit
DTMF dialling ($\overline{PD}$/DTMF input HIGH; SDA timing via PCD3312)					
Tone transmission time (t_{tb} diode OFF)	t_t	–	74	–	ms
Tone break time	t_b	–	74	–	ms
Mute hold-over time during dialling	t_h	–	154	–	ms
Tone transmission time (t_{tb} diode ON)	t_t	–	101	–	ms
Tone break time	t_b	–	101	–	ms
Mute hold-over time during dialling	t_h	–	101	–	ms
Access pause					
t_{ap} diode OFF	t_{ap}	–	1,5	–	s
t_{ap} diode ON	t_{ap}	–	2,5	–	s
Mute hold-over time during access pause	t_h	–	1	–	s

DEVELOPMENT DATA

Timing diagrams

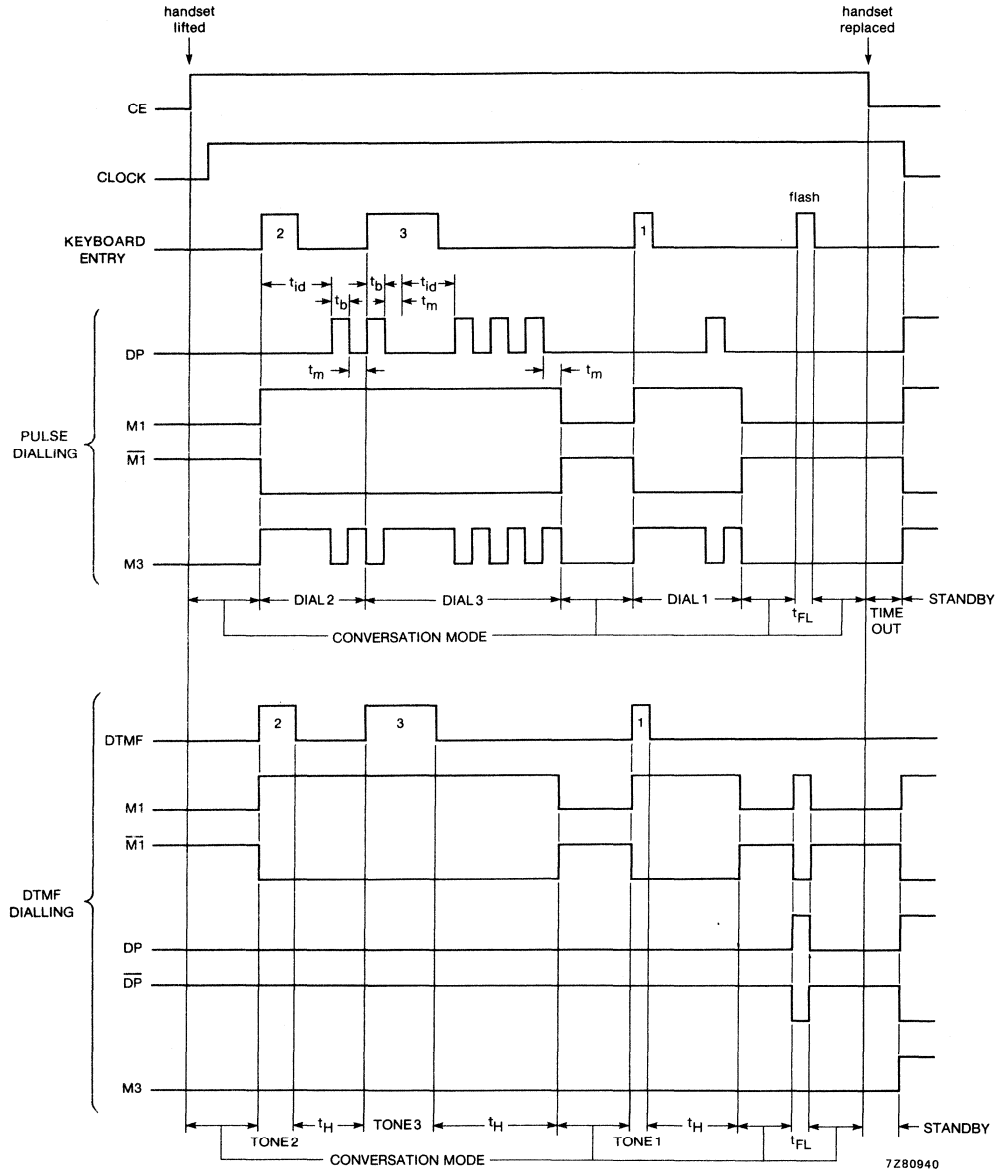


Fig. 5 Pulse dialling; DTMF dialling.

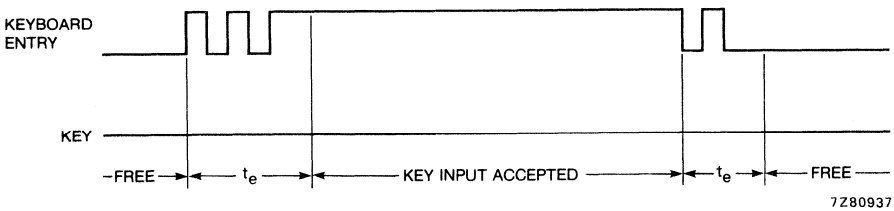


Fig. 6 Keyboard entry with noise debounced.

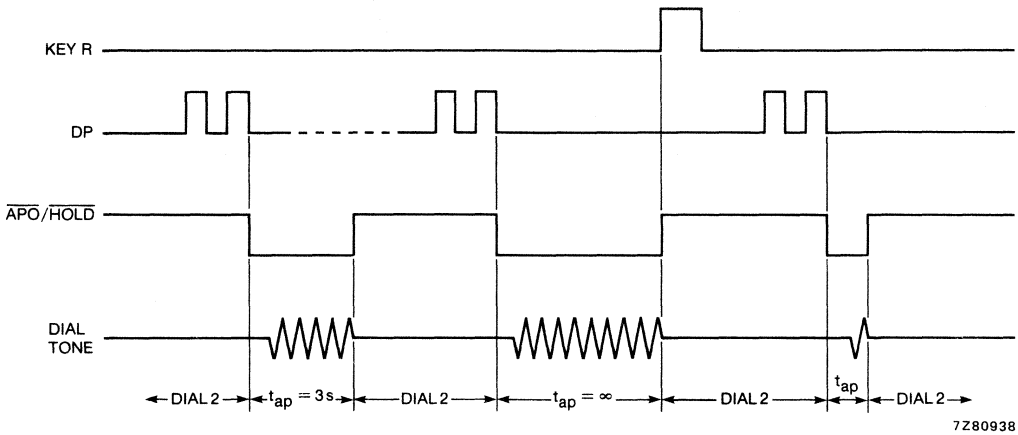


Fig. 7 Access pause with reset by; internal 3 s timer, key R, tone recognizer.

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

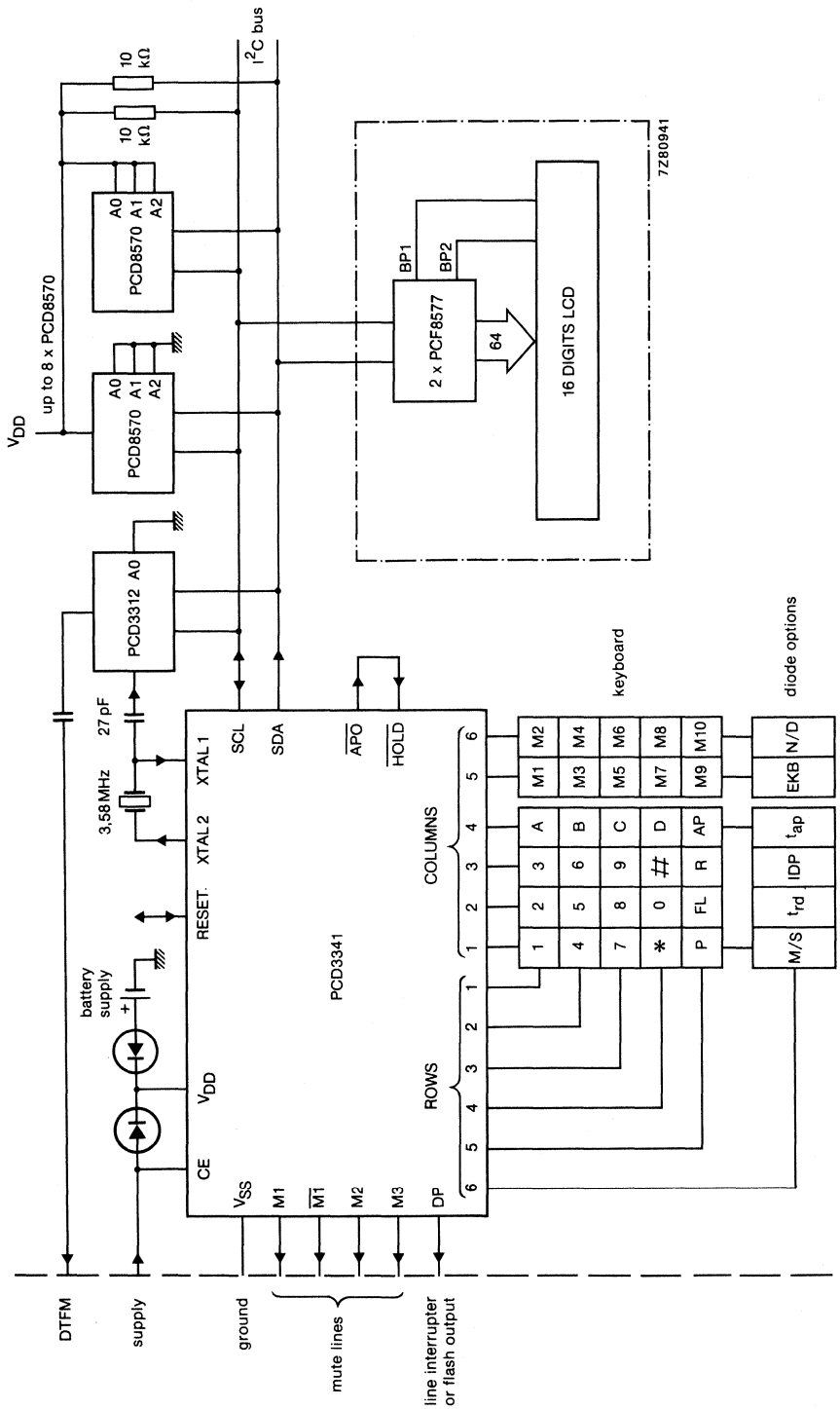


Fig. 8 PCD3341 in combination with PCD3312 (DTMF dialler), PCD8570 (2 K RAM) and PCF8577 (display drivers).

Single-chip 8-bit microcontroller family specification

PCD33XX

1 INTRODUCTION

This family data sheet describes the microcontroller core which is common for all members of the PCD33XX family. For complete information of a particular microcontroller, consult both the specific microcontroller data sheet and this family data sheet.

2 FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single package
- Up to 8 K bytes ROM
- Up to 256 bytes RAM
- Over 80 instructions, all instructions 1 or 2 cycles
- 8 or more quasi bi-directional I/O port lines
- 8-bit programmable timer/event counter
- 3 single-level vectored interrupts: external (chip enable), 8-bit programmable timer/counter, SIO/ derivative
- 2 Test inputs: T0 (may also be used as an interrupt) and T1 (may also be used as an input to an 8-bit counter)
- Serial I/O interface (not all devices)
- Power-on-reset
- 2 power reduction modes: Idle and Stop
- V_{DD} supply range: 1.8 V to 6 V (not all family members; for details on the supply range of a particular device, see the specific microcontroller data sheet)
- Clock frequency range: 450 kHz to 10 MHz
- Operating temperature range: – 20 °C to 70 °C
- Silicon gate CMOS fabrication process

3 GENERAL DESCRIPTION

The PCD33XX single-chip 8-bit microcontroller family consists of a wide range of derivatives containing up to 8 K bytes of on-chip mask programmable program ROM and up to 256 bytes RAM. All devices include flexible I/O ports, an 8-bit programmable timer/event counter and a choice of single-level vectored interrupts. The instruction set is based on that of the MAB8048. A number of PCD33XX family members may be used as CMOS replacements for their NMOS counterparts, where lower power consumption and higher speed are required.

The family is well supported with:

- Cross assemblers
- In-circuit emulation tools
- Window debugger
- Piggy-back versions for prototyping.

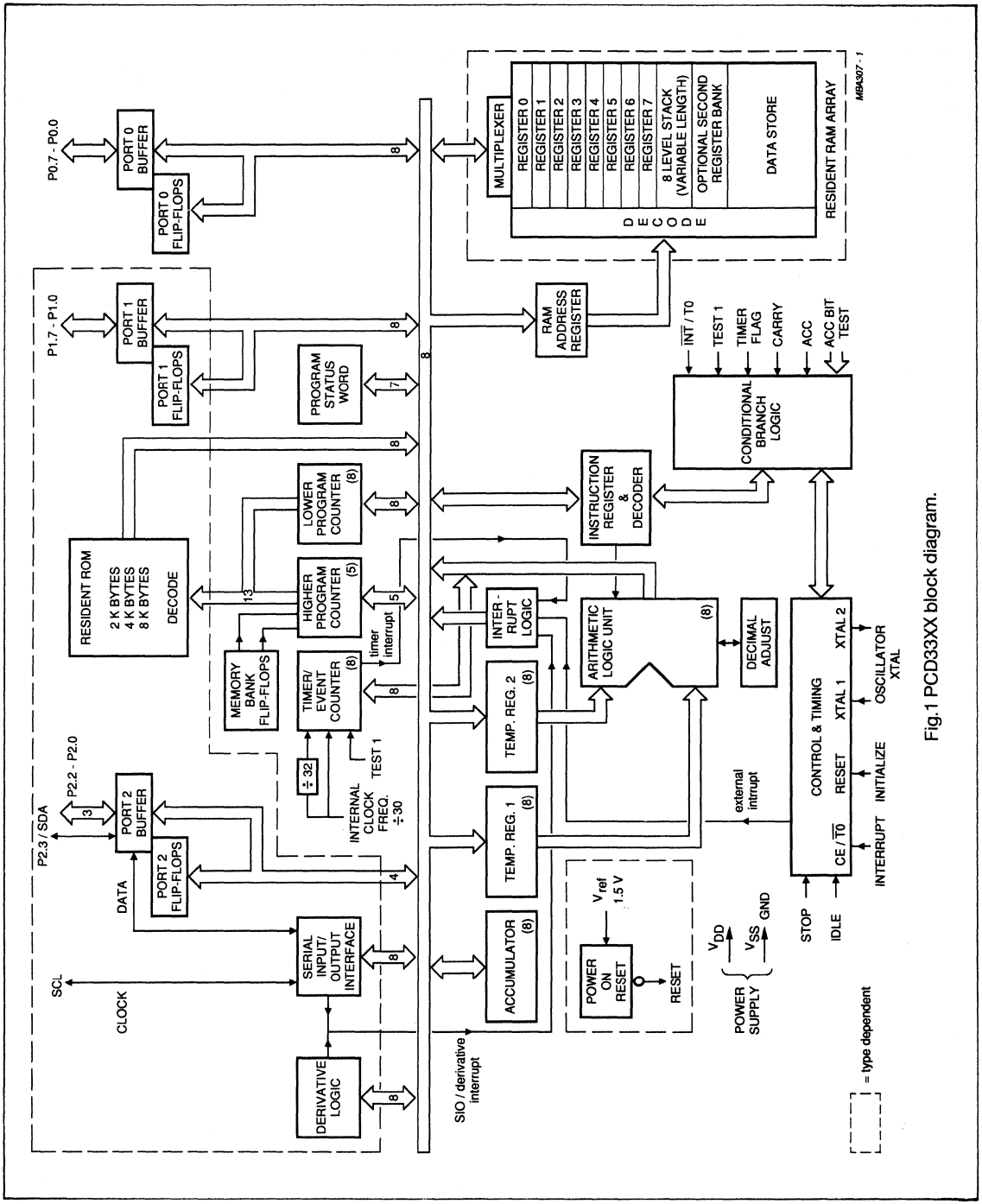


Fig.1 PCD33XX block diagram.

4 FUNCTIONAL DESCRIPTION

4.1 Program memory

Program memory consists of up to 8 K bytes of read-only memory (ROM). Each location is directly addressable by the program counter. The program memory is mask-programmed at the factory. Figure 2 shows the program memory map.

Four program memory locations are of special importance:

- Location 0: first instruction to be executed after the microcontroller is reset.
- Location 3: first instruction of an external (chip enable) interrupt (CE/$\overline{T0}$) service routine.
- Location 5: first instruction of an SIO/derivative interrupt service routine.
- Location 7: first instruction of a timer/event counter interrupt service routine.

Of the 13-bits in the program counter, only 11 function as a counter. The two most significant bits are preset by SEL MB instructions. Thus, program memory is arranged in banks of 2 K bytes. Memory bank boundaries can only be crossed using unconditional branches (JMP) or subroutine calls (CALL) after the appropriate memory bank has been selected by a SEL MB instruction.

Each program memory bank is further divided into 8 pages of 256 bytes. Indirect (JMPP) and conditional branches can't cross page boundaries.

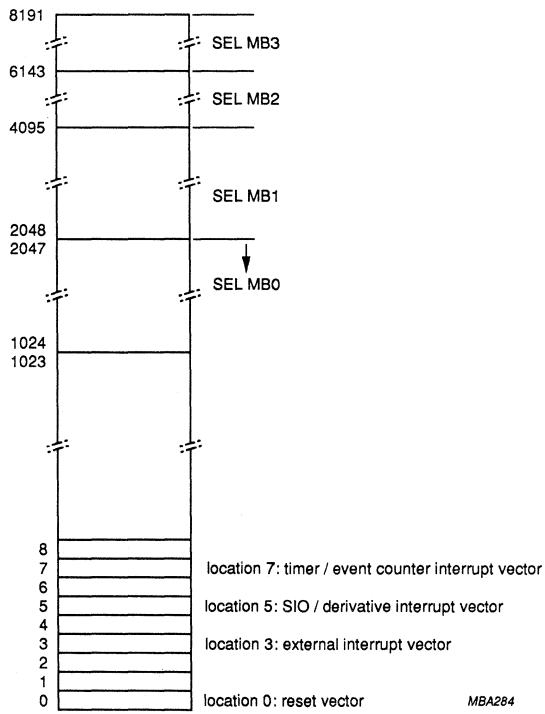


Fig.2 Program memory map.

4.2 Data memory

Data memory consists of up to 256 bytes of random access memory (RAM). All locations are indirectly addressable using RAM pointer registers. Up to 16 register locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. All RAM locations make efficient program loop counters when used with the 'decrement register and test' instruction DJNZ. Figure 3 shows the data memory map.

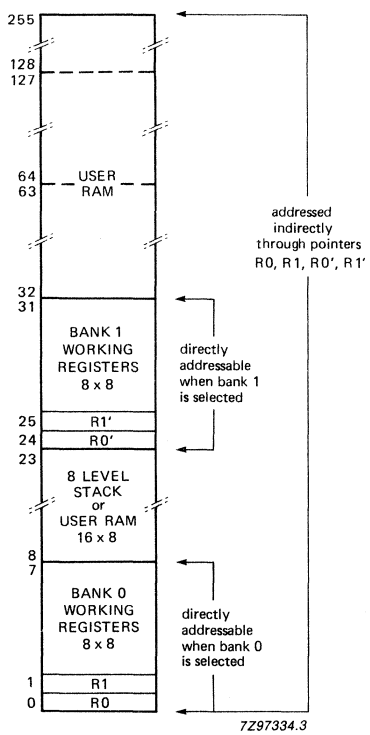


Fig.3 Data memory map.

4.2.1 Working registers

Locations 0 to 7 may be selected as working registers by the SEL RB0 instruction. These locations may then be accessed using efficient one byte, one cycle instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents make the working registers ideal for frequently accessed intermediate results.

Instead of locations 0 to 7, locations 24 to 31 may be selected as working registers by the SEL RB1 instruction. Register bank 1 may be used as an extension of register bank 0, as an alternative register bank for use by interrupt service routines, or as general purpose data memory.

The first two locations of each bank contain the RAM pointer registers (R0, R1, R0' and R1') which indirectly address all RAM locations.

4.2.2 Program counter stack

Locations 8 to 23 may be used as an 8-level program counter stack reserving 2 locations per level, or as general purpose RAM. The stack (Fig.4) saves return addresses and status during interrupt or subroutine servicing. Up to 8 levels of subroutine/interrupt nesting is possible.

A 3-bit stack pointer always points to the next free stack level. Following a device reset, the stack pointer points to level 0 (locations 8 and 9). On each subroutine call or interrupt, the contents of the 13-bit program counter and bits 4, 6 and 7 of the program status word are transferred to the level indicated by the stack pointer. The stack pointer increments and points to the next free level. Overflow from level 7 to level 0 occurs after nesting eight levels deep. Further subroutine calls and/or interrupts should be avoided since the contents of level 0 would be overwritten and lost.

The RETR instruction must be used to terminate an interrupt service routine. The RETR instruction decrements the stack pointer, and restores the program counter and status word. A subroutine should be terminated with the RET instruction. The RET instruction restores the program counter but does not restore the program status word.

As a general rule, the use of RETR in conjunction with a subroutine call is not recommended. RETR must not be used to terminate a subroutine which has been called within an interrupt routine since it would prematurely terminate the interrupt routine.

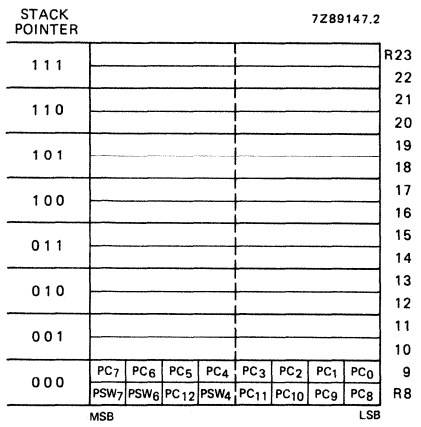


Fig.4 Program counter stack.

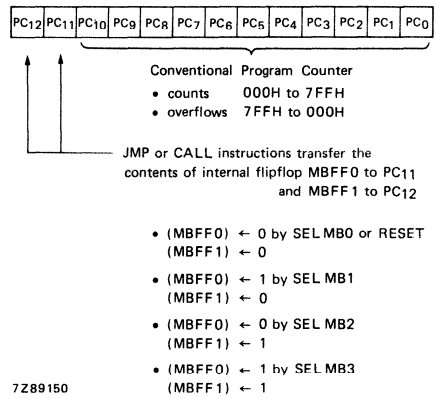


Fig.5 Program counter.

4.3 Program counter

The 13-bit program counter can address up to 8 K bytes of ROM (Fig.5). The least significant 11 bits (PC0 to PC10) are auto-incrementing. The two most significant bits, PC11 and PC12, are loaded with the contents of two internal flip flops (MBFF0 and MBFF1 respectively) when a JMP or CALL instruction is executed. The contents of these two internal flip-flops can be altered by the SEL MB instructions.

4.4 Program status word

The program status word (PSW) is an 8-bit register in the CPU which stores information about the current status of the microcontroller (Fig.6).

All bits can be read using the MOV A,PSW instruction. Only the PS bit can be written using the MOV PSW,A instruction. Table 1 describes the PSW bits and how they are affected.

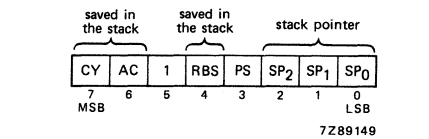


Fig.6 Program status word.

Table 1 Program status word.

BIT	NAME	FUNCTION	AFFECTED BY
7	CY	Carry, signals accumulator overflow	ADD, ADDC, DA, RLC, RRC, CLR C and CPL C instructions
6	AC	Auxiliary Carry, half carry	ADD and ADDC instructions
5	-	Not used, always 1 when read	
4	RBS	Register Bank Select 0: select register bank 0 1: select register bank 1	SEL RB instructions
3	PS	Timer Prescaler Select 0: prescaler selected (÷32) 1: prescaler not selected (÷1)	MOV PSW,A instruction
2 1 0	SP2 SP1 SP0	Stack Pointer bits 2-0	CALL, RET, RETR instructions and interrupts

Table 2 Interrupts.

INTERRUPT			INSTRUCTION	
PRIORITY	TYPE	VECTOR LOCATION	ENABLE	DISABLE
1 (highest)	external (chip enable)	003 (ROM)	EN I	DIS I
2	SIO/derivative interrupt	005 (ROM)	EN SI	DIS SI
3 (lowest)	timer/event counter	007 (ROM)	EN TCNTI	DIS TCNTI

4.5 Central processing unit

The PCD33XX instruction set provides arithmetic, logical, branching, input/output, and control facilities. The DA A, SWAP A, and XCHD instructions simplify BCD arithmetic and nibble handling. The MOVP A,@A instruction enables efficient table look-up within the current ROM page. The instruction set also has facilities for conditional branching and loop control (DJNZ).

4.6 Interrupts

The PCD33XX family handles external (chip enable), SIO/derivative and timer/event counter interrupts. The interrupt mechanism is single level. An executing interrupt routine can only be interrupted by a hardware RESET; it can't be interrupted by other interrupts (which are latched). If several interrupt requests are detected simultaneously, they are serviced in order of priority (see Table 2).

An interrupt request will only be serviced if the corresponding interrupt enable flag is set (Fig.7). When a request is serviced, the contents of the program counter, and bits 4, 6 and 7 of the program status word are saved on the program counter stack. The program counter is loaded with the appropriate interrupt vector which points to the start of the interrupt service routine. Since the accumulator is not automatically saved, it must be saved and restored by user software. The interrupt routine must be terminated by the RETR (return and restore) instruction. At least one instruction in the main program will then be executed before another interrupt routine is serviced.

To avoid erroneous real-time programs, a few words of caution:

- While the interrupt is in progress, the two most significant bits of the program counter are frozen at zero. Thus, interrupt routines and subroutines called from interrupt routines must reside (entirely) in memory bank 0.
- The SEL MB instruction should not be used within interrupt routines or in subroutines called within interrupt routines because altering the contents of MBFF0 and MBFF1 (Fig.5) may lead to erroneous JMP and CALL destinations after return from interrupt.
- Subroutines and nested subroutines called within an interrupt routine must all end with RET since RETR clears the IIP (interrupt in progress) flag (Fig.7 and Fig.8). Further pending interrupts would then interfere with the interrupt routine in progress.

4.6.1 External (chip enable) interrupt

A LOW-TO-HIGH transition on the CE/$\overline{T0}$ pin is latched in the digital filter latch if the HIGH state exceeds 7 clock periods after a LOW state of more than 4 clock periods. If the external interrupt is enabled, then the external interrupt flag (EIF) will also be asserted, constituting a valid external interrupt request. As soon as the IIP is clear, indicating that no interrupt routine is in progress, the external interrupt is invoked by a forced CALL to location 3. The EIF flag is simultaneously cleared (Fig.7 and Fig.8). The interrupt routine may acknowledge the interrupt via port lines.

Execution of a DIS I (disable external interrupt) instruction cancels a stored interrupt request by clearing both the digital filter latch and the EIF.

EI	External Interrupt
SI	SIO/Derivative Interrupt
TI	Timer/event counter Interrupt
EIF	External Interrupt Flag
TIF	Timer Interrupt Flag
PIN	Pending Interrupt Not
IIP	Interrupt In Progress Flag

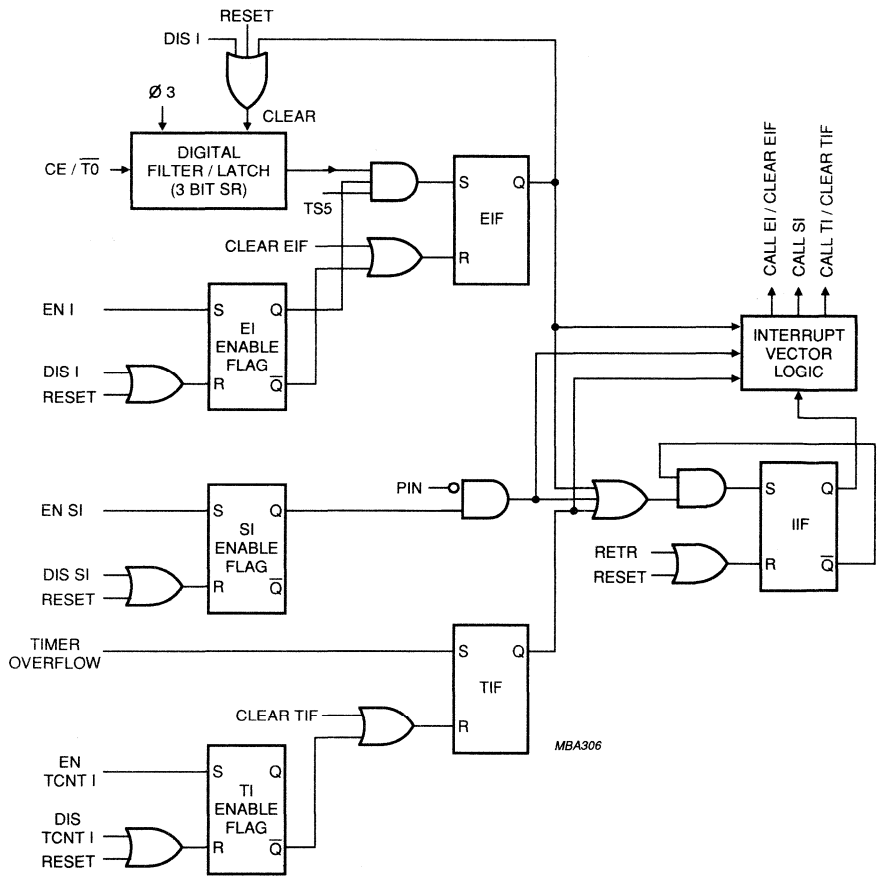


Fig.7 Simplified interrupt logic schematic (the R input overrules the S input for all flags).

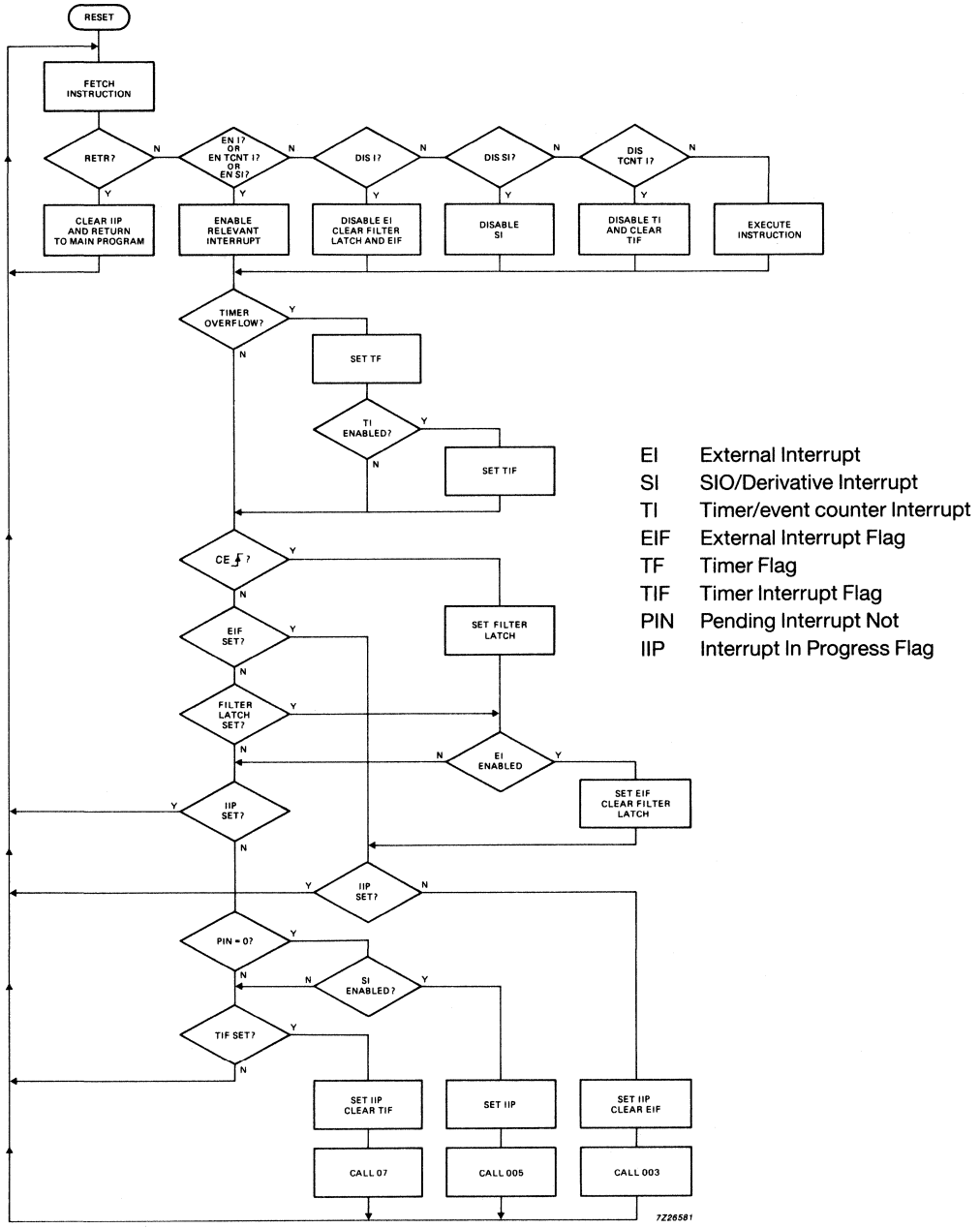


Fig.8 Flow chart illustrating CPU control in the presence of interrupts.

4.6.2 SIO/DERIVATIVE INTERRUPT

The SIO/derivative interrupt is shared between the serial I/O interface (if available) and the derivative logic (if available). Software polling may be necessary to determine the origin of a request.

An interrupt request from the SIO or derivative logic will force the PIN flag to its active LOW state. This action is independent of the Enable SIO interrupt enable flag. If the SIO/derivative interrupt is enabled and no interrupt routine is in progress, the active LOW PIN flag will invoke the SIO/derivative interrupt routine by forcing a CALL to program memory location 5. Invoking the SIO/derivative interrupt routine does not automatically clear the PIN flag. PIN must be cleared to its inactive HIGH state by software during the interrupt routine.

More details on SIO interrupts are given in the section on the serial I/O interface. For specific information on derivative interrupts, consult the relevant data sheet.

4.6.3 TIMER/EVENT COUNTER INTERRUPT

When the timer/event counter interrupt is enabled, a timer/event counter overflow sets the Timer Interrupt Flag (TIF). As soon as the Interrupt in Progress (IIP) flag is clear (indicating that no interrupt routine is in progress), the timer/event counter interrupt routine is invoked by a forced CALL to program memory location 7, and the TIF flag is simultaneously cleared (Fig.7 and Fig.8).

Execution of a DIS TCNTI (disable timer/event counter interrupt) instruction cancels a stored interrupt request by clearing the TIF flag.

An additional external interrupt may be simulated by enabling the timer/event counter (EN TCNTI) and loading the counter with FFH (one less than overflow). If the event counter mode is enabled by executing the STRT CNT instruction, a rising edge on the T1 input will cause a counter overflow and set TIF.

4.7 Interrupt/Test 0 input (CE/$\overline{T0}$)

The CE/$\overline{T0}$ input may be used as:

- chip enable
- a test 0 input for branch instructions JT0 and JNT0.

When used as a test 0 input (chip enable disabled):

- the conditional branch instruction JT0 will cause a branch if CE/$\overline{T0}$ = logic 0
- the conditional branch instruction JNT0 will cause a branch if CE/$\overline{T0}$ = logic 1.

There is no internal pull-up or pull-down resistor connected to the CE/$\overline{T0}$ input. When CE/$\overline{T0}$ is not used, it must be tied to V_{DD} or V_{SS}.

4.8 Timer/event counter

The internal 8-bit up-counter may be configured to count external events, modulo-32 machine cycles, or machine cycles directly. The MOV A,T and MOV T,A instructions can be used to read and preset the counter.

After a STRT T (start timer) instruction, the counter will increment either every machine cycle (30 oscillator periods) or every 32 machine cycles. If the PS bit in the program status word is set, the counter increments every machine cycle. If the PS bit is reset, it increments every 32 machine cycles. STRT T clears the prescaler which is not otherwise accessible (see Fig.9).

After a STRT CNT (start event counter) instruction, the counter will count each LOW-to-HIGH transition on pin T1 provided that the HIGH state exceeds 4 oscillator periods after a LOW state of more than 4 oscillator periods. The maximum count rate is one increment per machine cycle ($f_{XTAL}/30$).

The timer/event counter is inhibited after reset or by executing a STOP TCNT (stop timer/event counter) instruction (see Fig.9).

When a T1 overflow occurs:

- if the timer/event counter interrupt is enabled, the Timer Interrupt Flag (TIF) is set and an interrupt request is generated
- the Timer Flag (TF) is set. TF can be tested by conditional branch instructions JTF (jump if TF = logic 1) and JNTF (jump if TF = logic 0). When a JTF or JNTF instruction is executed, TF is reset. The only other way to clear TF is to reset the microcontroller.

Table 3 Timer/event counter control.

FUNCTION	TIMER MODE	COUNTER MODE
clear	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
preset	MOV T,A	MOV T,A
start	STRT T	STRT CNT
stop	STOP TCNT or RESET	STOP TCNT or RESET
test	JTF/JNTF	JTF/JNTF
read	MOV A,T	MOV A,T

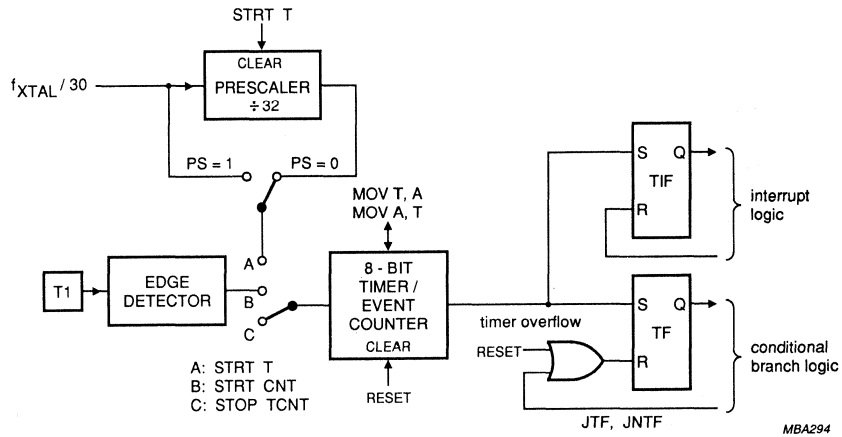


Fig.9 Timer/event counter.

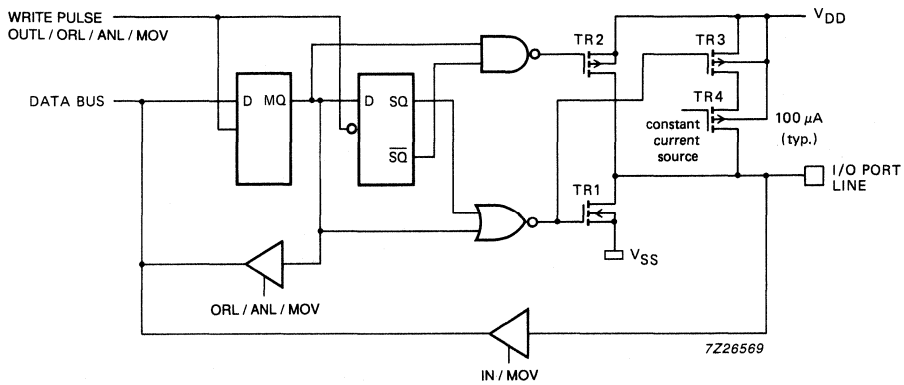


Fig.10 Standard port with switched pull-up current source (mask option 1).

4.9 Test 1/Count input (T1)

The T1 input may be used as:
- a count input to the 8-bit timer/event counter
- a test 1 input for branch instructions JT1 and JNT1.

When used as a test input:
- the conditional branch instruction JT1 will cause a branch if T1 = logic 1
- the conditional branch instruction JNT1 will cause a branch if T1 = logic 0.

There is no internal pull-up or pull-down resistor connected to the T1 input. When T1 is not used, it must be tied to V_{DD} or V_{SS}.

4.10 Parallel ports

The PCD33XX family provides up to three standard quasi-bidirectional I/O ports:
- Port 0: 8-bit parallel port (P0.0 to P0.7)
- Port 1: 8-bit parallel port (P1.0 to P1.7)
- Port 2: 4-bit parallel port (P2.0 to P2.2, P2.3/SDA)

Several members of the PCD33XX family provide all 20 I/O lines and all members contain port 0.

In addition to the standard ports, many PCD33XX microcontrollers provide a variety of derivative ports. For specific details, consult the relevant data sheet.

In general, all parallel ports lines can be individually configured as outputs or inputs. Output data written to a port is latched and remains unchanged until rewritten. Input data is not latched and must be stable when read by an input instruction.

The standard port configuration is shown in Fig.10. When a logic 0 is written to the master/slave flip-flop, TR2 and TR3 are turned off, turning off the constant current source. Current sinking is provided by TR1 which is simultaneously turned on, and the output is pulled LOW to V_{SS}.

When a logic 1 is written to the master/slave flip-flop for the first time (MQ = 1, SQ = 0), TR1 is turned off and TR3 is turned on. TR2 is also switched on for the duration of the internal write pulse (one oscillator period), driving the output rapidly to V_{DD}. TR3 turns on the constant current source TR4 which sources sufficient current for a TTL HIGH level; however, the port line can be pulled LOW by an external CMOS device, enabling the same pin to be used for both input and output. This arrangement also facilitates wired-OR applications. Subsequent writing of a logic 1 to the port line will not switch TR2 on. Booster transistor TR2 is only turned on for one oscillator period during a 0-to-1 transition at the output of the master/slave flip-flop.

To use the port line as an input, a logic one must written to the port line to turn TR1 off.

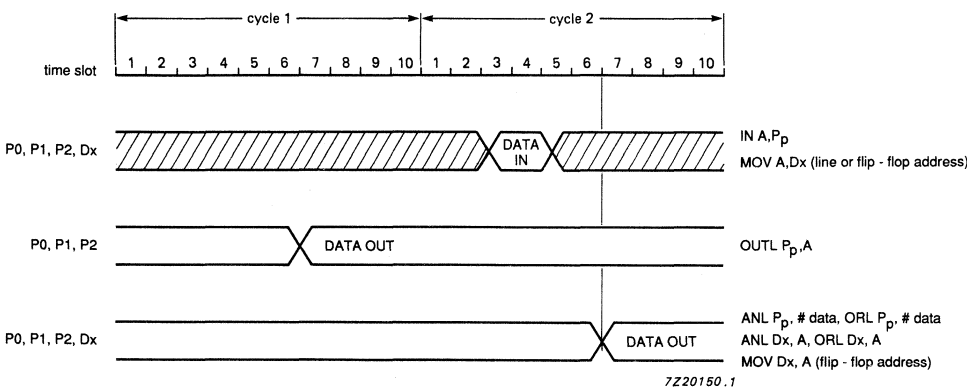


Fig.11 Input/output timing of standard and derivative ports.

Table 4 Derivative port addressing.

DERIVATIVE ADDRESS	TYPE	ACCESS
8-bit line address	R	derivative port line
8-bit flip-flop address	R/W	derivative port flip-flop

Ports 0, 1 and 2 are accessed using the parallel input/output instructions IN, OUTL, ANL and ORL. IN inputs port data to the accumulator. OUTL outputs accumulator data to the port. ANL and ORL are used to manipulate data in the port flip-flops.

Derivative ports are accessed by the derivative input/output instructions MOV, ANL and ORL. ANL and ORL are used to manipulate data in the port flip-flops. MOV is used for all data transfers between the port and the accumulator. When reading data into the accumulator, the data source can be a port line or the port flip-flop. Thus, two derivative addresses are provided per port (see Table 4).

All standard and derivative port accesses are performed by two-cycle instructions. Instruction timing is shown in Fig.11. For input operations, data is read during time slots 3 and 4 of machine cycle 2. For output operations, the data is written during time slot 7. For OUTL, data is written during machine cycle 1. For ANL, ORL and MOV Dx,A, data is transferred during machine cycle 2.

Three I/O mask options make it possible for every parallel I/O port line to be individually configured as follows:

Option 1 Standard Port: quasi-bidirectional I/O with switched pull-up current source (100 μA typ.) and p-channel booster transistor TR2. TR2 is only active for 1 clock cycle during 0-to-1 transitions (Fig.10).

Option 2 Open Drain: quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires the connection of an external pull-up resistor (Fig.12). If unused, an option 2 output should be tied to V_{SS} to prevent undesirable current flow through input stages.

Option 3 Push-Pull: outputs can sink or source 2 mA (typ.) at V_{DD} = 3 V. Push-pull lines may not be used as inputs (Fig.13).

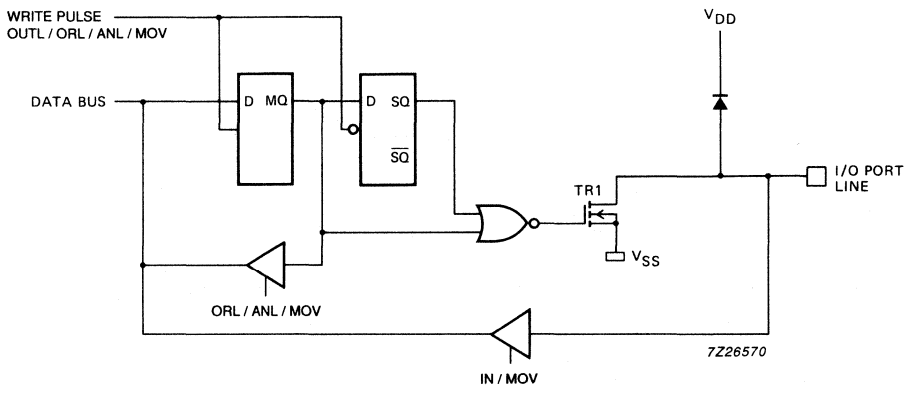


Fig.12 Open drain (mask option 2).

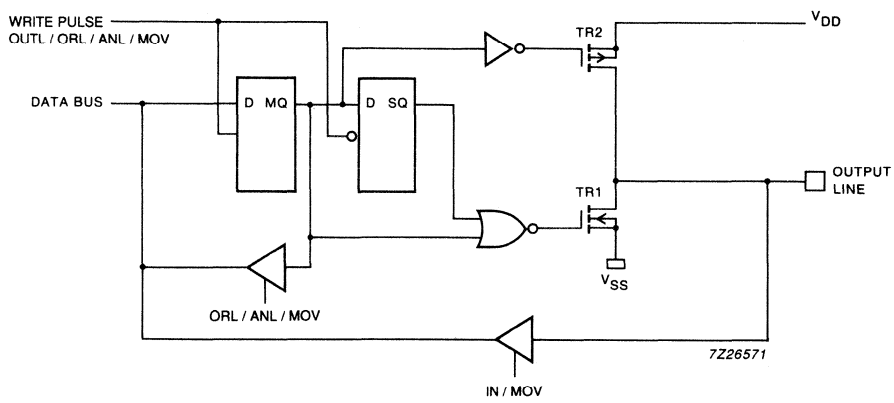


Fig.13 Push-pull (mask option 3).

For devices with a serial I/O interface, P2.3 becomes SDA and must be configured as an open drain (option 2) I/O line.

For the remaining port lines (P0.0 to P2.2), all three options are generally available. For some family members, option 3 on port 0 and port 1 lines may be restricted for emulation purposes. For specific information, refer to the relevant data sheet.

4.11 Serial I/O interface

Many members of the PCD33XX family have an on-chip serial I/O interface (I^2C). This two-line serial bus extends the microcontroller capabilities since it fully supports the PCF85XX (clips) family of I^2C-bus peripheral devices.

Microcontrollers that do not have dedicated serial I/O hardware can use port pins and software to simulate a serial interface. However, such microcontrollers must continuously monitor the serial bus, the data transfer rate is slower, and this approach may require significant processing and memory resources.

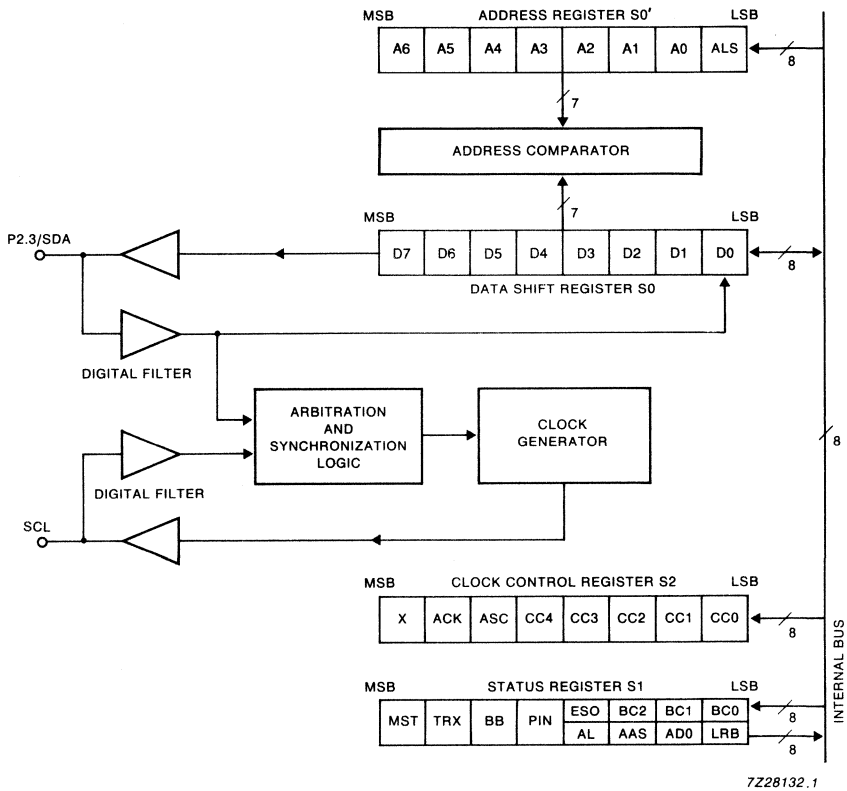
Each device on the I^2C-bus is allocated a 7-bit address. Address recognition is performed by the serial interface hardware and the microcontroller is interrupted only after a valid address (own address or general call address) has been recognized. The SIO hardware also transfers data serially and performs parallel-to serial and serial-to-parallel conversion without disrupting program execution. The microcontroller is interrupted only after a complete data byte has been transferred; the next data byte can then be written to or read from the serial I/O interface.

The serial I/O interface also facilitates the implementation of multimaster systems in which two or more microcontrollers communicate via the same I^2C-bus. An automatic arbitration procedure handles bus conflicts.

The I^2C-bus consists of a dedicated bidirectional clock line (SCL) and a bidirectional data line (P2.3/SDA) which also functions as parallel port line P2.3. When the serial I/O interface is enabled, P2.3 is disabled as a port line. Input signals on SCL and SDA are filtered for enhanced noise immunity. SCL and SDA are open drain and require external pull-up resistors if they are to be used as outputs. If unused, these two pins should be tied to V_{SS}.

The CPU and serial I/O interface communicate via the following four serial I/O interface registers (see Fig.14):

- Data Shift Register (S0)
- Address Register (S0')
- Clock Control Register (S2)
- Status Register (S1)



X = don't care

Fig.14 Serial I/O interface block diagram.

4.11.1 Data shift register (S0)

The data shift register converts serial data to parallel format and vice versa. The most significant bit is transferred first. An interrupt request is generated after a complete byte has been transferred or after a valid I²C-bus address has been detected. The MOV A,S0 instruction may be used to read S0; the MOV S0,A and MOV S0,#data instructions may be used to write to S0 if the ESO (enable serial I/O) bit in the status register (S1) is set.

4.11.2 Address register (S0')

The address register contains the device's 7-bit I²C-bus address and the ALS (always selected) bit. When ALS is zero (the recommended operating mode) bus transfers are ignored unless the START condition is immediately followed by the valid device address or the 'general call' address (00H). If ALS is set, any transfer on the bus is stored in the data shift register. The address register S0' is write-only. The MOV S0,A and MOV S0,#data instructions may be used to write to S0' if the ESO (enable serial I/O) bit in the status register (S1) is zero.

4.11.3 CLOCK CONTROL REGISTER (S2)

The clock control register is a write only register. Bits 0 to 4 of S2 define the serial clock frequency (f_{SCL}) as an integer multiple of the microcontroller clock frequency (Table 5).

Bit 5 (ASC) defines the asymmetrical clock duty cycle. If ASC is set, SCL has a duty cycle of approximately 75%. The asymmetrical clock limits the I²C-bus transmission rate to below 55 kHz. Divisors 39, 45 and 51 are not allowed if ASC is set. Resetting ASC (recommended operating mode) sets the SCL duty cycle to approximately 50%, allowing higher I²C-bus transmission rates of up to 100 kHz, and all of the divisors in Table 5 may be used.

For normal I²C-bus operation, bit 6 (ACK) must be set. After each byte transfer, an extra SCL pulse is generated during which the receiver may acknowledge reception. If ACK is reset, no acknowledge phase is available. This mode is used when a master receiver refuses to acknowledge a transfer in order to signal the 'end of transmission' to a slave transmitter.

Table 5 f_{SCL} as defined by the clock control register S2.

CC0 to CC4 (HEX)	f_{XTAL} DIVIDED BY	f_{SCL} (kHz) @ f_{XTAL} = 6 MHz	f_{SCL} (kHz) @ f_{XTAL} = 10 MHz
0	not allowed		
1	39	154*	256*
2	45	133*	222*
3	51	118*	196*
4	63	95	159*
5	75	80	133*
6	87	69	115*
7	99	61	101*
8	123	49	81
9	147	41	68
A	171	35	58
B	195	31	51
C	243	25	41
D	291	21	34
E	339	18	29
F	387	16	26
10	483	12	21
11	579	10	17
12	675	8.9	15
13	771	7.8	13.4
14	963	6.2	10.4
15	1155	5.2	8.7
16	1347	4.5	7.4
17	1539	3.9	6.5
18	1923	3.1	5.2
19	2307	2.6	4.3
1A	2691	2.2	3.7
1B	3075	2.0	3.3
1C	3843	1.6	2.6
1D	4611	1.3	2.2
1E	5379	1.1	1.9
1F	6147	1.0	1.6

* not permitted; f_{SCL} max. = 100 kHz in I²C systems

4.11.4 STATUS REGISTER (S1)

The status register controls the serial I/O interface and provides feedback about on-going bus transfers. Register S1 can be accessed by the MOV A,S1, MOV S1,A and MOV S1,#data instructions. The lower nibble of the status register is duplicated: control bits BC0-BC2 and ESO are write only, whereas feedback bits LRB, AD0, AAS and AL are read only. The status bits interact in intricate ways with each other. This must be kept in mind when developing an I²C-bus application. Table 6 describes the status bits.

4.11.4.1 Master bit (MST) and transmitter bit (TRX)

The MST and TRX bits determine the operating mode of the serial I/O interface. When not engaged in a bus transfer, MST and TRX should always be zero, placing the SIO in the slave receiver mode (see Fig.15). Return to the slave receiver mode is always performed by software. If the previous mode was a master mode, the transition (MOV S1,#D8H) involves a STOP condition, which automatically clears both MST and TRX.

The transition to the master transmitter mode is also performed by software. However, transitions to the master receiver and slave transmitter modes occur automatically if ALS = 0 (standard I²C-bus protocol). A slave receiver becomes a slave transmitter if the R/$\overline{W}$ bit in the valid address immediately following a START condition is set. A master transmitter becomes a master receiver if R/$\overline{W}$ is set in the transmitted address.

Table 6 Serial I/O status register (S1).

BIT	NAME	TYPE	DESCRIPTION
MST	Master	R/W	MST = 0: Slave (SCL input) MST = 1: Master (SCL output)
TRX	Transmitter	R/W	TRX = 0: Receiver (SDA/P2.3 input) TRX = 1: Transmitter (SDA/P2.3 output)
BB	Bus Busy	R/W	BB = 0: Bus inactive (R)/generates STOP condition (W) BB = 1: Bus busy (R)/generates START condition (W)
PIN	Pending Interrupt Not	R/W	PIN = 0: Serial interrupt pending (after byte transfer, valid address or lost arbitration); SCL forced to V_{SS} PIN = 1: No serial interrupt pending
ESO	Enable Serial I/O	W	ESO = 0: Serial I/O interface disabled; write access to S0' possible ESO = 1: Serial I/O interface enabled; write access to S0 possible
BC0, BC1, BC2	Bit Counter	W	Preset of the Bit Counter for 1 up to 8 serial data bits. (001) = 1 bit, (010) = 2 bits, etc. (000) = complete byte (8 bits) = default value.
AL	Arbitration Lost	R	AL = 1: Arbitration Lost (bus conflict) AL = 0: When corresponding serial interrupt (PIN) is cancelled
AAS	Addressed As Slave	R	AAS = 1: Following a START condition if a valid address is detected (ALS = 0), or if the first byte is received (ALS = 1) AAS = 0: When corresponding serial interrupt (PIN) is cancelled
AD0	Address Zero	R	AD0 = 1: Following a START condition if the general call address (00H) is detected AD0 = 0: After a repeated START or a STOP condition
LRB	Last Received Bit	R	Set or reset depending on last bit transferred, acknowledgement bit if ACK = 1

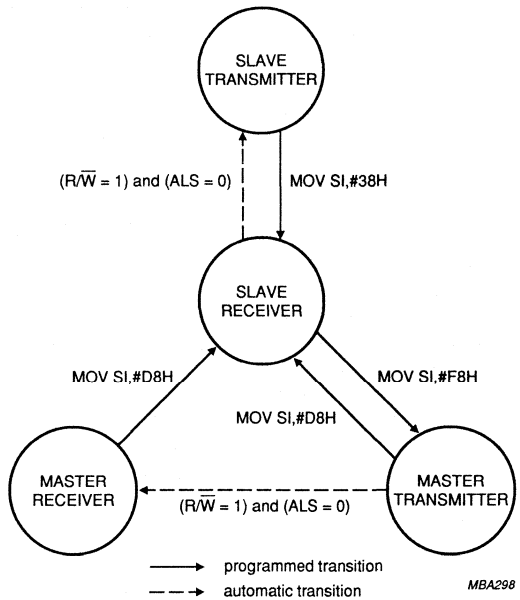


Fig.15 State diagram of the serial I/O interface.

4.11.4.2 Pending interrupt not bit (PIN)

If either MST or ALS is set, PIN is reset to zero (activated) after every byte transfer. If MST and ALS are both reset, PIN becomes zero (generating a serial interrupt request) when the valid address is detected and after each byte of the following transfer. Clock synchronization is implemented as follows: the SCL line is pulled to V_{SS} as long as PIN is zero enabling a slave to delay a master in order to read the data register (in the case of a slave receiver) or to write to the data register (in the case of a slave transmitter). PIN is automatically inactivated when S0 is accessed; it may also be inactivated by explicitly setting PIN to logic 1.

If the SIO/derivative interrupt is disabled, the serial I/O interface may be serviced by testing PIN directly in user software.

4.11.4.3 Bus busy bit (BB)

The status of the BB bit is controlled by the serial I/O interface or by bus master software. When a master clears BB (MOV S1,D8H), the serial I/O interface automatically clears MST and TRX, returning to the slave receiver mode (see Fig.15). If BB is set, write access to S1 other than accesses by the master or an addressed slave are inhibited. If BB is inadvertently set by excessive noise on the bus, the deadlock can be resolved by executing two consecutive MOV S1,18H instructions, the first of which just clears BB.

When a slave transmitter detects an end of transmission (signalled by the absence of an acknowledgment from the master receiver), it has to access S1 to inactivate PIN and become a slave receiver. However, BB should remain set. This is reflected by the MOV S1,38H instruction in Fig.15. When PIN = logic 1, clock synchronization terminates, enabling the master to generate the STOP condition.

A START condition must only be generated when BB = logic 0. Otherwise, the serial I/O interface responds as if bus arbitration had been lost.

4.11.4.4 Arbitration lost bit (AL)

The AL bit is set by the serial I/O interface when it loses bus arbitration in the master transmitter mode. Simultaneously, MST and TRX are cleared to enable the interface (now in the slave receiver mode) to determine if it is validly addressed by the device that won the arbitration. PIN is activated when the byte transfer is complete. AL will be cleared when the serial interrupt is terminated.

4.11.4.5 Addressed as slave bit (AAS)

AAS is set by the serial I/O interface following a START condition when the valid address is detected (ALS = logic 0 in register S0') or when the first byte is received (ALS = logic 1 in register S0'). AAS is cleared when the serial interrupt is terminated.

4.11.4.6 Address zero bit (AD0)

AD0 is set by the serial I/O interface independently of ALS when the 'general call' address (00H) is detected following a START condition. AD0 is cleared after a repeated START or a STOP condition.

4.11.4.7 Last received bit (LRB)

LRB contains the last bit transferred. If ACK = logic 1, LRB contains the acknowledgement bit. It remains valid as long as PIN = logic 0.

4.11.4.8 Enable serial I/O bit (ESO)

The ESO bit enables/disables the serial I/O interface. When ESO = logic 0, access to register S0' is enabled, the SCL pin is in a high impedance state and the P2.3/SDA pin is made available as a normal I/O port line.

When ESO = logic 1, the serial I/O interface is enabled and access to register S0 is possible. The remaining S1 bits can only be altered when ESO is set. The SCL and P2.3/SDA pins are enabled as serial clock and data lines respectively.

To avoid bus deadlock, ESO must be reset before a STOP instruction is executed.

4.11.4.9 Bit counter bits (BC0, BC1 and BC2)

BC0, BC1 and BC2 should all be zero for normal I^2C-bus operation. The bit counter is always cleared by a START condition; thus all eight bits of the first byte are transferred.

If a non-zero bit counter value is chosen, it is only valid for one S0transfer since the counter decrements to zero. The bit counter is useful when a master receiver signals an end of transmission by sending a negative acknowledge after the last byte received; the last byte is received with ACK = logic 0 in register S2. The negative acknowledge is then issued by setting the bit counter to one and 'receiving' one bit from the HIGH level on the SDA line. The slave transmitter interprets the same signals as a negative acknowledgement.

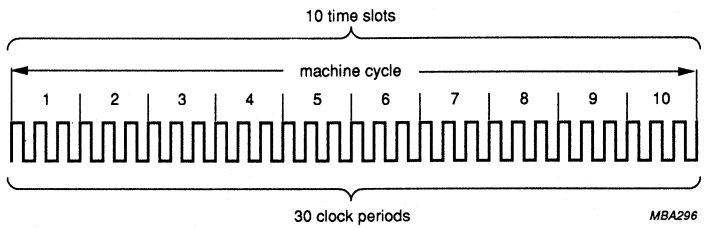


Fig.16 Machine cycle timing.

4.12 Timing

Every machine cycle consists of 10 time slots. Each time slot consists of 3 clock periods (see Fig.16).

The clock frequencies range is from 100 kHz to a maximum which is a function of supply voltage. When $V_{DD} \geq 4.5$ V, operation at 10 MHz is guaranteed.

The clock signal may be internally generated by the on-chip oscillator and an external crystal. Alternatively, an external clock may be applied to the XTAL1 pin.

4.13 Oscillator

The on-chip oscillator consists of an invertor stage including a feedback resistor and load capacitors (see Fig.17). A quartz crystal is usually connected between XTAL1 and XTAL2. Alternatively, a ceramic resonator or an inductor may be used as the timing element; however, external load capacitors should then be added for good frequency stability.

When the supply voltage drops below the power-on-reset level, the oscillator is inhibited. The internal oscillator may also be inhibited by the STOP instruction.

Oscillator start-up time depends on the external timing element. The start-up time of a quartz crystal is several milliseconds due to the narrow crystal bandwidth.

For proper oscillator start-up, the transconductance (gm) of the invertor stage must satisfy the following relationship (see Fig.17 and Fig.18):

$$4.2[R_1\omega^2(C_L + C_0 + C_f)^2 + 1/R_f] < gm < C_1C_2/[R_1(C_0 + C_f)^2 + 1/\omega^2R_f]$$

where:

R_1 = resonator series resistance
C_0 = static resonator capacitance
R_f = feedback resistor
C_L = $C_1C_2/[C_1 + C_2]$
C_f = parasitic feedback capacitance (typically 2 pF on-chip, external value depends on PC board wiring)
ω = $2\pi f_{XTAL}$

For more information on crystal oscillators and start-up conditions see the application note 'Crystal Oscillators for CMOS Circuits'.

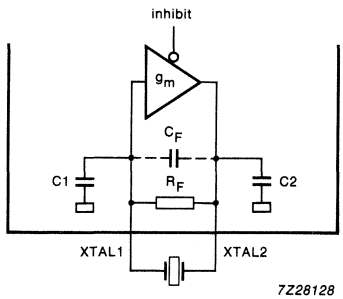


Fig.17 Oscillator with integrated elements.

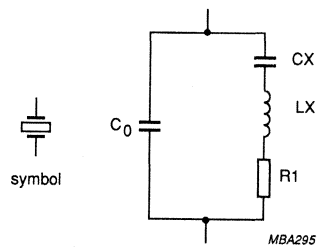


Fig.18 Crystal unit equivalent circuit.

4.14 Reset

After a falling edge on the internal reset, 1866 clock cycles are required to initialize the microcontroller to a defined state. The first instruction is then executed.

4.14.1 Passive reset

A passive reset is generated by the RC circuit shown in Fig.19. As V_{DD} rises, the discharged C_{reset} pulls the RESET pin close to V_{DD}. When V_{DD} crosses the power-on reference level V_{ref} (typically 1.5 V), the device generates a reset pulse of approximately 50 μs which helps to pull the RESET pin to V_{DD}. To ensure a correct reset, the RESET voltage should reach at least 70% of the final value of V_{DD} before C_{reset} charges through TR2 and R_{reset}. If the RESET voltage and V_{DD} rise exponentially, this requirement is satisfied when the time constant τ ($C_{reset}R_{reset}$) of the RESET pulse is greater than eight times the time constant of V_{DD}. If V_{DD} rises linearly, the requirement is satisfied when the time constant of the RESET pulse is greater than twice the time constant of V_{DD}.

In the event of a drop in the supply voltage, the diode rapidly discharges C_{reset}, ensuring reliable power-on-reset even after short supply voltage interruptions.

In battery-powered systems where V_{DD} quickly reaches its minimum operating value, passive reset can be performed without external components since the 50 μs reset pulse guarantees proper initialization.

4.14.2 Active reset

An active reset can be generated by driving the RESET pin HIGH with external logic. This pulse should be present until V_{DD} has reached its minimum operating value.

4.14.3 Reset state

After a reset, the microcontroller is initialized as follows: The program counter points to 00H. Memory bank 0, register bank 0, and stack pointer 0 (locations 8 and 9) are selected. All interrupts are disabled. The timer/event counter is stopped and cleared, the timer flag is cleared, and the timer prescaler is set to modulo 32 (PS = 0). All port flip-flops (except P2.3/SDA) are set to logic 1. P2.3/SDA and SCL are high impedance 30 clock pulses (max.) after the end of the internal reset pulse. The serial I/O interface is disabled (ESO = 0) and in the slave receiver mode 30 clock pulses (max.) after the end of internal reset pulse (S0, S0', S1 and S2 are cleared except when PIN = logic 1). The Idle and Stop modes are terminated.

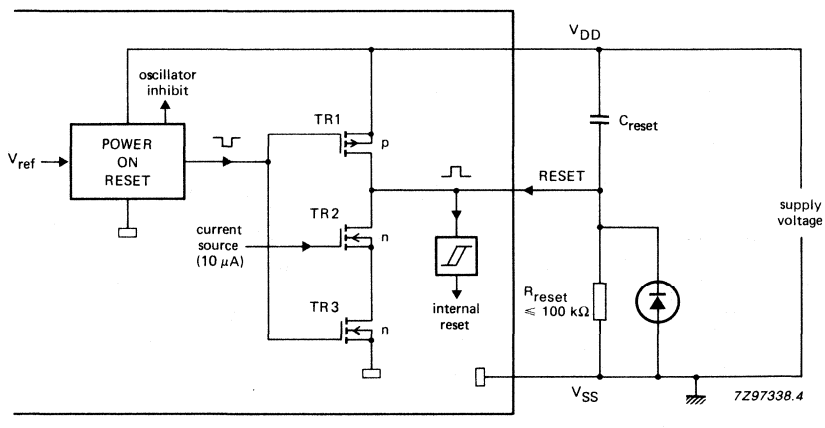


Fig.19 Passive power-on-reset.

4.15 Idle mode

The Idle mode is very useful in low power applications. When all computational tasks are completed, the device can be placed in the Idle mode instead of a power consuming waiting loop.

When the microcontroller enters the Idle mode by executing an IDLE instruction, all activity is halted except for the oscillator, the timer/event counter and the serial I/O interface(if available).

The Idle mode is terminated when an enabled interrupt (or reset) occurs. The interrupt routine is executed and program execution resumes at the instruction immediately following the IDLE instruction.

For timer/event counter interrupts and SIO/derivative interrupts, termination of the Idle mode is straightforward. However, care must be taken when the Idle mode is terminated by the external (chip enable) interrupt since CE/$\overline{T0}$ is rising-edge triggered. If CE/$\overline{T0}$ was HIGH prior to entering the Idle mode, it must go LOW before a rising edge can be generated. Fig.20 shows the exact timing for Idle mode termination with an external interrupt (CE/$\overline{T0}$).

If no interrupt is enabled, the Idle mode can only be terminated by an active signal on the RESET pin. A normal reset sequence is executed (Fig.20).

4.16 Stop mode

The Stop mode enables very low power operation. When all computational tasks are completed, the device can be virtually shut down by stopping the oscillator.

When the microcontroller enters the Stop mode by executing a STOP instruction, the oscillator is switched off. All internal states (CPU status, RAM) and I/O levels are maintained.

The Stop mode is terminated by a HIGH level on the CE/$\overline{T0}$ pin or a reset. In the latter case, a normal reset sequence is executed (see Fig.21).

Unlike the Idle mode, the microcontroller responds to a HIGH level on the CE/$\overline{T0}$ pin (i.e. not to a rising edge). If the CE/$\overline{T0}$ pin is HIGH when the STOP instruction is executed, the Stop mode will not be entered.

A rising edge on CE/$\overline{T0}$ causes program execution to continue after a delay of 1866 clock cycles. If the external interrupt is enabled, the microcontroller executes the instruction immediately following the STOP instruction before executing the interrupt routine. If the external interrupt is disabled, program execution continues with the instruction following the STOP instruction (see Fig.21).

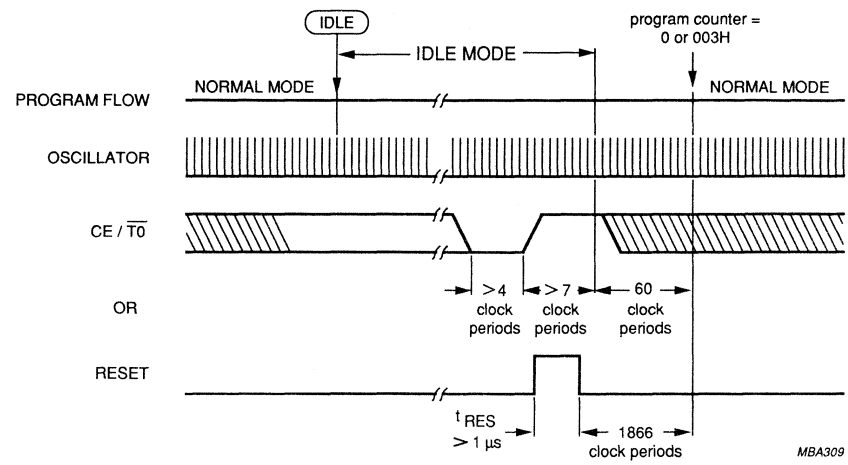


Fig.20 Entering and leaving the Idle mode.

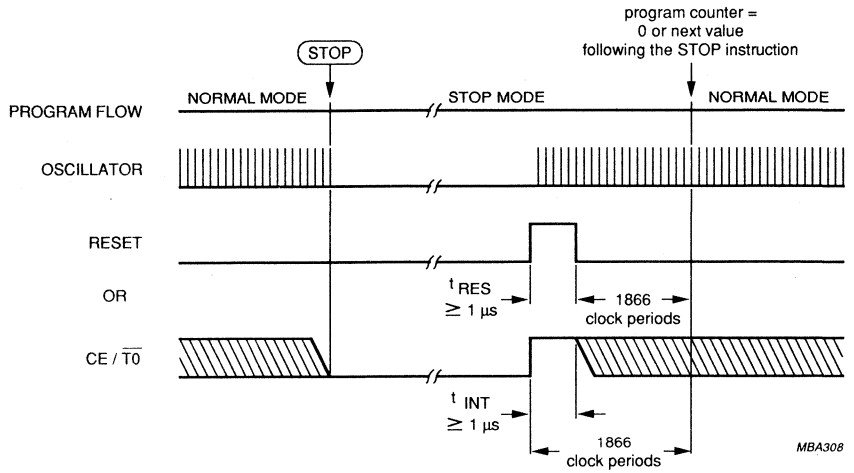


Fig.21 Entering and leaving the Stop mode.

4.17 Derivative logic

Several members of the PCD33XX family contain derivative logic. For specific information on a particular device, refer to the relevant data sheet.

The derivative registers are write only, read only or read/write (see Fig.22). They may be accessed internally via the derivative address register using the derivative input/output instructions (MOV A,Dx, MOV Dx,A, ANL Dx,A and ORL Dx,A).

Derivative interrupts share the PIN flag with the SIO interrupt (if available). When the derivative interrupt routine is executed, the PIN flag must be inactivated by software.

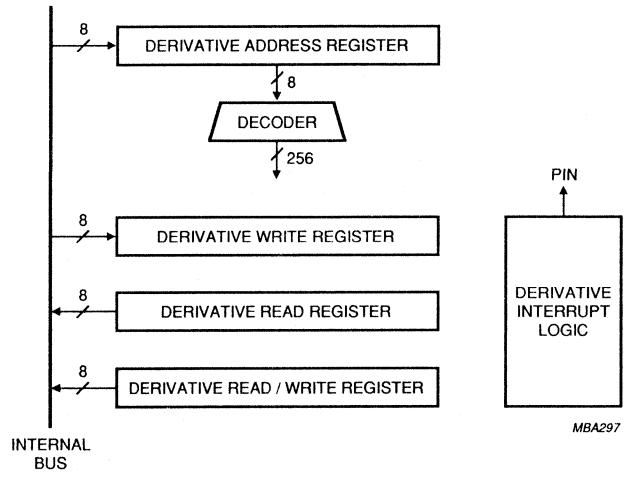


Fig.22 Block diagram of derivative logic.

5 INSTRUCTION SET

The PCD33XX family instruction set consists of over 80 one and two byte instructions. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 8 contains the instruction set of the PCD33XX. Figure 23 shows the instruction map and Table 7 describes the symbols that are used.

Table 7 Symbols and definitions.

SYMBOL	DESCRIPTION
A	accumulator
addr	program memory address
Bb	bit designation (b = 0 to 7)
C	carry bit (bit CY)
CNT	event counter
Dx	mnemonic derivative register (x = 0 to 255)
direct	8-bit derivative register address
data	8-bit immediate data
I	interrupt
MBn	memory bank (n = 0 to 3)
MBFFn	memory bank flip-flop (n = 0 or 1)
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1, or 2)
PS	Timer prescaler select
PSW	program status word
RB	register bank
RBS	register bank select flag
@Rr	8-bit address register (r = 0, 1)
Rr	8-bit register (r = 0 to 7)
Sn	serial I/O register (n = 0, 1, or 2)
SP	stack pointer
T	timer
TCNT	timer/event counter
TF	timer flag
T0, T1	test 0 and test 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with
< >	represents a hex digit

PCF84CXXX PCD33XX

first hexadecimal character of opcode — second hexadecimal character of opcode

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, #data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	IN A,Pp 1	IN A,Pp 2		MOV A,Sn 0	MOV A,Sn 1		
1	INC @ Rr 0	INC @ Rr 1	JB0 addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0	INC Rr 1	INC Rr 2	INC Rr 3	INC Rr 4	INC Rr 5	INC Rr 6	INC Rr 7
2	XCH A, @Rr 0	XCH A, @Rr 1	STOP	MOV A, #data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A,Rr 0	XCH A,Rr 1	XCH A,Rr 2	XCH A,Rr 3	XCH A,Rr 4	XCH A,Rr 5	XCH A,Rr 6	XCH A,Rr 7
3	XCHD A, @Rr 0	XCHD A, @Rr 1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A 0	OUTL Pp,A 1	OUTL Pp,A 2		MOV Sn,A 0	MOV Sn,A 1	MOV Sn,A 2	
4	ORL A, @Rr 0	ORL A, @Rr 1	MOV A, T	ORL A, #data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0	ORL A,Rr 1	ORL A,Rr 2	ORL A,Rr 3	ORL A,Rr 4	ORL A,Rr 5	ORL A,Rr 6	ORL A,Rr 7
5	ANL A, @Rr 0	ANL A, @Rr 1	JB2 addr	ANL A, #data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0	ANL A,Rr 1	ANL A,Rr 2	ANL A,Rr 3	ANL A,Rr 4	ANL A,Rr 5	ANL A,Rr 6	ANL A,Rr 7
6	ADD A, @Rr 0	ADD A, @Rr 1	MOV T, A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0	ADD A,Rr 1	ADD A,Rr 2	ADD A,Rr 3	ADD A,Rr 4	ADD A,Rr 5	ADD A,Rr 6	ADD A,Rr 7
7	ADDC A, @Rr 0	ADDC A, @Rr 1	JB3 addr		CALL page 3			RR A	ADDC A,Rr 0	ADDC A,Rr 1	ADDC A,Rr 2	ADDC A,Rr 3	ADDC A,Rr 4	ADDC A,Rr 5	ADDC A,Rr 6	ADDC A,Rr 7
8				RET	JMP page 4	EN SI			ORL Pp,#data 0	ORL Pp,#data 1	ORL Pp,#data 2		MOV A,Dx	MOV Dx,A	ANL Dx,A	ORL Dx,A
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data 0	ANL Pp,#data 1	ANL Pp,#data 2		MOV Sn,#data 0	MOV Sn,#data 1	MOV Sn,#data 2	
A	MOV @ Rr,A 0	MOV @ Rr,A 1		MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0	MOV Rr,A 1	MOV Rr,A 2	MOV Rr,A 3	MOV Rr,A 4	MOV Rr,A 5	MOV Rr,A 6	MOV Rr,A 7
B	MOV @Rr, #data 0	MOV @Rr, #data 1	JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data 0	MOV Rr,#data 1	MOV Rr,#data 2	MOV Rr,#data 3	MOV Rr,#data 4	MOV Rr,#data 5	MOV Rr,#data 6	MOV Rr,#data 7
C	DEC @Rr 0	DEC @Rr 1			JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr 0	DEC Rr 1	DEC Rr 2	DEC Rr 3	DEC Rr 4	DEC Rr 5	DEC Rr 6	DEC Rr 7
D	XRL A, @Rr 0	XRL A, @Rr 1	JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr 0	XRL A,Rr 1	XRL A,Rr 2	XRL A,Rr 3	XRL A,Rr 4	XRL A,Rr 5	XRL A,Rr 6	XRL A,Rr 7
E	DJNZ @ Rr,addr 0	DJNZ @ Rr,addr 1			JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr,addr 0	DJNZ Rr,addr 1	DJNZ Rr,addr 2	DJNZ Rr,addr 3	DJNZ Rr,addr 4	DJNZ Rr,addr 5	DJNZ Rr,addr 6	DJNZ Rr,addr 7
F	MOV A, @Rr 0	MOV A, @Rr 1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0	MOV A,Rr 1	MOV A,Rr 2	MOV A,Rr 3	MOV A,Rr 4	MOV A,Rr 5	MOV A,Rr 6	MOV A,Rr 7

MBA281

Fig.23 PCD33XX instruction map.

Table 8 PCD33XX family instruction set.

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION		NOTES
ACCUMULATOR						
ADD A, Rr	6<8 + r>	1/1	Add register contents to A	(A) ← (A) + (Rr)	r = 0 to 7	1
ADD A, @Rr	6r	1/1	Add RAM data, addressed by Rr, to A	(A) ← (A) + ((Rr))	r = 0, 1	1
ADD A, #data	03 data	2/2	Add immediate data to A	(A) ← (A) + data		1
ADDC A, Rr	7<8 + r>	1/1	Add carry and register contents to A	(A) ← (A) + (Rr) + (C)	r = 0 to 7	1
ADDC A, @Rr	7r	1/1	Add carry and RAM data, addressed by Rr, to A	(A) ← (A) + ((Rr)) + (C)	r = 0, 1	1
ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A) ← (A) + data + (C)		1
ANL A, Rr	5<8 + r>	1/1	'AND' Rr with A	(A) ← (A) AND (Rr)	r = 0 to 7	
ANL A, @Rr	5r	1/1	'AND' RAM data, addressed by Rr, with A	(A) ← (A) AND ((Rr))	r = 0, 1	
ANL A, #data	53 data	2/2	'AND' immediate data with A	(A) ← (A) AND data		
ORL A, Rr	4<8 + r>	1/1	'OR' Rr with A	(A) ← (A) OR (Rr)	r = 0 to 7	
ORL A, @Rr	4r	1/1	'OR' RAM data, addressed by Rr, with A	(A) ← (A) OR ((Rr))	r = 0, 1	
ORL A, #data	43 data	2/2	'OR' immediate data with A	(A) ← (A) OR data		
XRL A, Rr	D<8 + r>	1/1	'XOR' Rr with A	(A) ← (A) XOR (Rr)	r = 0 to 7	
XRL A, @Rr	Dr	1/1	'XOR' RAM data, addressed by Rr, with A	(A) ← (A) XOR ((Rr))	r = 0, 1	
XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A) ← (A) XOR data		
INC A	17	1/1	Increment A by 1	(A) ← (A) + 1		
DEC A	07	1/1	Decrement A by 1	(A) ← (A) – 1		
CLR A	27	1/1	Clear A to zero	(A) ← 0		
CPL A	37	1/1	One's complement A	(A) ← NOT(A)		
RL A	E7	1/1	Rotate A left	$(A_{n+1}) \leftarrow (A_n)$ $(A_0) \leftarrow (A_7)$	n = 0 to 6	
RLC A	F7	1/1	Rotate A left through carry	$(A_{n+1}) \leftarrow A_n$ $(A_0) \leftarrow (C), (C) \leftarrow (A_7)$	n = 0 to 6	2
RR A	77	1/1	Rotate A right	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (A_0)$	n = 0 to 6	
RRC A	67	1/1	Rotate A right through carry	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (C), (C) \leftarrow (A_0)$	n = 0 to 6	2
DA A	57	1/1	Decimal adjust A	(A) ← (A) + 06H if AC = 1 or $(A_{0-3}) > 9$; (A) ← (A) + 60H if $(A_{4-7}) > 9$		2
SWAP A	47	1/1	Swap nibbles of A	$(A_{4-7}) \leftrightarrow (A_{0-3})$		2

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION		NOTES
DATA MOVES						
MOV A, Rr	F<8 + r>	1/1	Move register contents to A	(A) ← (Rr)	r = 0 to 7	
MOV A, @Rr	Fr	1/1	Move RAM data, addressed by Rr, to A	(A) ← ((Rr))	r = 0, 1	
MOV A, #data	23 data	2/2	Move immediate data to A	(A) ← data		
MOV Rr, A	A<8 + r>	1/1	Move accumulator contents to register	(Rr) ← (A)	r = 0 to 7	
MOV @Rr, A	Ar	1/1	Move accumulator contents to RAM location addressed by Rr	((Rr)) ← (A)	r = 0, 1	
MOV Rr, #data	B<8 + r> data	2/2	Move immediate data to Rr	(Rr) ← data	r = 0 to 7	
MOV @Rr, #data	Br data	2/2	Move immediate data to RAM location addressed by Rr	((R0)) ← data	r = 0, 1	
XCH A, Rr	2<8 + r>	1/1	Exchange accumulator contents with Rr	(A) ↔ (Rr)	r = 0 to 7	
XCH A, @Rr	2r	1/1	Exchange accumulator contents with RAM data addressed by Rr	(A) ↔ ((Rr))	r = 0, 1	
XCHD A, @Rr	3r	1/1	Exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3}) \leftrightarrow ((Rr_{0-3}))$	r = 0, 1	
MOV A, PSW	C7	1/1	Move PSW contents to accumulator	(A) ← (PSW)		
MOV PSW, A	D7	1/1	Move accumulator bit 3 to PSW_3 (PS)	(PS) ← (A_3)		3
MOVP A, @A	A3	1/2	Move indirectly addressed data in current page to A	(PC_{0-7}) ← (A), (A) ← ((PC))		
CARRY FLAG						
CLR C	97	1/1	Clear carry bit	(C) ← 0		2
CPL C	A7	1/1	Complement carry bit	(C) ← NOT(C)		2
REGISTER						
INC Rr	1<8 + r>	1/1	Increment register by 1	(Rr) ← (Rr) + 1	r = 0 to 7	
INC @Rr	1r	1/1	Increment RAM data, addressed by Rr, by 1	((Rr)) ← ((Rr)) + 1	r = 0, 1	
DEC Rr	C<8 + r>	1/1	Decrement register by 1	(Rr) ← (Rr) – 1	r = 0 to 7	
DEC @Rr	Cr	1/1	Decrement RAM data, addressed by Rr, by 1	((Rr)) ← ((Rr)) – 1	r = 0, 1	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION		NOTES
BRANCH						
JMP addr	<2n>4 addr	2/2	Unconditional jump within a 2 K bank	$(PC_{8-10}) \leftarrow n$ $(PC_{0-7}) \leftarrow$ addr $(PC_{11-12}) \leftarrow$ (MBFF 0-1)	n = 0 to 7	
JMPP @A	B3	1/2	Indirect jump within a page	$(PC_{0-7}) \leftarrow ((A))$		
DJZN Rr, addr	E<8 + r> addr	2/2	Decrement Rr by 1 and jump if not zero to addr	(Rr) ← (Rr) – 1; if (Rr) not zero, then $(PC_{0-7}) \leftarrow$ addr	r = 0 to 7	
DJNZ @Rr, addr	Er	2/2	Decrement RAM data, addressed by Rr, by 1 and jump if not zero to addr	((Rr)) ← ((Rr)) – 1; if ((Rr)) not zero, then $(PC_{0-7}) \leftarrow$ addr	r = 0, 1	
JBb addr	<2b + 1>2 addr	2/2	Jump to addr if Accumulator bit b = 1	If $(A_b) = 1$, then $(PC_{0-7}) \leftarrow$ addr	b = 0 to 7	
JC addr	F6 addr	2/2	Jump to addr if C = 1	If (C) = 1, then $(PC_{0-7}) \leftarrow$ addr		
JNC addr	E6 addr	2/2	Jump to addr if C = 0	If (C) = 0, then $(PC_{0-7}) \leftarrow$ addr		
JZ addr	C6 addr	2/2	Jump to addr if A = 0	If (A) = 0, then $(PC_{0-7}) \leftarrow$ addr		
JNZ addr	96 addr	2/2	Jump to addr if A is NOT zero	If (A) ≠ 0, then $(PC_{0-7}) \leftarrow$ addr		
JT0 addr	36 addr	2/2	Jump to addr if T0 = 1	If T0 = 1, then $(PC_{0-7}) \leftarrow$ addr		
JNT0 addr	26 addr	2/2	Jump to addr if T0 = 0	If T0 = 0: $(PC_{0-7}) \leftarrow$ addr		
JT1 addr	56 addr	2/2	Jump to addr if T1 = 1	If T1 = 1: $(PC_{0-7}) \leftarrow$ addr		
JNT1 addr	46 addr	2/2	Jump to addr if T1 = 0	If T1 = 0: $(PC_{0-7}) \leftarrow$ addr		
JTF addr	16 addr	2/2	Jump to addr if Timer Flag = 1	If TF = 1: $(PC_{0-7}) \leftarrow$ addr		4
JNTF addr	06 addr	2/2	Jump to addr if Timer Flag = 0	If TF = 0: $(PC_{0-7}) \leftarrow$ addr		4
TIMER/EVENT COUNTER						
MOV A, T	42	1/1	Move timer/event counter contents to accumulator	(A) ← (T)		
MOV T, A	62	1/1	Move accumulator contents to timer/event counter	(T) ← (A)		
STRT CNT	45	1/1	Start event counter			
STRT T	55	1/1	Start timer			
STOP TCNT	65	1/1	Stop timer/event counter			
EN TCNTI	25	1/1	Enable timer/event counter interrupt			
DIS TCNTI	35	1/1	Disable timer/event counter interrupt			

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION		NOTES
CONTROL						
EN I	05	1/1	Enable external (chip enable) interrupt			
DIS I	15	1/1	Disable external (chip enable) interrupt			
SEL RB0	C5	1/1	Select register bank 0	(RBS) ← 0		5
SEL RB1	D5	1/1	Select register bank 1	(RBS) ← 1		5
SEL MB0	E5	1/1	Select program memory bank 0	(MBFF0) ← 0, (MBFF1) ← 0		10
SEL MB1	F5	1/1	Select program memory bank 1	(MBFF0) ← 1, (MBFF1) ← 0		10
SEL MB2	A5	1/1	Select program memory bank 2	(MBFF0) ← 0, (MBFF1) ← 1		10
SEL MB3	B5	1/1	Select program memory bank 3	(MBFF0) ← 1, (MBFF1) ← 1		10
STOP	22	1/1	Enter Stop mode			
IDLE	01	1/1	Enter Idle mode			
SUBROUTINE						
CALL addr	<2n + 1>4 addr	2/2	Jump to subroutine	((SP)) ← (PC), ($PSW_{4, 6, 7}$) (SP) ← (SP) + 1 (PC_{8-10}) ← n (PC_{0-7}) ← addr (PC_{11-12}) ← (MBFF0-1)	n = 0 to 7	6
RET	83	1/2	Return from subroutine	(SP) ← (SP) - 1 (PC) ← ((SP))		6
RETR	93	1/2	Return from interrupt and restore bits 4, 6, 7 of PSW	(SP) ← (SP) - 1 ($PSW_{4, 6, 7}$) + (PC) ← ((SP))		6
PARALLEL INPUT/OUTPUT						
IN A, Pp	08 09 0A	1/2	Input port p data to accumulator	(A) ← (P0) (A) ← (P1) (A) ← (P2)		7
OUTL Pp, A	38 39 3A	1/2	Output accumulator data to port p	(P0) ← (A) (P1) ← (A) (P2) ← (A)		
ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p with immediate data	(P0) ← (P0) AND data (P1) ← (P1) AND data (P2) ← (P2) AND data		
ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0) ← (P0) OR data (P1) ← (P1) OR data (P2) ← (P2) OR data		
DERIVATIVE INPUT/OUTPUT						
MOV A, Dx	8C direct	2/2	Move derivative register contents to accumulator	(A) ← (Dx)	x = 0 to 255	8
MOV Dx, A	8D direct	2/2	Move accumulator contents to derivative register	(Dx) ← (A)	x = 0 to 255	8
ANL Dx, A	8E direct	2/2	AND derivative register with accumulator	(Dx) ← (Dx) AND (A)	x = 0 to 255	8
ORL Dx, A	8F direct	2/2	OR derivative register with accumulator	(Dx) ← (Dx) OR (A)	x = 0 to 255	8

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION		NOTES
SERIAL INPUT/OUTPUT						
MOV A, S_n	0C 0D	1/2	Move serial I/O register contents to accumulator	(A) ← (S0) (A) ← (S1)	n = 0, 1	
MOV S_n, A	3C 3D 3E	1/2	Move accumulator contents to serial I/O register	(S0) ← (A) (S1) ← (A) (S2) ← (A)	n = 0, 1, 2	
MOV S_n, #data	9C data 9D data 9E data	2/2	Move immediate data to serial I/O register	(S0) ← data (S1) ← data (S2) ← data	n = 0, 1, 2	
EN SI	85	1/1	Enable serial I/O interrupt			
DIS SI	95	1/1	Disable serial I/O interrupt			
NOP	00	1/1	No operation	(PC_{0-10}) ← (PC_{0-10}) + 1		

Notes

1. PSW CY, AC affected.
2. PSW CY affected.
3. PSW PS affected.
4. Execution of a JTF or JNTF instruction resets the Timer Flag (TF).
5. PSW RBS affected.
6. PSW SP_0, SP_1, SP_2 affected.
7. (A) = 0000, P2.3, P2.2, P2.1, P2.0
8. For more information on the derivative input/output instructions of a particular microcontroller, consult the specific microcontroller data sheet.
9. (S1) has a different meaning for read and write operations. See section 4.11.4.
10. SEL MB instructions may not be used within interrupt routines.

6 LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Supply voltage range	−0.8	8.0	V
V_I	All input voltages	−0.5	V_{DD} + 0.5	V
I_I, I_O	DC current into any input or output	-	10	mA
P_{tot}	Total power dissipation	-	125	mW
T_{stg}	Storage temperature range	−65	150	°C
T_{amb}	Operating ambient temperature range	−20	70	°C
T_j	Operating junction temperature	-	90	°C

7 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

8 DC CHARATERISTICS

V_{DD} = 1.8 V to 6 V; V_{SS} = 0 V; T_{amb} = −20 to 70 °C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	Operating supply voltage range	See Fig.24.	1.8	-	6.0	V
I_{DD}	Operating supply current	See Fig.26, Fig.27, and note 1; at V_{DD} = 5 V; f_{XTAL} = 10 MHz at V_{DD} = 5 V; f_{XTAL} = 6 MHz at V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	 - - -	 1.6 1.0 0.3	 3.2 2.0 0.8	 mA mA mA
I_{DD}	Idle mode supply current	See Fig.28, Fig.29, and note 1; at V_{DD} = 5 V; f_{XTAL} = 10 MHz at V_{DD} = 5 V; f_{XTAL} = 6 MHz at V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	 - - -	 0.8 0.5 0.15	 1.6 1.0 0.4	 mA mA mA
IDD	Stop mode supply current	See Fig.25, note 1, and note 2; at V_{DD} = 2.5 V; T_{amb} = 25 °C at V_{DD} = 2.5 V; T_{amb} = 85 °C	 - -	 1.2 -	 2.5 10.0	 µA µA
Inputs						
V_{IL}	Input voltage LOW		0	-	$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH		$0.7V_{DD}$	-	V_{DD}	V
$\pm I_{IL}$	Input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	-	-	1	µA
Outputs						
I_{OL}	Output sink current	All outputs except SCL, P2.3/SDA; see Fig.30. at V_{DD} = 5 V ± 10%; V_O = 0.4 V	 1.6	 3.0	 -	 mA
I_{OL}	Output sink current	SCL, P2.3/SDA; see Fig.31. at V_{DD} = 5 V ± 10%; V_O = 0.4 V	 3.0	 5.5	 -	 mA
$-I_{OH}$	Output source current	See Fig.32. at V_{DD} = 5 V ± 10%; V_O = $0.7V_{DD}$ at V_{DD} = 5 V ± 10%; V_O = V_{SS}	 40 -	 - -	 - 400	 µA µA
$-I_{OH}$	Output source current	See Fig.33. at V_{DD} = 5 V ± 10%; V_O = V_{DD} − 0.4 V	 1.6	 3.0	 -	 mA

9 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −20 to 70 °C. All voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_R	Rise time all outputs	See note 3.	-	30	-	ns
t_F	Fall time all outputs	See note 3.	-	30	-	ns
f_{XTAL}	Clock frequency	See Fig.24.	0.45	-	10.0	MHz

10 SERIAL I/O INTERFACE CHARACTERISTICS

See Fig.34, Fig.35 and note 4.

SYMBOL	PARAMETER	CONDITIONS	SCL INPUT	SCL OUTPUT
$t_{HD;STA}$	START condition hold time		$\geq 14/f_{XTAL}$	$(DF+9)/(2f_{XTAL})$
t_{LOW}	SCL LOW time	Note 5.	$\geq 17/f_{XTAL}$	$(DF-3)/(2f_{XTAL})$
t_{HIGH}	SCL HIGH time	Note 5.	$\geq 17/f_{XTAL}$	$(DF+3)/(2f_{XTAL})$
t_{RC}	SCL rise time	Note 6.	≤ 1 µs	≤ 1 µs
t_{FC}	SCL fall time	Note 7.	≤ 0.3 µs	≤ 0.1 µs
SYMBOL	**PARAMETER**	**CONDITIONS**	**P2.3/SDA INPUT**	**P2.3/SDA OUTPUT**
t_{BUF}	Bus free time	Note 8.	$\geq 14/f_{XTAL}$	≥ 4.7 µs
$t_{SU;DAT}$	Data set-up time	Note 9.	≥ 250 ns	$\geq 15/f_{XTAL}$
$t_{HD;DAT}$	Data hold time		> 0	$\geq 9/f_{XTAL}$
t_{RD}	SDA rise time	Note 6.	≤ 1 µs	≤ 1 µs
t_{FD}	SDA fall time	Note 7.	≤ 0.3 µs	≤ 0.1 µs
$t_{SU;STO}$	Stop condition set-up time		$\geq 14/f_{XTAL}$	$(DF-3)/(2f_{XTAL})$

Notes

1. $V_{IL} = 0$; $V_{IH} = V_{DD}$; open drain outputs connected to V_{SS}; all other outputs open.
2. Crystal connected between XTAL1 and XTAL2; pin T1 at V_{SS}; pin CE/$\overline{T0}$ at V_{SS}.
3. $V_{DD} = 5$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF.
4. DF is the f_{XTAL} divisor (see Table 2).
5. Values given for ASC = 0; for ASC = 1, $t_{LOW} = (DF-3)/4f_{XTAL}$, $t_{HIGH} = 3(DF+1)/4f_{XTAL}$.
6. Determined by the I^2C-bus capacitance (C_b) and the external pull-up resistor.
7. At maximum allowed I^2C-bus capacitance $C_b = 400$ pF.
8. Determined by program.
9. Independently of ASC, if $t_{LOW} \leq 24/f_{XTAL}$, $t_{SU;DAT} \geq t_{LOW} - 9/f_{XTAL}$.

11 CHARACTERISTIC CURVES

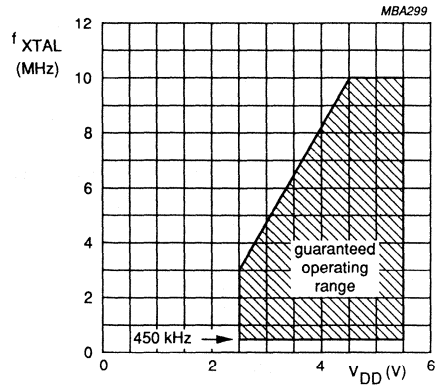
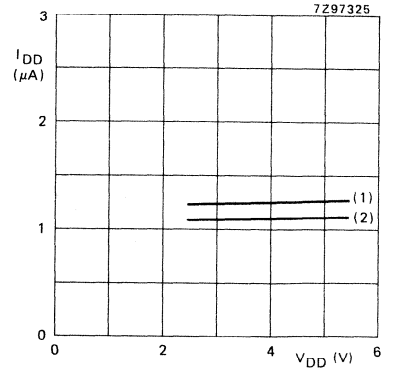
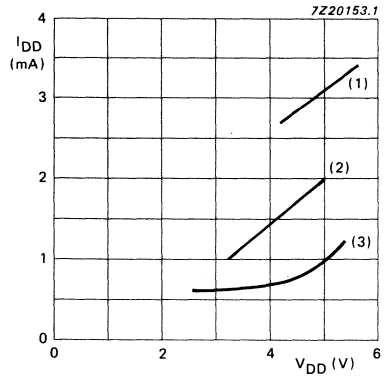


Fig.24 Maximum clock frequency (f_{XTAL}) as a function of supply voltage (V_{DD}).



(1) T_{amb} = 85° C
(2) T_{amb} = 25° C

Fig.25 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).



(1) f_{XTAL} = 10.0 MHz
(2) f_{XTAL} = 6.0 MHz
(3) f_{XTAL} = 3.58 MHz

Fig.26 Maximum operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).

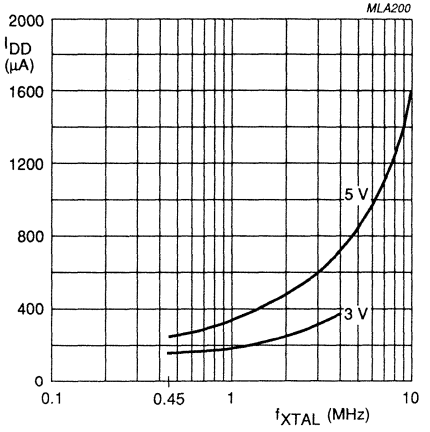
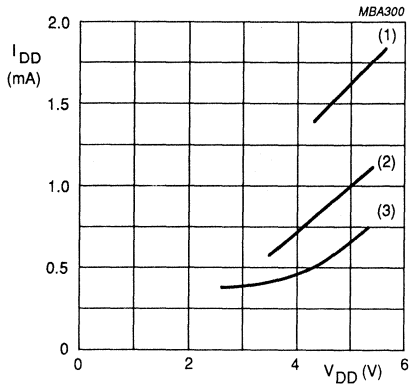


Fig.27 Typical operating supply current (I_{DD}) as a function of frequency at V_{DD} = 3 V and V_{DD} = 5 V.



(1) f_{XTAL} = 10.0 MHz
(2) f_{XTAL} = 6.0 MHz
(3) f_{XTAL} = 3.58 MHz

Fig.28 Maximum supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).

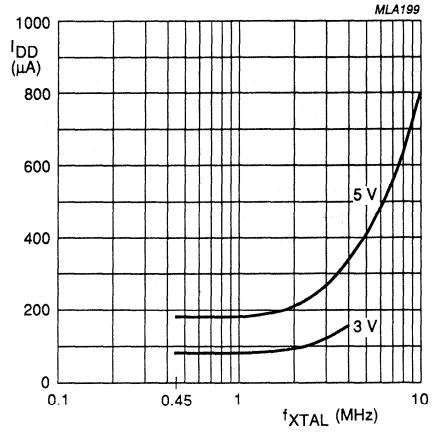


Fig.29 Typical supply current (I_{DD}) in Idle mode as a function of frequency at V_{DD} = 3 V and V_{DD} = 5 V.

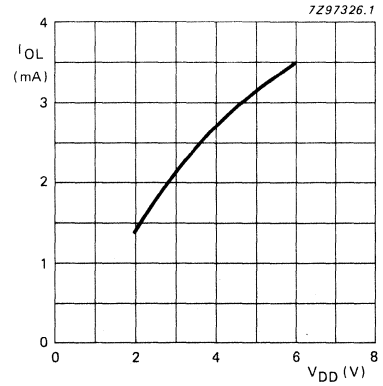


Fig.30 Typical output sink current (I_{OL}) as a function of supply voltage (V_{DD}); V_O = 0.4 V.

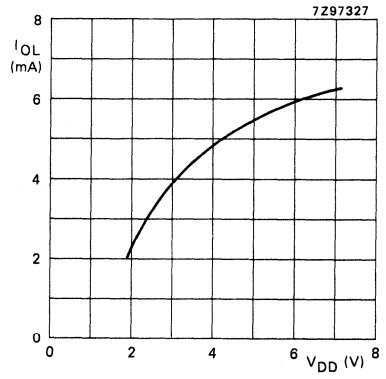
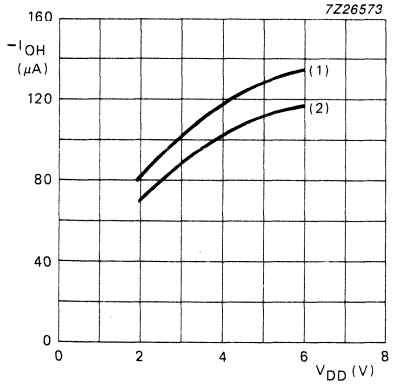


Fig.31 Typical output sink current (I_{OL}), outputs P2.3/SDA and SCL as a function of supply voltage (V_{DD}); V_O = 0.4 V.



(1) $V_O = V_{SS}$
(2) $V_O = 0.7\ V_{DD}$

Fig.32 Typical output source current ($-I_{OH}$) as a function of supply voltage (V_{DD}).

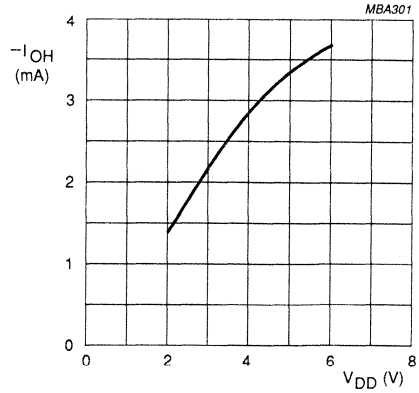


Fig.33 Typical push-pull output source current ($-I_{OH}$) as a function of supply voltage (V_{DD}); $V_O = V_{DD} - 0.4$ V.

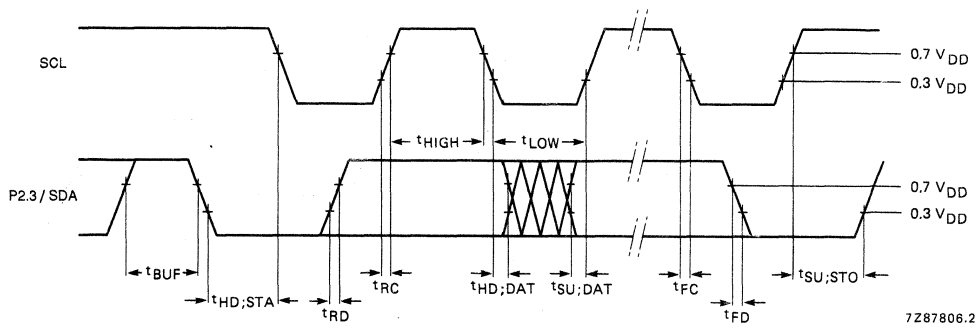


Fig.34 Slave SCL and receiver P2.3/SDA timing (SCL and P2.3/SDA input).

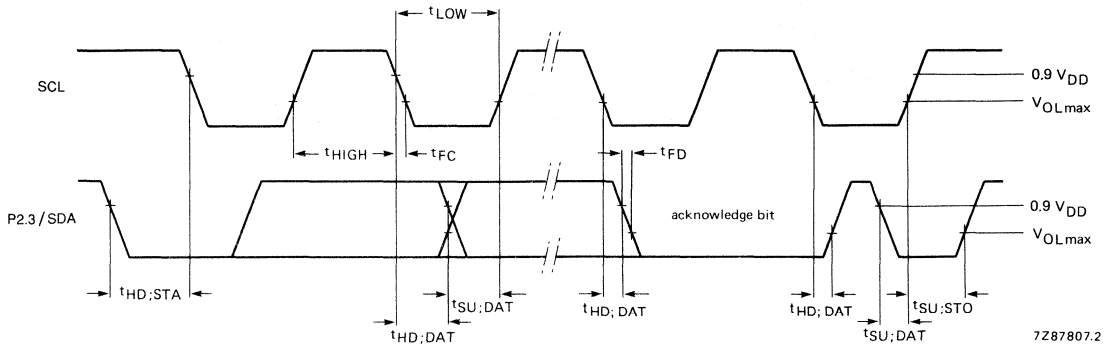


Fig.35 Master SCL and transmitter P2.3/SDA timing (SCL and P2.3/SDA output).

CMOS MICROCONTROLLER FOR TELEPHONE SETS

GENERAL DESCRIPTION

The PCD3343 is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD33XX family. It has special on-chip features for application in telephone sets.
The device is mask programmable, designed to provide telephone dialling facilities such as redial, repertory dial, emergency call, keyboard scan and control for liquid crystal display, pulse dial and/or DTMF dial via dedicated peripheral. For further detailed information, see PCD33XX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 3 K ROM bytes
- 224 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O which can be used in bus systems with more than one master (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles
- Clock frequency 100 kHz to 10 MHz
- Single supply voltage from 1,8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals (e.g. PCD3312 DTMF generator)
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3343P: 28-lead DIL; plastic (SOT117).
PCD3343T: 28-lead mini-pack; plastic (SO28; SOT136A).

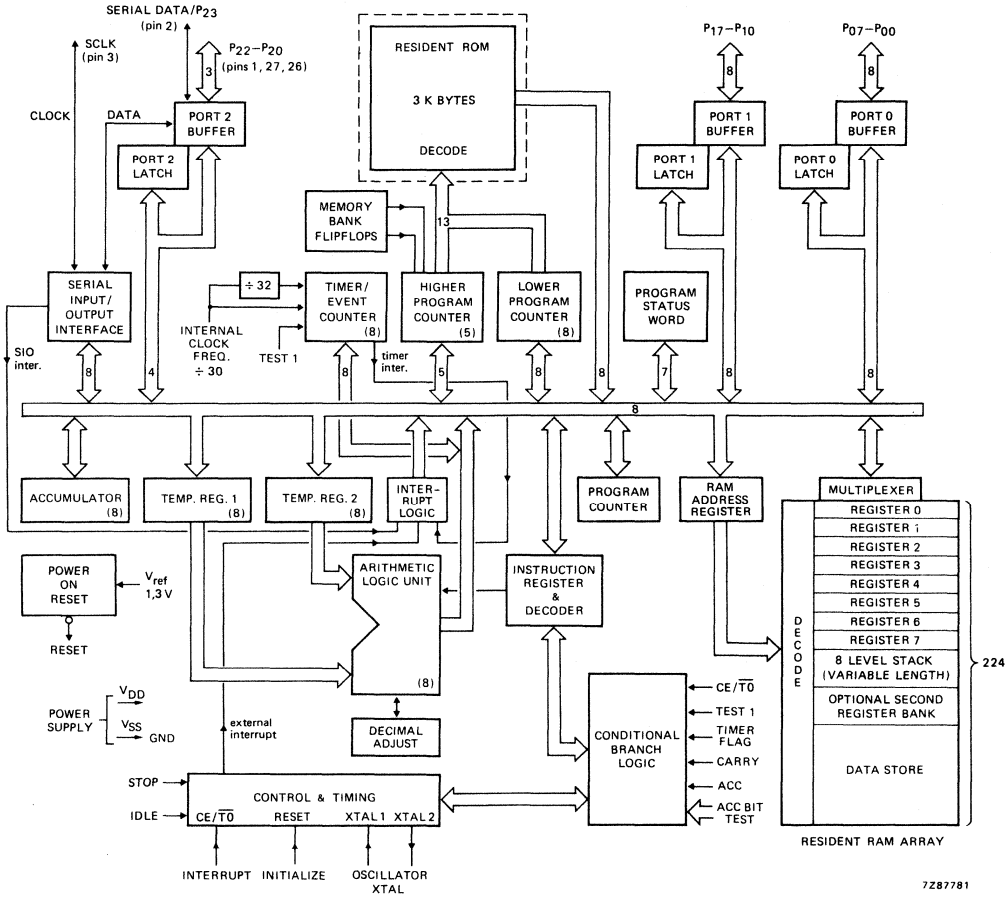
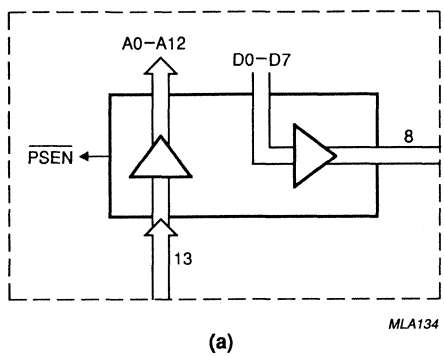


Fig. 1 Block diagram; PCD3343.

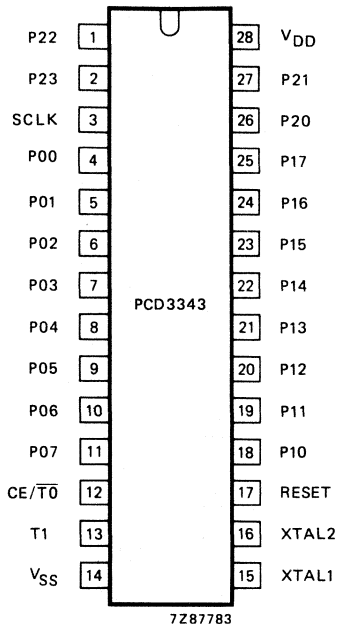


(a)

Fig. 1a Replacement of dotted part in Fig. 1, for the PCD3301B

DEVELOPMENT DATA

PINNING



Note CE/$\overline{T0}$ is labelled $\overline{INT}$/T0 on the PCD3301B and has inverted polarity.

Fig. 2 Pinning diagram: PCD3343 and bottom pinning PCD3301B.

PIN DESIGNATION

3	SCLK	**Clock**: bidirectional clock for serial I/O.
4-11	P00-P07	**Port 0**: 8-bit quasi-bidirectional I/O port.
12	CE/$\overline{T0}$	**Interrupt/Test 0**: external interrupt input (sensitive to positive-going edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
13	T1	**Test 1**: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
14	V_{SS}	**Ground**: circuit earth potential.
15	XTAL 1	**Crystal input**: connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
16	XTAL 2	connection to the other side of the timing component.
17	RESET	**Reset input**: used to initialize the processor (active HIGH), or output of power-on-reset circuit.
18-25	P10-P17	**Port 1**: 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P20-P23	**Port 2**: 4-bit quasi-bidirectional I/O port. P23 is the serial data input/output in serial I/O mode.
28	V_{DD}	**Power supply**: 1,8 V to 6 V.

PINNING (continued)

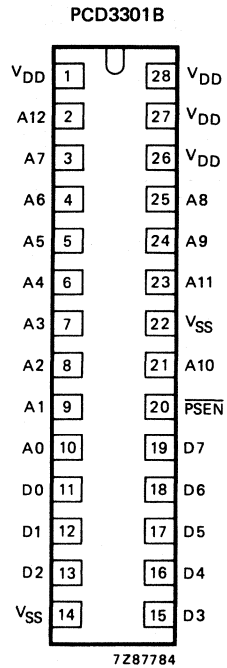


Fig. 3 Pinning diagram: PCD3301B 'Piggy-back' version top pinning; to access a 2732 or 2764 EPROM.

PIN DESIGNATION

14, 22	V_{SS}	**Ground**
1, 26-28	V_{DD}	**Power supply**
10-3, 25, 24, 21, 23, 2	A0-A12	**Address outputs**
11-13, 15-19	D0-D7	**Data**
20	$\overline{PSEN}$	**Program store enable**

Notes

1. RAM capacity of PCD3301B is 256 bytes.
2. Access time for ROMS/EPROMS to be below 7 x $1/f_{XTAL}$.
3. Pin 12 CE/$\overline{T0}$ is on the PCD3301B, inverted and labelled $\overline{INT}$/T0.

FUNCTIONAL DESCRIPTION

'Piggy-back' version PCD3301B

The PCD3301B is a special package that has standard pinning to the bottom which facilitates insertion as a mask-programmed device. An EPROM can be mounted on top in an additional socket. The total package height is greater than the standard DIL package. The RAM has 256 bytes and can also address 8 K bytes of program memory.

Program memory PCD3343

The program memory consists of 3072 bytes (8-bit words), in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 4 shows the program memory map.

Four program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine,
- Location 5; contains the first byte of a serial I/O interrupt service subroutine,
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using the unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory PCD3343

Data memory consists of 224 bytes (8-bit words), random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 5 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

FUNCTIONAL DESCRIPTION (continued)

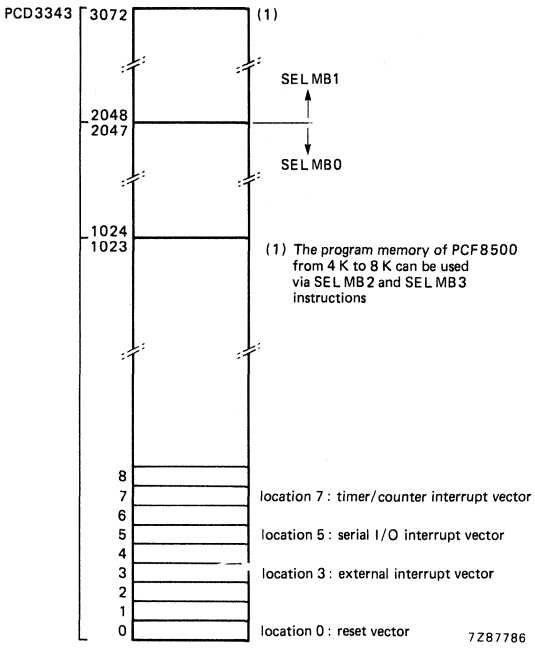


Fig. 4 Program memory map.

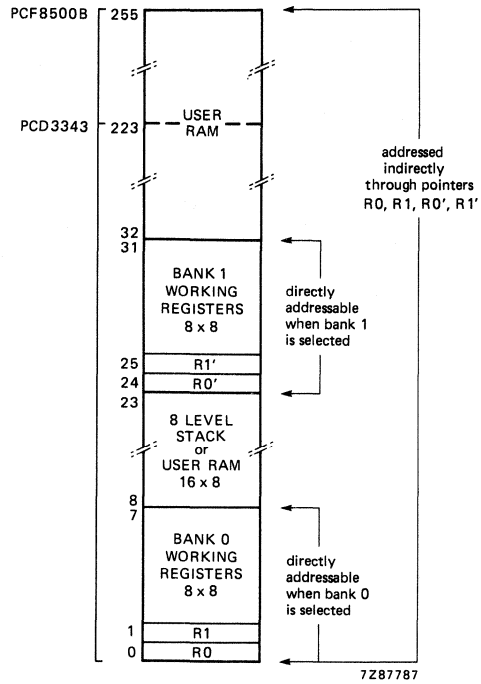


Fig. 5 Data memory map.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 6) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with next generated return address.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations. Possible locations from 32 to 223 may be used for storage of program variables or data.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

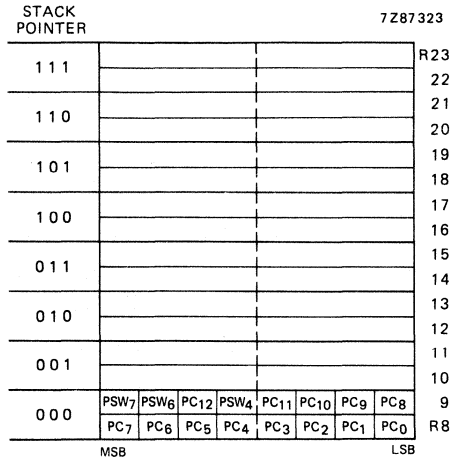


Fig. 6 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (H'01') the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode by one of three interrupts if they are enabled or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 7).

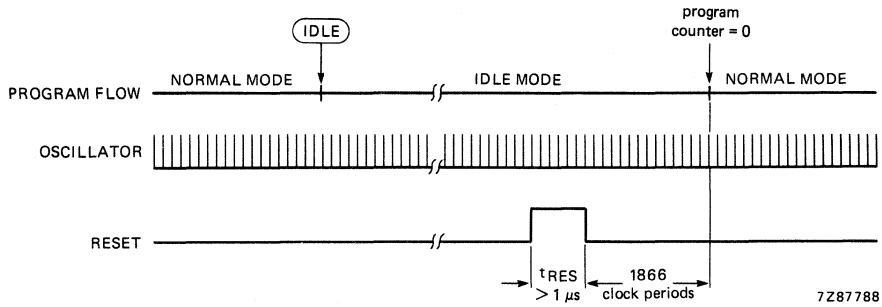


Fig. 7 Exit from IDLE mode via a RESET.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A LOW-to-HIGH transition on the external interrupt pin (CE/$\overline{T0}$) reactivates the microcontroller. A HIGH level applied to CE/$\overline{T0}$ will reactivate the microcontroller only in the STOP mode. Thus, if CE/$\overline{T0}$ was HIGH before the microcontroller entered the IDLE mode, it must go LOW before the microcontroller can be reactivated (see Fig. 8).

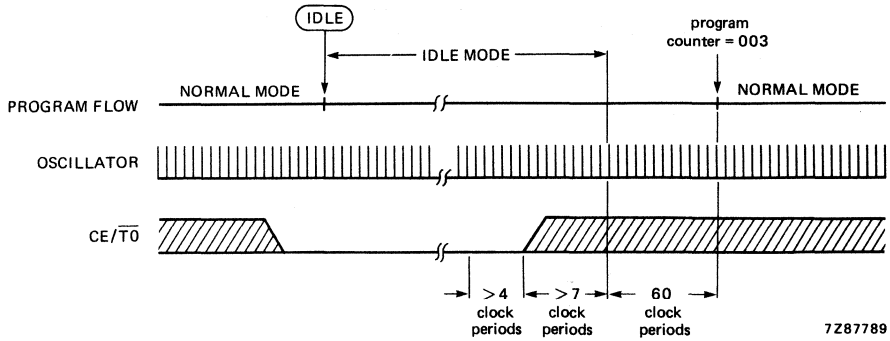


Fig. 8 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when CE/$\overline{T0}$ is LOW for 4 CP (clock periods) followed by a HIGH for 7 CP. After the initial forced CALL H'003' operation (60 CP) the program continues with the external interrupt service routine.

STOP mode

The microcontroller enters the STOP mode by the STOP instruction (H'22'). The oscillator is switched off. The internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 9).

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

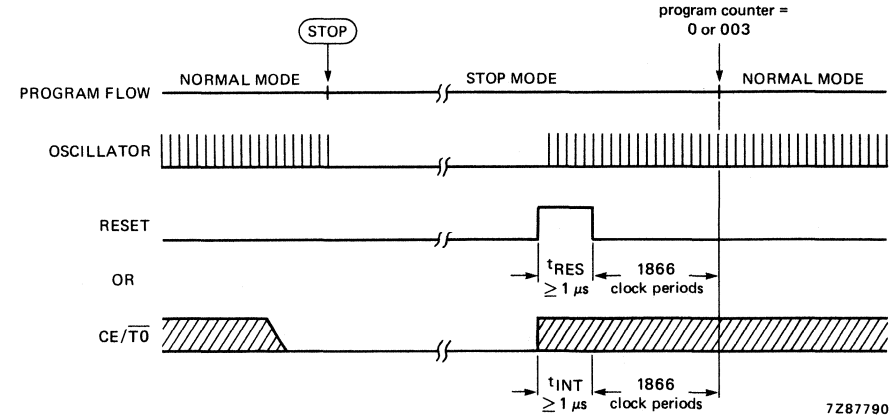


Fig. 9 Entering and exiting the STOP mode.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin HIGH, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a HIGH level applied at the CE/$\overline{T0}$ pin, and not by a LOW-to-HIGH transition as in a normal interrupt mechanism.

When the CE/$\overline{T0}$ level is active during the STOP instruction then no STOP is executed.

A HIGH level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode.

I/O facilities

The PCD3343 family has 23 I/O lines arranged as:

- Port 0 parallel port of 8 lines (P00 to P07)
- Port 1 parallel port of 8 lines (P10 to P17)
- Port 2 parallel port of 4 lines (P20 to P23)
- SCLK serial I/O consisting of a data line shared with a parallel port line (P23) and a separate clock line SCLK
- CE/$\overline{T0}$ external interrupt and test input. When used as a test input can be directly tested by conditional branch instructions JT0 and JNT0
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional.
Output data written to a port is latched and remains unchanged until rewritten.
Input data is not latched and so must be present until read by an input instruction.

Input lines are fully CMOS compatible, output lines can drive one LS-TTL or CMOS load.

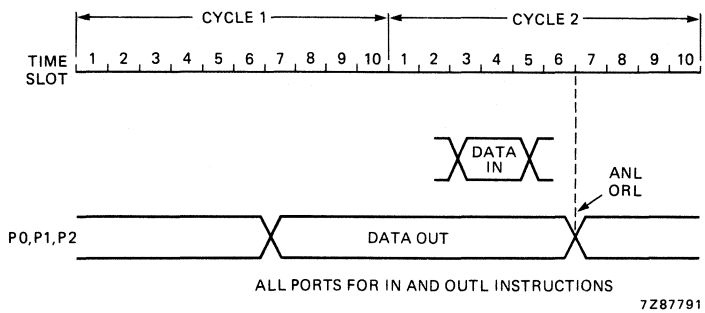


Fig. 10 Timing diagram of all ports on IN and OUTL instructions; for ANL and ORL instructions, the ports change on the time slot 7 of cycle 2.

Fig. 11 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source.
Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current provides sufficient source current for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

FUNCTIONAL DESCRIPTION (continued)

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

In telephone applications this switched pull-up source may not be sufficient. Therefore the PCD3343 offers the possibility to select individually 19 of the 20 parallel port pins (not P23), by the following mask options:

Option 1- STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2 (1,5 mA). TR2 is only active during 1 clock cycle (0,28 μs at 3,58 MHz).

Option 2- OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 12). When an open drain port is unused it must be connected to V_{SS}

Option 3- PUSH-PULL OUTPUT; drive capability of the output will be 1,5 mA (typ.) at V_{DD} = 3 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must only be used as outputs (Fig. 13).

Also, individual mask selection of the RESET state of these port pins can be achieved by appending the following options S and R to options 1, 2 or 3.

Option S-SET; after RESET this pin will be initialized to HIGH.

Option R-RESET; after RESET this pin will be initialized to LOW.

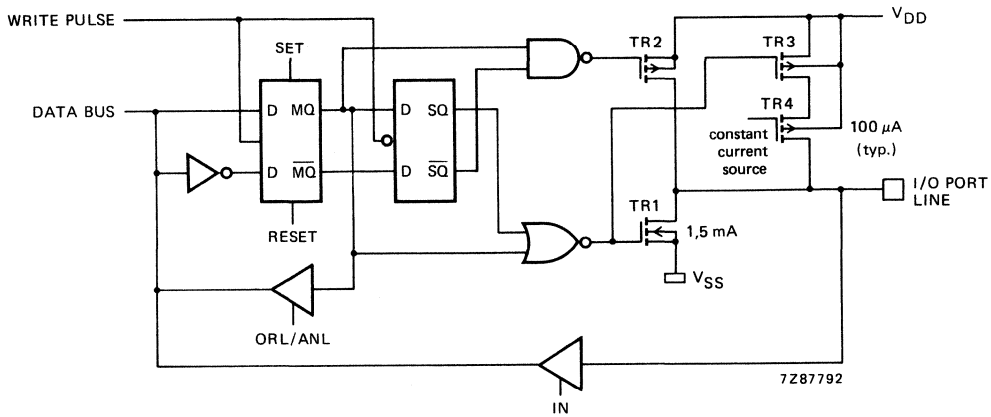


Fig. 11 Standard output with switched pull-up current source.

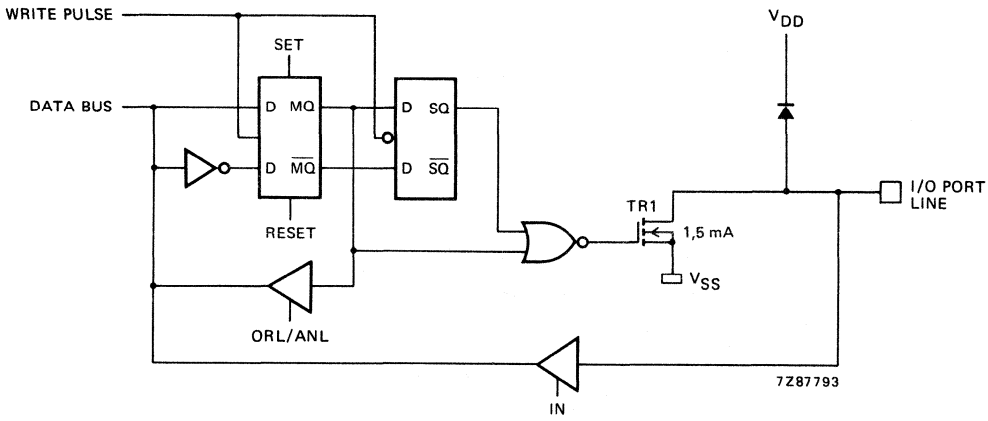


Fig. 12 Open drain output.

DEVELOPMENT DATA

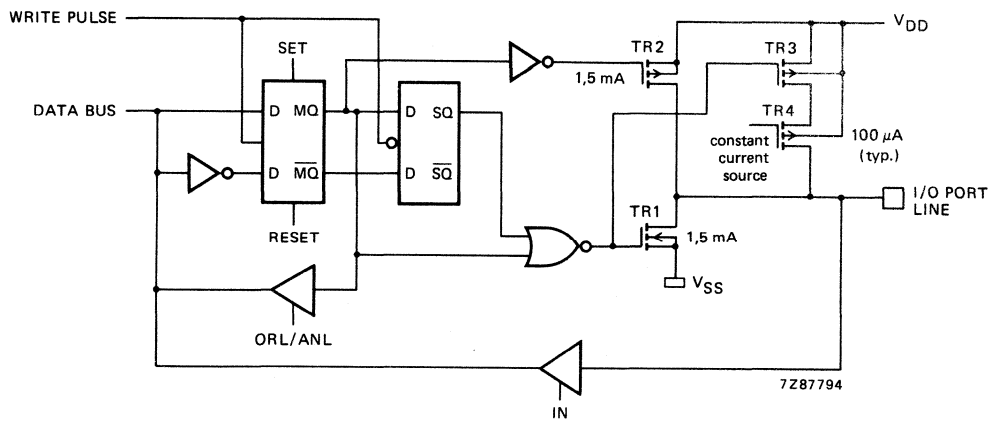


Fig. 13 Push-pull output.

FUNCTIONAL DESCRIPTION (continued)

Serial I/O (SIO)

The PCD3343 has an on-chip serial I/O interface. This SIO interface is a versatile feature in an intelligent telephone set, as shown in application diagram Fig. 32.

In this application the SIO is used to communicate with the different peripherals, such as:

- DTMF generator (PCD3312)
- LCD drivers (PCF8577)
- External RAM (PCD8571)
- Clock calendar (PCB8573)

No extra hardware is required for decoding, addressing and data processing.

Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCD3343 only when a complete byte is received. It then reads the data byte in one instruction. Likewise during transmission the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data. The microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

The design of the PCD3343 serial I/O system allows any number of devices from PCF8500 family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCD3343 is switched off. This means that the serial I/O logic will remain in the state it was at the occurance of the STOP instruction. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction. This must be carried out only when the PCD3343 has finished a serial data transfer.
After a negative RESET signal the first 30 clock pulses of the 1866 pulse initialization phase set P23/SDA and SCLK HIGH. When P23/SDA or SCLK are not used, they must be connected to V_{SS}.

Serial I/O interface

Figure 14 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 3 (SCLK) while the data line shares pin 2 (serial data) with the I/O line P23 of port 2. When the serial I/O is enabled, P23 is disabled as a parallel port line; (P23 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register

Data shift register (S0)

Register S0 converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while interface bits can only be read.

MST and TRX (see Table 1)

These bits determine the operating mode of the serial I/O interface.

Table 1 Operating modes of the serial I/O interface

MST	TRX	operating mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy.

This is the flag which indicates the status of the bus.

PIN: Pending Interrupt Not

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial output

The ESO flag enables/disables the serial I/O interface: ESO = '1' enables, ESO = '0' disables. ESO can only be written by software.

BC0, BC1 and BC2

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

AAS: Addressed As Slave

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

FUNCTIONAL DESCRIPTION (continued)

Serial clock control word (S2)

Bits 0 to 4 of the clock control register S2 are used to set the frequency of the serial clock signal. When a 3,58 MHz crystal is used, the frequency of the serial clock can be varied between 92 kHz and 580 Hz (see Table 2). An asymmetrical clock with a HIGH-to-LOW ratio of 3 : 1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O. S2 is a write only register.

Address register

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, # data instructions, but only when ES0 = '0'.

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When the logic is enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt is still indicated by PIN in S1, allowing the interrupt to be serviced. However, vectored interrupt will not occur.

Table 2 SIO clock pulse frequency control when using a 3,58 MHz crystal

hexadecimal S20-S24 code	divisor	f_{SCLK} (kHz) (approximate)
0	not allowed	
1	39	92
2	45	80
3	51	70
4	63	57
5	75	48
6	87	41
7	99	36
8	123	29
9	147	24
A	171	21
B	195	18
C	243	15
D	291	12
E	339	11
F	387	9,2
10	483	7,4
11	579	6,2
12	675	5,3
13	771	4,6
14	963	3,7
15	1155	3,1
16	1347	2,7
17	1539	2,3
18	1923	1,9
19	2307	1,6
1A	2691	1,3
1B	3075	1,2
1C	3843	0,93
1D	4611	0,78
1E	5379	0,67
1F	6147	0,58

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Table 3 Serial I/O addresses for telephony peripherals

type	address 7	6	5	4	3	2	1	0	description
PCF8570A	1	0	1	0	A2	A1	X	R/$\overline{W}$	2 K RAM
PCF8570	1	0	1	0	A2	A1	A0	R/$\overline{W}$	2 K RAM
PCD8571	1	0	1	0	A2	A1	A0	R/$\overline{W}$	1 K RAM
PCD3311	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialler
PCD3312	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialler
PCE2111	0	0	0	0	0	0	1	0	LCD driver *
PCD8573	1	1	0	1	0	A1	A0	R/$\overline{W}$	clock calendar
PCF8574	0	0	1	1	A2	A1	A0	R/$\overline{W}$	8-bit I/O expander
PCF8576	0	1	1	1	0	0	SA0	R/$\overline{W}$	1 : 4 LCD driver
PCF8577	0	1	1	1	0	1	0	R/$\overline{W}$	1 : 2 LCD driver

* LCD driver requires an additional enable line.

DEVELOPMENT DATA

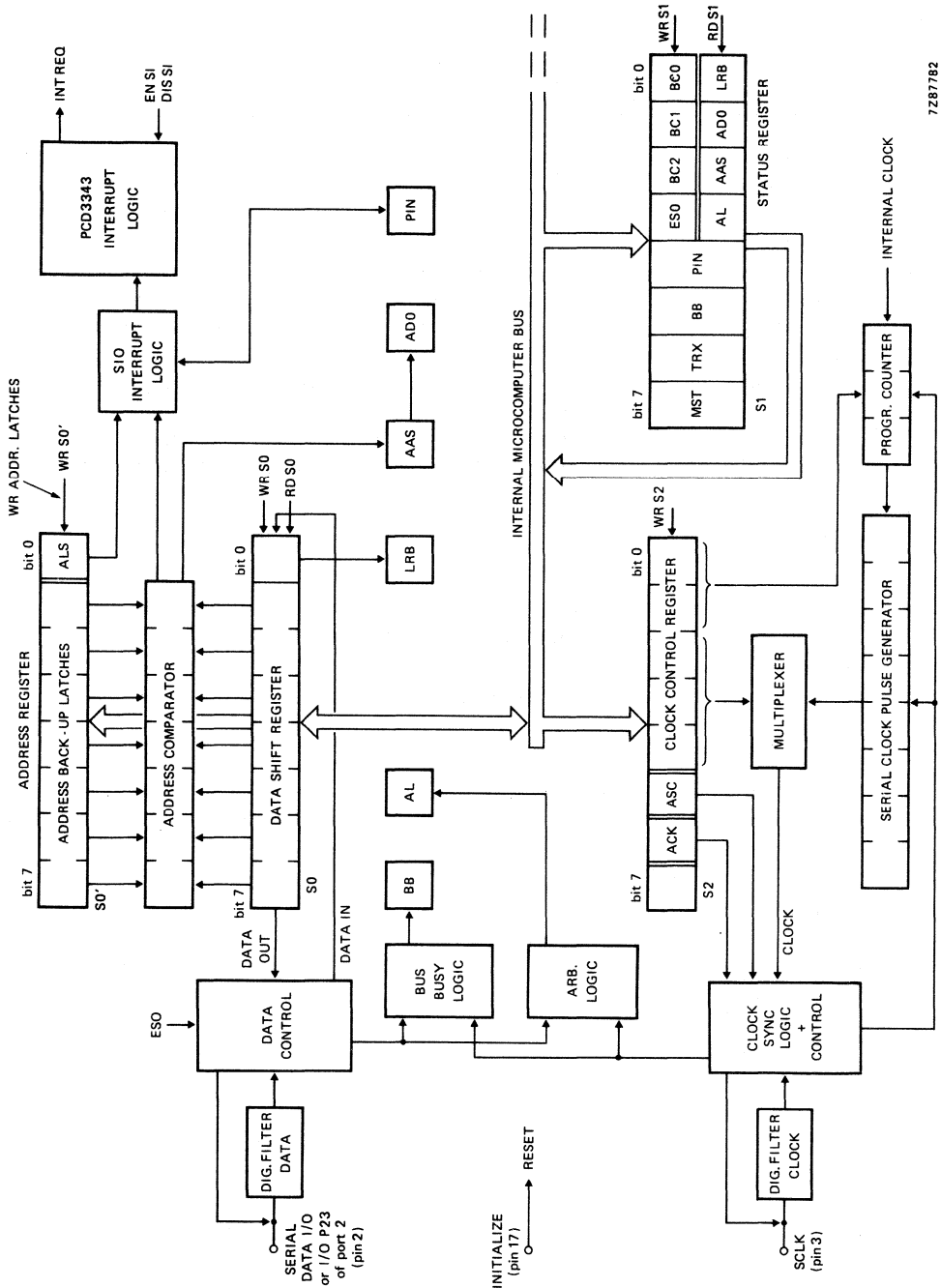


Fig. 14 Serial I/O interface.

FUNCTIONAL DESCRIPTION (continued)

Interrupts (see Fig. 15)

When the external interrupt is enabled, a LOW-to-HIGH transition on the CE/$\overline{T0}$ input initiates an external interrupt subroutine which causes a CALL to program memory location 3 following completion of the current instruction.
The interrupt must remain enabled until the interrupt instruction is completed, otherwise the next instruction of the main program will be executed. Serial I/O interrupt, when enabled, causes a CALL to location 5, and a timer/event counter overflow forces a CALL to location 7 when the timer interrupt is enabled.

When an interrupt subroutine starts, the contents of the program counter and bits 4, 6 and 7 of the PSW have been saved in the program counter stack. Accumulator contents have to be saved by software. Interrupt acknowledgement can be carried out by software via port pins. All interrupt subroutines must reside in memory bank 0.

Since the interrupt system is single level, once an interrupt is detected, all further interrupt requests are latched, but ignored, pending a RETR instruction to re-enable the interrupt input logic. After executing RETR, the program continues in the main part; this is independent of the occurance of a second interrupt during the running of the first routine. If 2 or 3 interrupts occur simultaneously, their priority is:

- (1) external
- (2) serial I/O
- (3) timer/event counter

An external interrupt can be generated by using the timer/counter in the event counter mode. The counter is first preset to (H'FF'), then EN TCNTI instruction is executed. A LOW-to-HIGH transition of the T1 input will then initiate an interrupt subroutine and cause a CALL to location 7.

On execution of a DIS I instruction, the PCD3343 always clears the digital filter/latch and the External Interrupt Flag.

The Timer Flag (TF) is reset only when the JTF or JNTF instruction is executed or after RESET.

The Timer Interrupt Flag is set when timer overflow occurs, only if the timer interrupt is enabled.

The microcontroller will exit the IDLE mode when any one of the following three interrupts is enabled:

- External
- Serial I/O
- Timer/event counter

There is no internal pull-up or pull-down device connected to the external interrupt input (pin 12). If required pin 12 must be externally connected to a resistor ($R \leqslant 100\ k\Omega$). When the external interrupt is not used pin 12 must be connected to V_{SS}.

DEVELOPMENT DATA

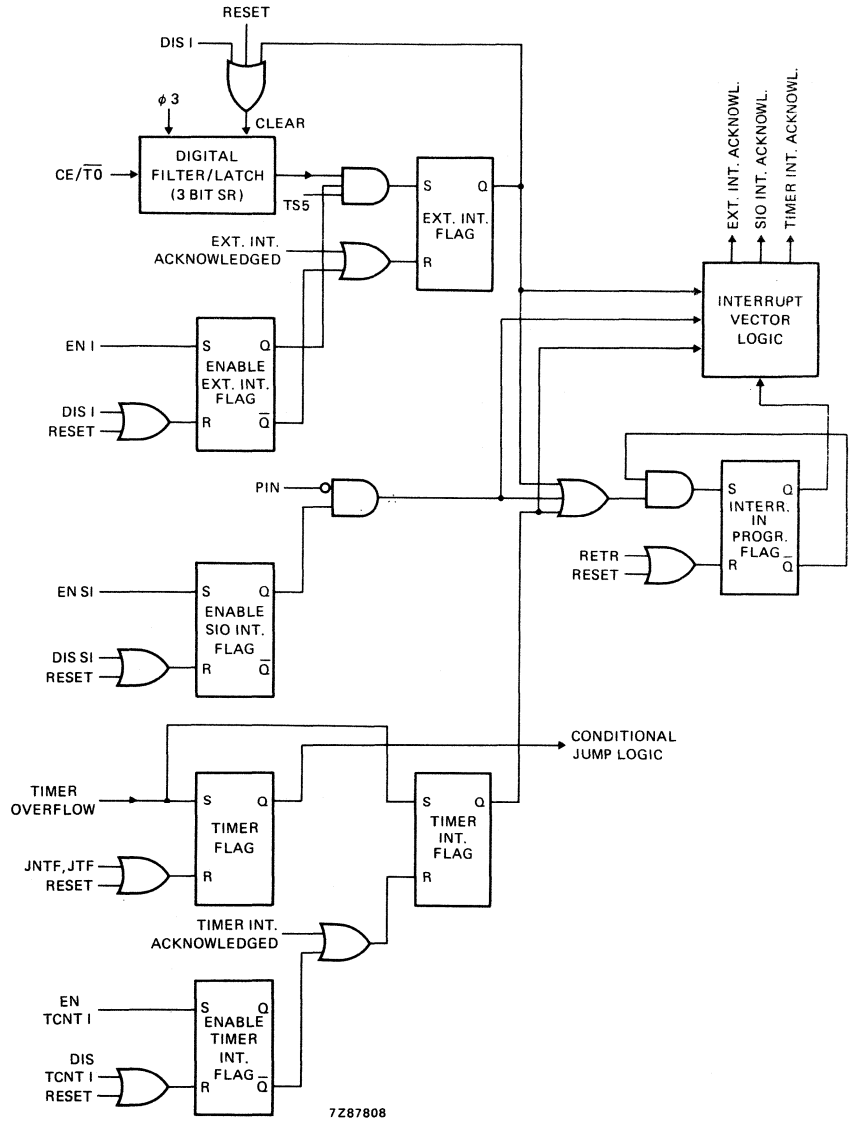


Fig. 15 Interrupt logic.

Notes to figure 15

1. CE/$\overline{T0}$ positive edge is always latched in the digital filter/latch.
2. Correct interrupt timing in ensured when CE/$\overline{T0}$ is LOW for $>$ 4 CP followed by a HIGH for $>$ 7 CP.
3. When the interrupt in progress flag is set, further interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.

FUNCTIONAL DESCRIPTION (continued)

Oscillator (see Fig. 16)

The 3,58 MHz oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-voltage condition is present to prevent discharge of a weak back-up battery.

Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a HIGH level at either the CE/$\overline{T0}$ or RESET pin.

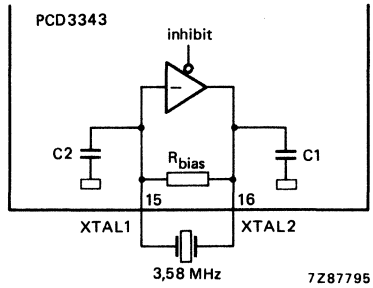


Fig. 16 Oscillator with integrated elements.

The oscillator has the output drive capability for the DTMF generator (PCD3311/3312) via pin 16 (XTAL 2). An external clock can be applied to pin 15 (XTAL 1). A machine cycle consists of 10 time slots, each time slot being 3 oscillator periods.

In telephony applications the 3,58 MHz crystal provides a 8,4 μs machine cycle. The range of the clock frequency is from 100 kHz up to a maximum which is a function of the supply voltage (see Fig. 23).

Timer/event counter (see Fig. 17)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 4 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin 13 (T1) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (182,6 kHz for a 8,4 μs machine cycle). When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump if timer flag = 1) or JNTF instruction. Overflow also generates an interrupt to the processor via setting of the Timer Interrpt Flag when the timer/event counter interrupt is enabled.

Table 4 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

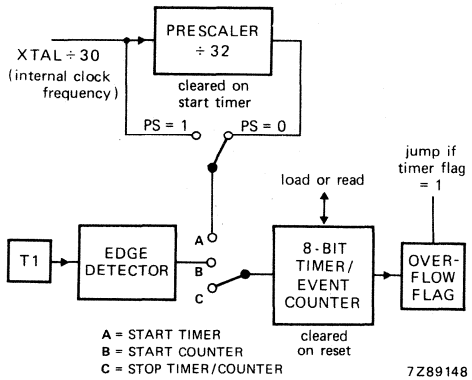


Fig. 17 Timer/event counter.

DEVELOPMENT DATA

Program status word (see Fig. 18)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS); 0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS); 0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

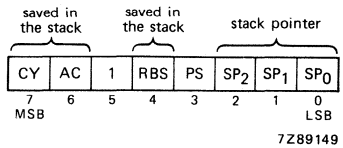


Fig. 18 Program status word.

* With prescaler select, PS = 0, the timer counts modulo-32 machine cycles, with PS = 1 it counts modulo-1 cycles (prescaler not used); prescaler cleared with STRT T, prescaler not readable.

** READ does not disturb the counting process.

FUNCTIONAL DESCRIPTION (continued)

Program status word (continued)

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program counter (see Fig. 19)

A 13-bit program counter is used to facilitate 8 K bytes of ROM being addressed. The arrangement of the bits is shown in figure 19. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 13 bits are saved in the stack during CALL and interrupt routines.

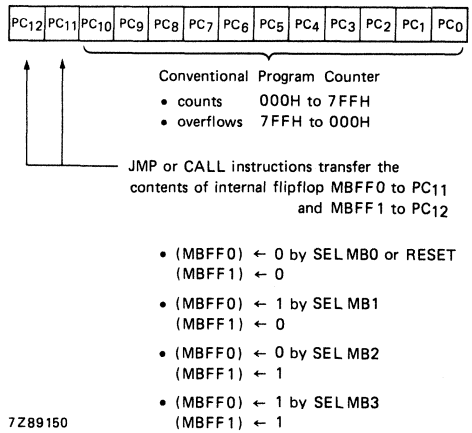


Fig. 19 Program counter.

Central processing unit

The PCD3343 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 5 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 5 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JNT0
	0	JT0*
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

Test input T1 (pin 13)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for > 4 CP, followed by a HIGH for > 4 CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor ($R = \leqslant 100\ k\Omega$). When T1 is not used pin 13 must be connected to V_{DD} or V_{SS}.

Reset (pin 17)

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory band 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports according to reset states
- Sets all ports except P23 to reset state *(see Serial I/O)*
- Cancels IDLE and STOP mode

A negative-going signal on the RESET input/output:

- Sets P23/SDA and SCLK to HIGH after a maximum of 30 clock pulses
- Sets the serial I/O to slave receiver mode and disables the serial I/O after 1866 clock pulses
- Starts an internal delay of 1866 clock pulses after which the microcontroller commences operation.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Power-on-reset and low-voltage detection (see Fig. 20)

In telephony applications, correct operation of the PCD3343 during moments of slowly changing supply voltages and low-voltage conditions is essential. This is achieved by the addition of an internal power-on-reset and low-voltage detection circuit.
To allow an external RESET signal being fed into the PCD3343, the reset pin (pin 17) has been configured as an input/output.

While a reset condition exists in the detection circuit, pin 17 is pulled HIGH by TR1 controlled by the reset circuit.
When the reset condition is not present a pull-down current source (TR2) will be activated. TR2 forces pin 17 LOW thus removing the RESET signal from the microcontroller.

Since the level at pin 17 is recognized by the microcontroller, the reset time constant can be stretched by connecting an external capacitor between V_{DD} and pin 17 (see Fig. 22).

The signal at pin 17 can also be used as an output to reset other devices in the system.

The internal reset circuit monitors the PCD3343 supply voltage. If the voltage drops below the switching level (typ. 1,3 V), a reset (HIGH) is applied to pin 17. This reset is removed (pin 17 goes LOW), after a fixed delay (t_d), when the supply voltage rises above the switching level again. The delay ensures a complete reset even when the supply voltage quickly rises above switching level after initial switch-on.

During a low-voltage condition the oscillator is inhibited to prevent complete discharge of a weak battery. The timing of the power-on-reset and low-voltage detection circuit is shown in figure 21.

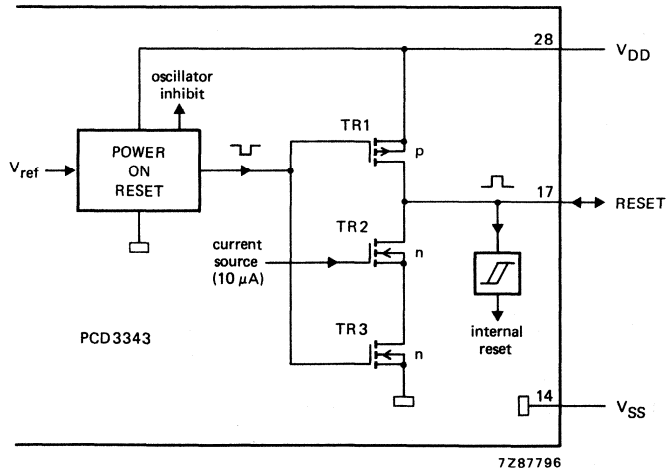
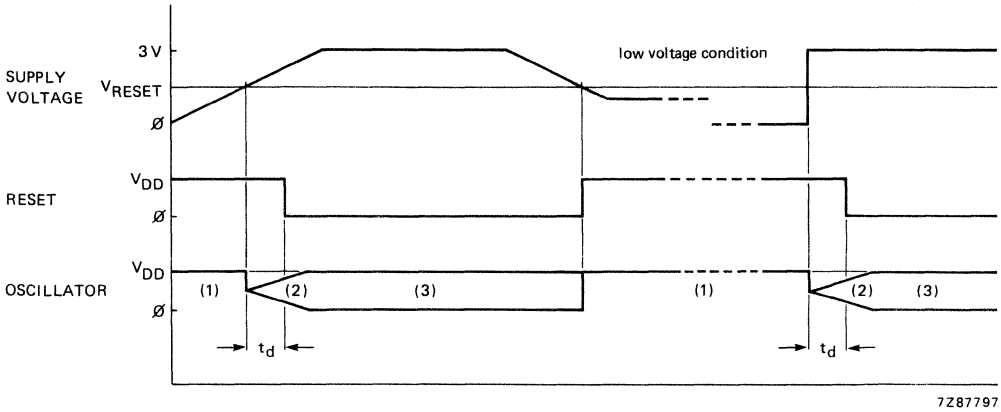


Fig. 20 Power-on-reset configuration.



Where: (1) Oscillator inhibited
(2) Oscillator starting
(3) Oscillator running, but may be stopped with a STOP condition

Fig. 21 Timing of power-on-reset and low-voltage detection.

DEVELOPMENT DATA

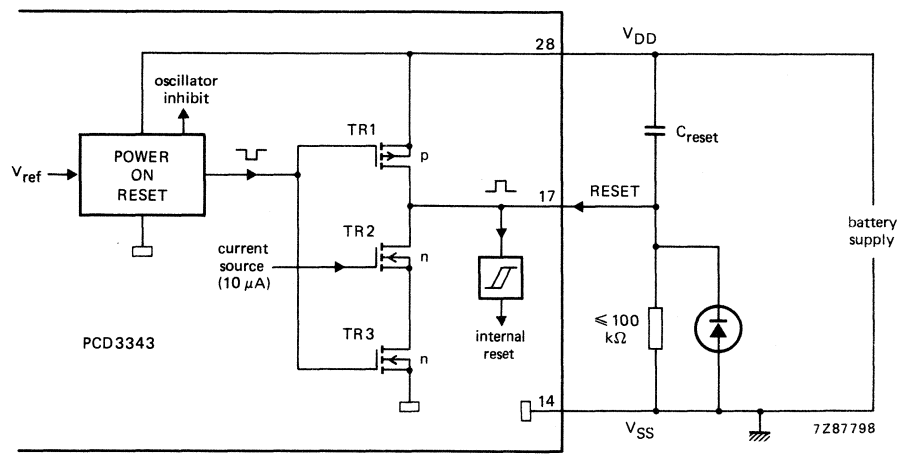


Fig. 22 Stretched power-on-reset with external capacitor.

INSTRUCTION SET

The PCD3343 instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for serial I/O operation and memory bank selection. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 8 gives the instruction set of the PCD3343. Table 7 shows the instruction map and Table 6 details the symbols and definition descriptions that are used.

Table 6 Symbols and definitions used in Table 8

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0-7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
D	mnemonic for 4-bit digit (nibble)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0-7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

Table 7 PCD3343 instruction map

first hexadecimal character of opcode ↓

second hexadecimal character of opcode →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A,#data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0 1 2				MOV A,Sn 0 1			
1	INC @Rr 0 1		JB0 addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0 1 2 3 4 5 6 7							
2	XCH A,@Rr 0 1		STOP	MOV A,#data	JMP page 1	EN TCNTI	JNTO addr	CLR A	XCH A,Rr 0 1 2 3 4 5 6 7							
3	XCHD A,@Rr 0 1		JB1 addr		CALL page 1	DIS TCNTI	JTO addr	CPL A	OUTL Pp,A 0 1 2				MOV Sn,A 0 1 2			
4	ORL A,@Rr 0 1		MOV A,T	ORL A,#data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0 1 2 3 4 5 6 7							
5	ANL A,@Rr 0 1		JB2 addr	ANL A,#data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0 1 2 3 4 5 6 7							
6	ADD A,@Rr 0 1		MOV T,A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0 1 2 3 4 5 6 7							
7	ADDC A,@Rr 0 1		JB3 addr		CALL page 3			RR A	ADDC A,Rr 0 1 2 3 4 5 6 7							
8				RET	JMP page 4	EN SI			ORL Pp,#data 0 1 2							
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data 0 1 2				MOV Sn,#data 0 1 2			
A	MOV @Rr,A 0 1			MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0 1 2 3 4 5 6 7							
B	MOV @Rr,#data 0 1		JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data 0 1 2 3 4 5 6 7							
C	DEC @Rr 0 1				JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr 0 1 2 3 4 5 6 7							
D	XRL A,@Rr 0 1		JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr 0 1 2 3 4 5 6 7							
E	DJNZ @Rr,addr 0 1				JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr 0 1 2 3 4 5 6 7							
F	MOV A,@Rr 0 1		JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0 1 2 3 4 5 6 7							

INSTRUCTION SET (continued)

Table 8 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1}) \leftarrow A_n$ $(A_0) \leftarrow (C)$, $(C) \leftarrow (A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (C)$, $(C) \leftarrow (A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7}) \leftrightarrow (A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3}) \leftrightarrow ((R0_{0-3}))$ $(A_{0-3}) \leftrightarrow ((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3) \leftarrow (A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7}) \leftarrow (A)$, $(A) \leftarrow ((PC))$		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1	
BRANCH	JMP addr	● 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0 : (PC_{0-7})←addr	
	JT0 addr	36 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JNT0 addr	26 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4,6,7}$) 6 (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) −1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) −1 ($PSW_{4,6,7}$) + (PC)←((SP))	6

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	 7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 99 9A	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 89 8A	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	 8
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	 9
	MOV S_n, #data	9C 9D 9E	2/2	move immediate data to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 8

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 1111 P23, P22, P21, P20.
8. (S1) has a different meaning for read and write operation, see serial I/O interface.
9. (S2) is a write only register. Reading S2 will give value FFH.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 28)	V_{DD}		−0,8 to + 8	V
All input voltages	V_I	0,8 to V_{DD} + 0,8		V
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
Total power dissipation (see note)	P_{tot}	max.	500	mW
Power dissipation per output				
except P23, SCLK	P_O	max.	50	mW
P23, SCLK	P_O	max.	180	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Operating junction temperature	T_j	max.	125	°C

Note

Thermal resistance (junction to ambient)				
for SOT117	$R_{th\ j\text{-}a}$	max.	120	K/W
for SOT136A	$R_{th\ j\text{-}a}$	max.	150	K/W

DEVELOPMENT DATA

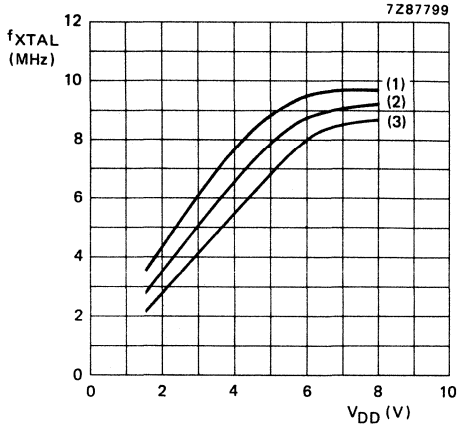
D.C. CHARACTERISTICS

V_{DD} = 2,75 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 50 Ω; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 23)	V_{DD}	1,8	–	6	V
STOP mode for RAM retention	V_{DD}	1,0	–	6	V
Supply current					
operating					
at V_{DD} = 3 V (see Fig. 24)	I_{DD}	–	600	–	μA
IDLE mode					
at V_{DD} = 3 V (see Fig. 25)	I_{DD}	–	300	–	μA
STOP mode (see Fig. 26 and note 1)					
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 1,8 V; T_{amb} = 55 °C	I_{DD}	–	–	5	μA
at V_{DD} = 1,8 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O					
Switching level	V_{RESET}	–	1,3	–	V
Sink current					
at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\|I_O\| < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 3 V; V_O = 0,4 V					
except P23/SDA, SCLK (see Fig. 27)	I_{OL}	0,75	1,5	–	mA
P23/SDA, SCLK (see Fig. 28)	I_{OL}	1,5	–	–	mA
Pull-up output source current HIGH (see Fig. 29)					
at V_{DD} = 3 V; $V_O = 0{,}9V_{DD}$	$-I_{OH}$	25	–	–	μA
at V_{DD} = 3 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	200	μA
Push-pull output source current HIGH					
at V_{DD} = 3 V; $V_O = V_{DD}$−0,4 V	$-I_{OH}$	0,75	1,5	–	mA

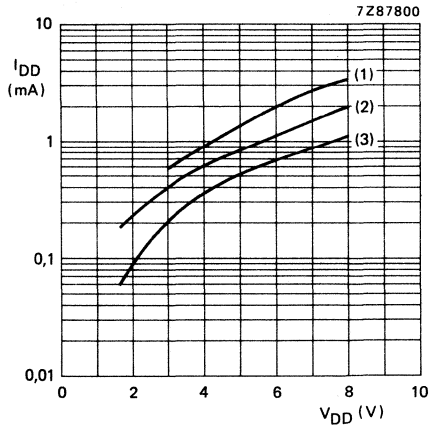
Note 1

Crystal connected between XTAL 1 and XTAL 2; SCL and SDA pulled to V_{DD} via 5,6 kΩ resistor; CE and T1 at V_{SS}.



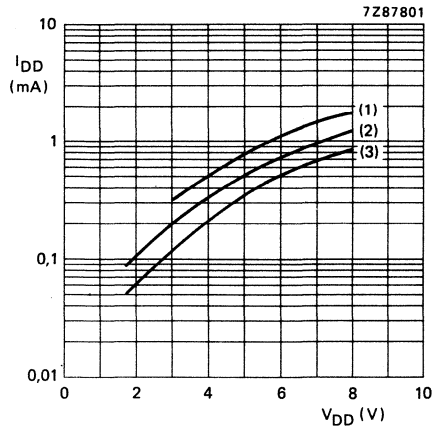
(1) $T_{amb} = -25$ °C
(2) $T_{amb} = 25$ °C
(3) $T_{amb} = 70$ °C

Fig. 23 Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (V_{DD}).



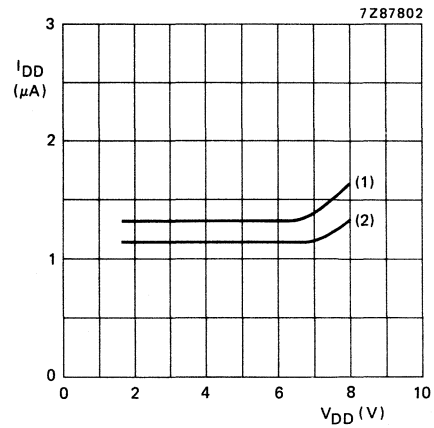
(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

Fig. 24 Typical supply current (I_{DD}) in operating mode as a function of the supply voltage (V_{DD}); $T_{amb} = 25$ °C.



(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

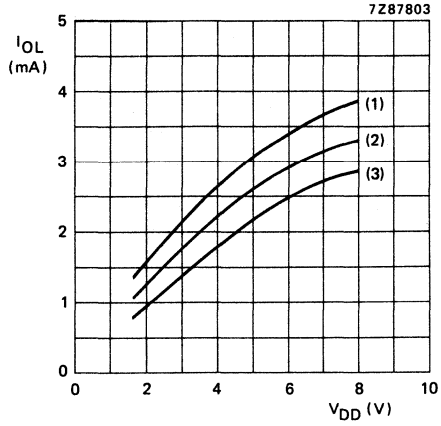
Fig. 25 Typical supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}); $T_{amb} = 25$ °C.



(1) $T_{amb} = 70$ °C
(2) $T_{amb} = 25$ °C

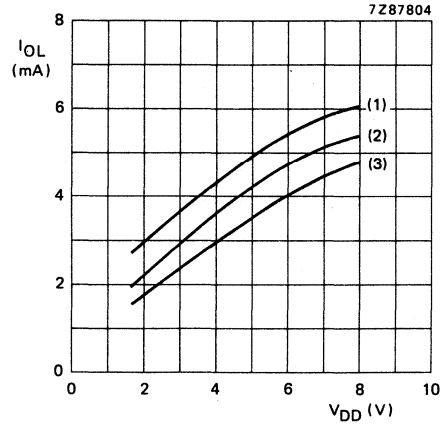
Fig. 26 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).

DEVELOPMENT DATA



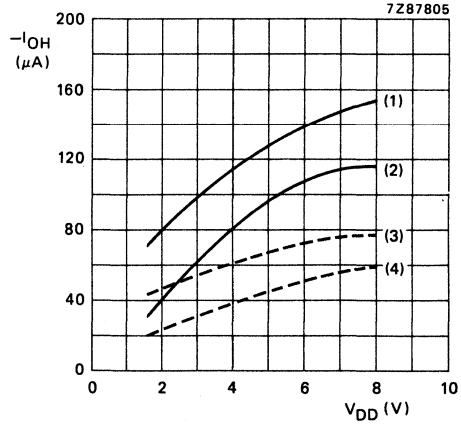
(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = 25\ ^{o}C$
(3) $T_{amb} = 70\ ^{o}C$

Fig. 27 Output sink current LOW (I_{OL}), except outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); $V_O = 0,4$ V.



(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = +25\ ^{o}C$
(3) $T_{amb} = +70\ ^{o}C$

Fig. 28 Output current LOW (I_{OL}), outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); $V_O = 0,4$ V.



(1) $T_{amb} = 25\ ^{o}C$; $V_O = V_{SS}$
(2) $T_{amb} = 25\ ^{o}C$; $V_O = 0,9V_{DD}$
(3) $T_{amb} = 70\ ^{o}C$; $V_O = V_{SS}$
(4) $T_{amb} = 70\ ^{o}C$; $V_O = 0,9V_{DD}$

Fig. 29 Output source current HIGH ($-I_{OH}$) as a function of supply voltage (V_{DD}).

A.C. CHARACTERISTICS

Rise and fall times between 10 and 90% levels; C_L = 50 pF

parameter	symbol	at 70 °C max. value			unit
	V_{DD}	1,8	3,0	6,0	V
Fall time	t_f	200	100	70	ns
Rise time	t_r	200	100	80	ns

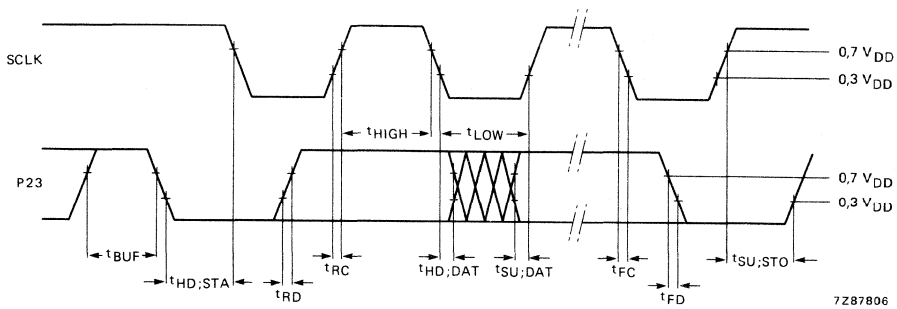


Fig. 30 PCD3343 timing requirements for the P23 and SCLK *input* signals.

Table 9 Input timing shown in figure 30

symbol	timing
t_{BUF}	$\geqslant 14t_{XTAL}$
$t_{HD;STA}$	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
$t_{SY;STO}$	$\geqslant 14t_{XTAL}$
$t_{HD;DAT}$	> 0
$t_{SU;DAT}$	$\geqslant 250$ ns
t_{RD}	$\leqslant 1\ \mu s$
t_{RC}	$\leqslant 1\ \mu s$
t_{FD}	$\leqslant 1\ \mu s$
t_{FC}	$\leqslant 0{,}3\ \mu s$

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Notes to Table 9

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280 ns for f_{XTAL} = 3,58 MHz.
These figures apply to all modes.

DEVELOPMENT DATA

A.C. CHARACTERISTICS (continued)

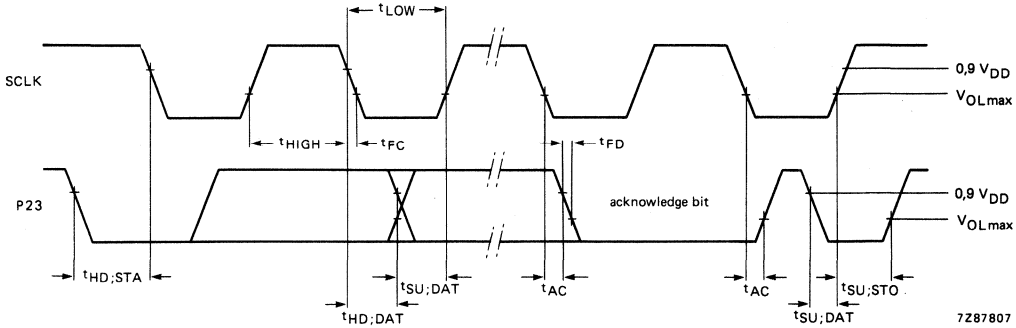


Fig. 31 PCD3343 timing requirements for the P23 and SCLK *output* signals.

Table 10 Output timing shown in figure 31

symbol	timing	
	normal mode (ASC in S2 = 0)	low-speed mode (ASC in S2 = 1)
$t_{HD;STA}$	½ (DF + 9) t_{XTAL}	¾ (DF + 9) t_{XTAL}
t_{HIGH}	½ (DF) t_{XTAL}	¾ (DF) t_{XTAL}
t_{LOW}	½ (DF) t_{XTAL}	¼ (DF) t_{XTAL}
$t_{SU;STO}$	½ (DF − 3) t_{XTAL}	¼ (DF − 3) t_{XTAL}
$t_{HD;DAT}$ (slave transmitter)		
any DF	$\geqslant 9t_{XTAL}$	$\geqslant 9t_{XTAL}$
	$\leqslant 12t_{XTAL}$	$\leqslant 12t_{XTAL}$
$t_{HD;DAT}$ (master transmitter)		
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$	–
	$\leqslant 12t_{XTAL}$	–
for DF $\leqslant$ 99	–	$\geqslant 9t_{XTAL}$
	–	$\leqslant 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter)		
for DF > 51	$\geqslant 15t_{XTAL}$	–
	$\leqslant 24t_{XTAL}$	–
for DF > 99	–	$\geqslant 15t_{XTAL}$
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$	$\leqslant 24t_{XTAL}$
for DF $\leqslant$ 99	–	$\geqslant 9t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$	$\geqslant 9t_{XTAL}$
	$\leqslant 12t_{XTAL}$	$\leqslant 12t_{XTAL}$
t_{FD}, t_{FC}	$\leqslant$ 100 ns at C_b = 400 pF	$\leqslant$ 100 ns at C_b = 400 pF

Notes to Table 10

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280 ns for f_{XTAL} = 3,58 MHz.
DF = divisor (see Table 2 Serial I/O section).
C_b = the maximum bus capacitance for each line.

DEVELOPMENT DATA

APPLICATION INFORMATION

A block diagram of an electronic featurephone built around the PCD3343 is shown in figure 32. It comprises the following dedicated telephony IC's:

- TEA1060/1061 — transmission circuit for telephony
- PCD3312 — DTMF generator with Serial I/O
- PCE2111 or PCF8577 — 2 LCD drivers in LCD module MB7020160
- PCD8571 — 1 K RAM's with Serial I/O; the number of RAM's depends on the required amount of stored telephone numbers
- PCD3360/3361 — programmable multi-tone ringer

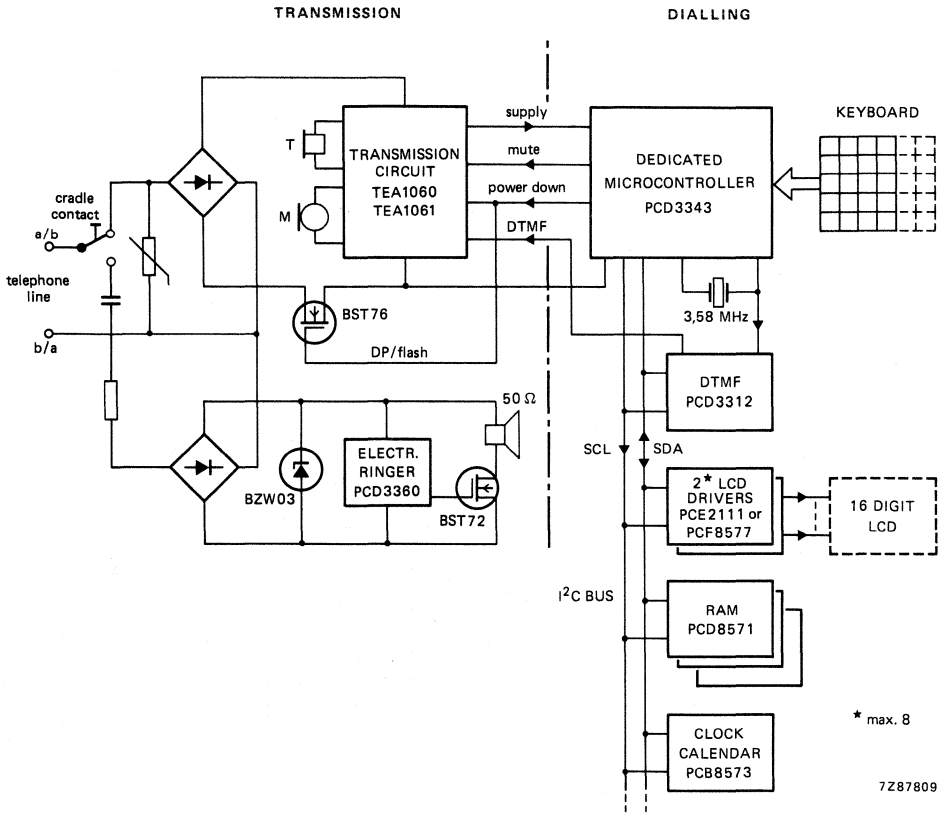


Fig. 32 Block diagram of electronic featurephone with common line interface.

A detailed application diagram of the PCD3343 with PCD3312 (DTMF), two PCD8571 (RAM) and two PCE2111 (LCD display drivers) is shown in figure 33.

Row 5 of the keyboard contains the following special keys:

- P — program and autodial
- FL — flash or register recall
- R — redial or extended redial
- AP — access pause

Row 6 contains the different diode options.

Columns 5 and 6 contain the button keys M0 to M9; single name keys for repertory telephone numbers.

APPLICATION INFORMATION (continued)

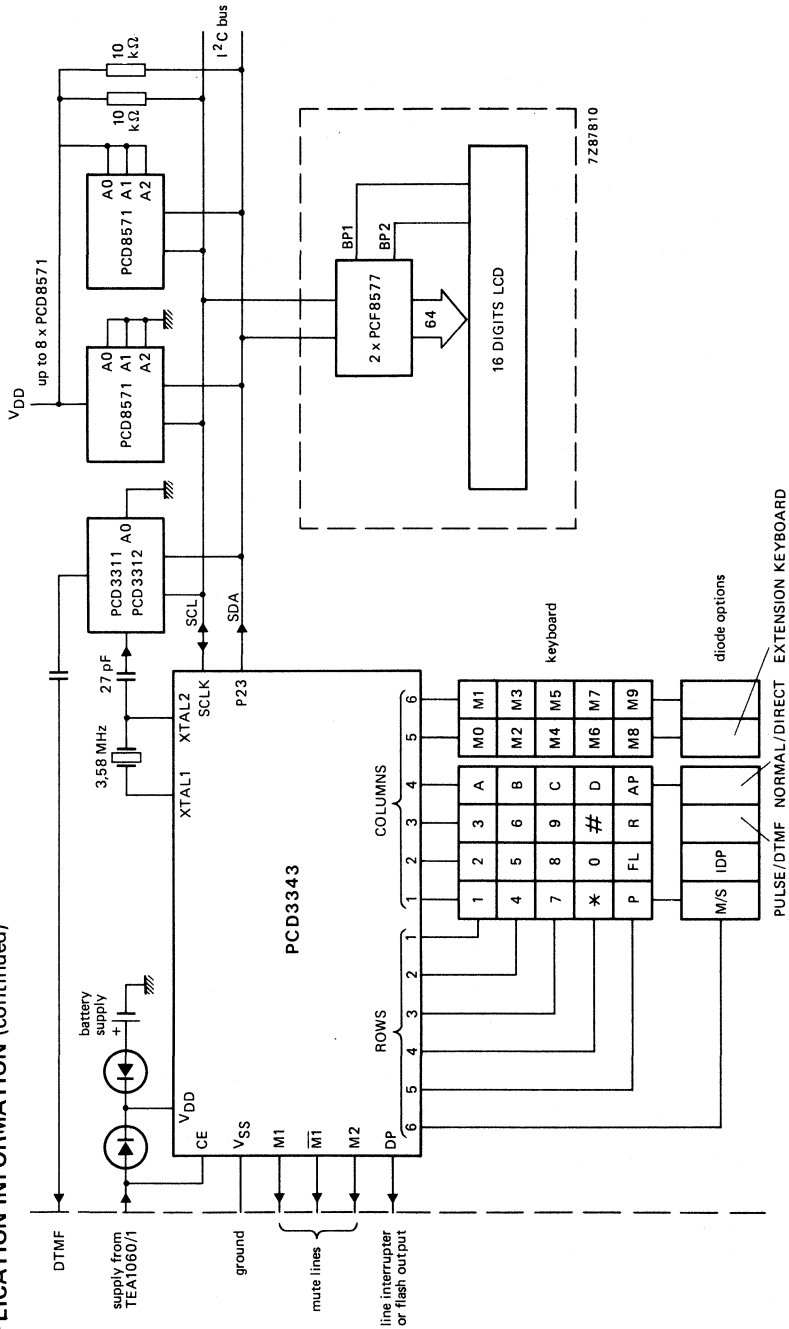


Fig. 33 Application diagram of PCD3343 for electronic featurephone with associated keyboard.

Additional information is available on request for the following:

- Serial I/O
- I^2C bus specification
- Interrupt logic
- Instruction set descriptions
- Software routines for an intelligent telephone set

CMOS MICROCONTROLLER WITH ON-CHIP DTMF GENERATOR

GENERAL DESCRIPTION

The PCD3344 is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD33XX family. It has an on-chip dual tone multi-frequency (DTMF) generator and other features for application in telephone sets. For further detailed information, see PCD33XX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 2048 ROM bytes
- 224 RAM bytes
- On-chip DTMF tone generator
- On-chip voltage reference for supply and temperature-independent tone output
- On-chip filtering for low output distortion (CEPT CS203 compatible)
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles
- Clock frequency 3,58 MHz
- Single supply voltage from 2,5 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3344P: 28-lead DIL; plastic (SOT117).
PCD3344T: 28-lead mini-pack; plastic (SO28; SOT136A).

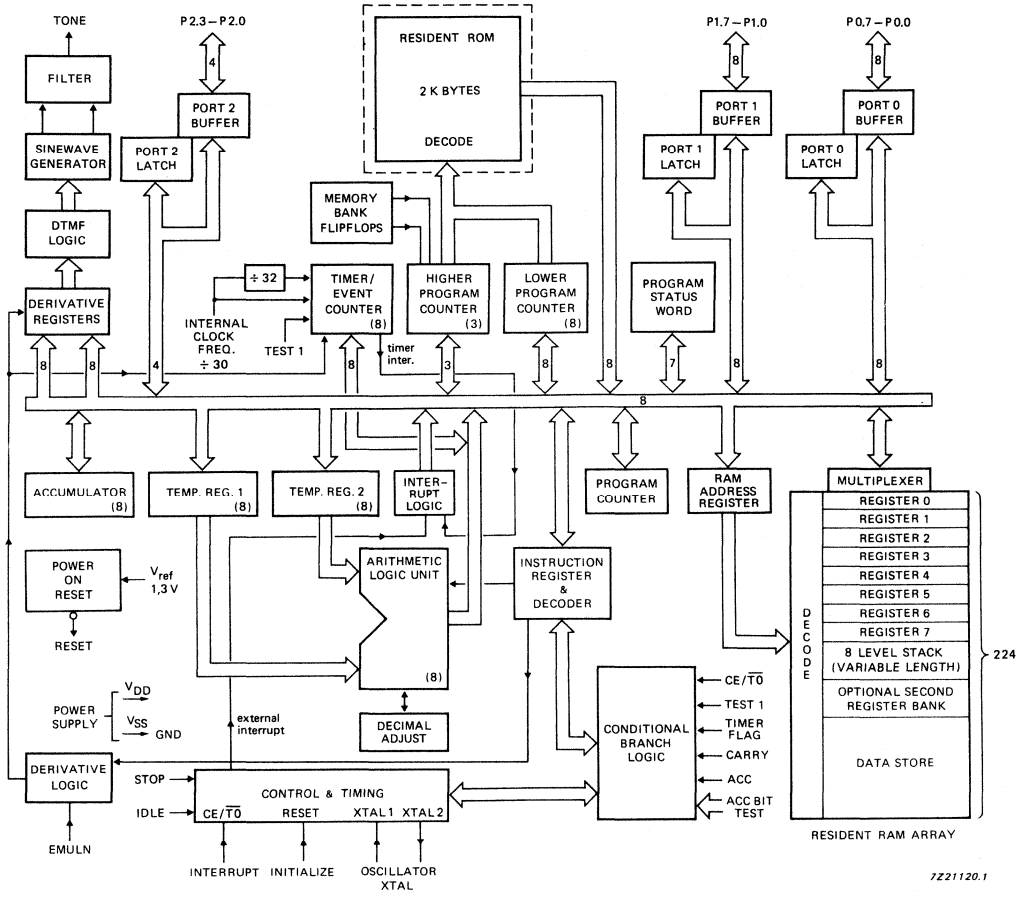


Fig. 1 PCD3344 block diagram: the function in the dotted outline is replaced as shown in (a) for the PCD3344B 'piggy-back' version.

DEVELOPMENT DATA

PINNING (for normal operation)

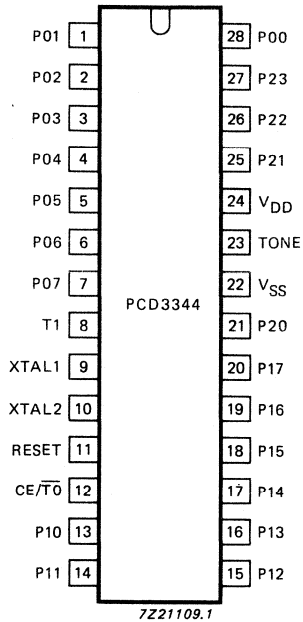


Fig. 2 Pinning diagram.

PIN DESIGNATION

28, 1-7	P00-P07	Port 0: 8-bit quasi-bidirectional I/O port.
8	T1	Test 1: test input, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter using the STRT CNT instruction.
9	XTAL1	Crystal input: connection to the timing component (crystal) which determines the frequency of the internal oscillator; is also the input for an external clock source.
10	XTAL2	Connection to other side of timing component.
11	RESET	Reset input (active HIGH): used to initialize the processor or output of the power-on-reset circuit.
12	CE/$\overline{T0}$	Interrupt/Test 0: external interrupt input (sensitive to positive-going edge)/test input pin. When used as a test input is directly tested by conditional branch instructions JT0 and JNT0.
13-20	P10-P17	Port 1: 8-bit quasi-bidirectional I/O port.
21, 25-27	P20-P23	Port 2: 4-bit quasi-bidirectional I/O port.
22	V_{SS}	Ground: circuit earth potentional.
23	TONE	Tone output: single or dual tone frequency output with on-chip filtering for low output distortion (CEPT CS203 compatible). This generator is controlled via the internal processor bus.
24	V_{DD}	Power supply: 2,5 to 6 V.

FUNCTIONAL DESCRIPTION

Program memory PCD3344

The program memory comprises 2048 bytes (8-bit words) in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 3 shows the program memory map.

Three program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine,
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

The program memory is divided into location 'pages', each of 256 bytes. This division applies only for conditional branches. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory PCD3344

Data memory consists of 224 bytes (8-bit words) of random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 4 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently-addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 5) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with next generated return address.

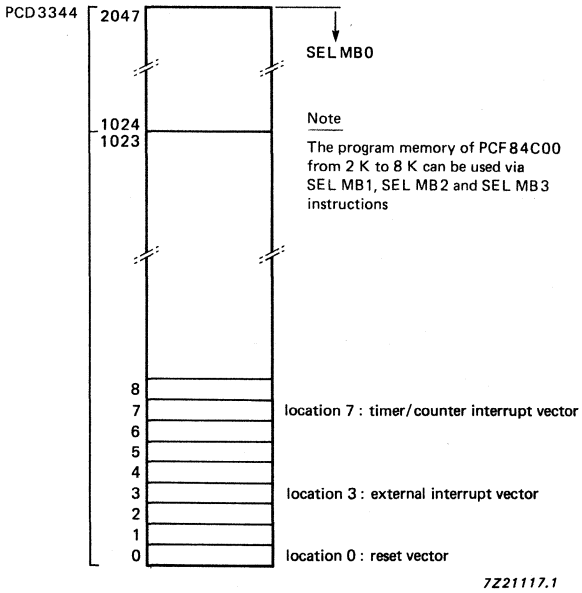


Fig. 3 Program memory map.

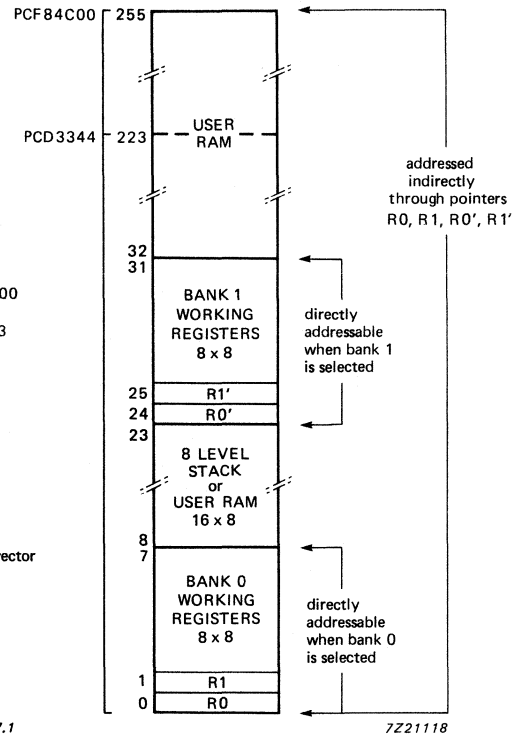


Fig. 4 Data memory map.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations. Possible locations from 32 to 223 may be used for storage of program variables or data.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

FUNCTIONAL DESCRIPTION (continued)

Program counter stack (continued)

stack pointer									
1 1 1	----------								R23/22
1 1 0	----------								R21/20
1 0 1	----------								R19/18
1 0 0	----------								R17/16
0 1 1	----------								R15/14
0 1 0	----------								R13/12
0 0 1	----------								R11/10
0 0 0	PSW7	PSW6	PC12	PSW4	PC11	PC10	PC9	PC8	R9
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	R8

Fig. 5 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (H'01') the oscillator and timer/counter are kept running. The microcontroller exits from the IDLE mode by one of two interrupts if they are enabled or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 6).

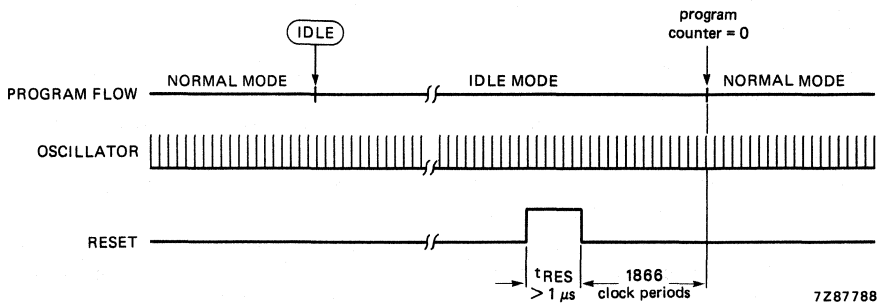


Fig. 6 Exit from IDLE mode via a RESET.

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A LOW-to-HIGH transition on the external interrupt pin (CE/$\overline{T0}$) reactivates the microcontroller. A HIGH level applied to CE/$\overline{T0}$ will reactivate the microcontroller only in the STOP mode. Thus, if CE/$\overline{T0}$ was HIGH before the microcontroller entered the IDLE mode, it must go LOW before the microcontroller can be reactivated (see Fig. 7).

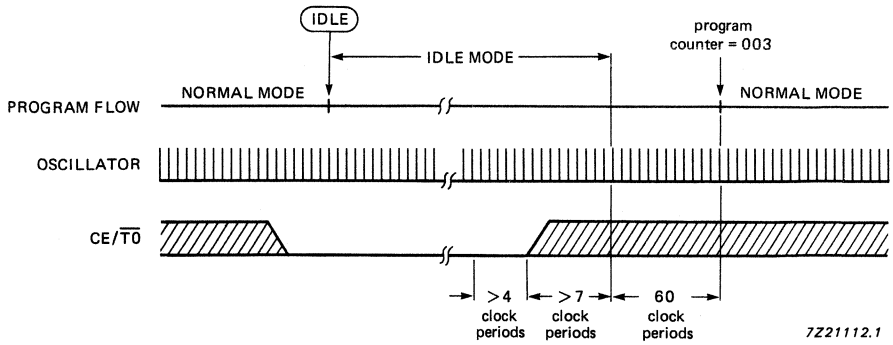


Fig. 7 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when CE/$\overline{T0}$ is LOW for 4 CP (clock periods) followed by a HIGH for 7 CP. After the initial forced CALL H'003' operation (60 CP) the program continues with the external interrupt service routine.

STOP mode

The microcontroller enters the STOP mode by the STOP instruction (H'22'). The oscillator is switched off. The internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 8).

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin HIGH, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a HIGH level applied at the CE/$\overline{T0}$ pin, and not by a LOW-to-HIGH transition as in a normal interrupt mechanism.

When the CE/$\overline{T0}$ level is active during the STOP instruction then no STOP is executed.

A HIGH level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

STOP mode (continued)

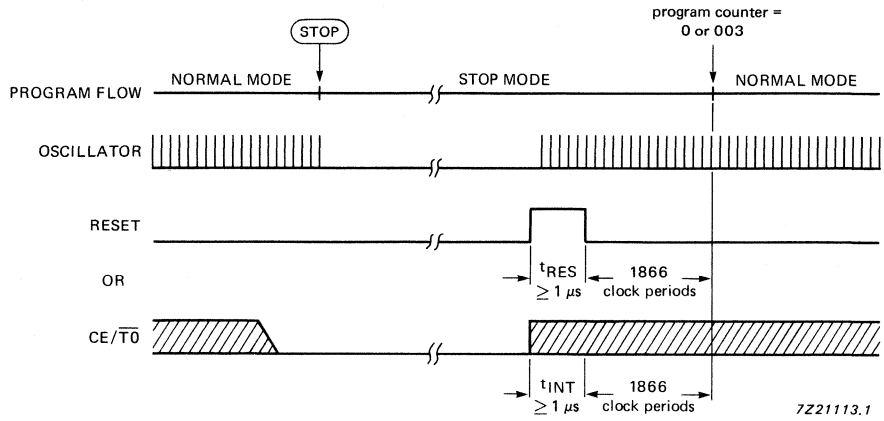


Fig. 8 Entering and exiting the STOP mode.

Tone output (DTMF mode)

Control of the sinewave generator

The on-chip sinewave oscillator is controlled by the 'derivative' registers Dx (x = H'O' to 'FF'). The instruction that controls the derivative registers is shown in Table 1.

Table 1 Derivative register control

mnemonic	opcode	description	function
MOV Dx,A	8D Dx	move accumulator contents to derivative register	(Dx) ← (A)

The instruction is 2 cycles/2 bytes. The second byte selects the derivative register to be addressed (H'O' to 'FF'). Register H'01' is for control of HIGH group frequencies, and register H'02' for control of LOW group frequencies. Thus data transport from accumulator to derivative register D01 is done by the 2-byte opcode 8D,01.

Generation of frequencies

The single and dual tones at the tone output are filtered by an on-chip switched-capacitor filter followed by an on-chip active RC low-pass filter. These ensure that the total harmonic distortion of the DTMF tones fulfil the CEPT CS 203 recommendations. An on-chip reference voltage provides output tone levels that are independent of the supply voltage.

The output frequency can be calculated as follows:

$$f_{out} = \frac{f_{XTAL}}{23\,(x + 2)} \quad \text{Hz}$$

x = 60 to 255 and is the decimal value of the appropriate ROM-code (see Table 2)

Table 2 ROM-codes for DTMF applications

telephone keyboard symbol	contents of low register (hex)	contents of high register (hex)
0	A3	72
1	DD	7F
2	DD	72
3	DD	67
4	C8	7F
5	C8	72
6	C8	67
7	B5	7F
8	B5	72
9	B5	67
A	DD	5D
B	C8	5D
C	B5	5D
D	A3	5D
*	A3	7F
#	A3	67

DTMF generation is stopped by loading H'00' into both derivative registers.

I/O facilities

The PCD3344 family has 22 I/O lines arranged as:

- Port 0 parallel port of 8 lines (P00 to P07)
- Port 1 parallel port of 8 lines (P10 to P17)
- Port 2 parallel port of 4 lines (P20 to P23)
- CE/$\overline{T0}$ external interrupt and test input. When used as a test input it can be directly tested by conditional branch instructions JT0 and JNT0.
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional. Output data written to a port is latched and remains unchanged until rewritten. Input data is not latched and so must be present until read by an input instruction.

Input lines are fully CMOS compatible, output lines can drive one LS-TTL or CMOS load.

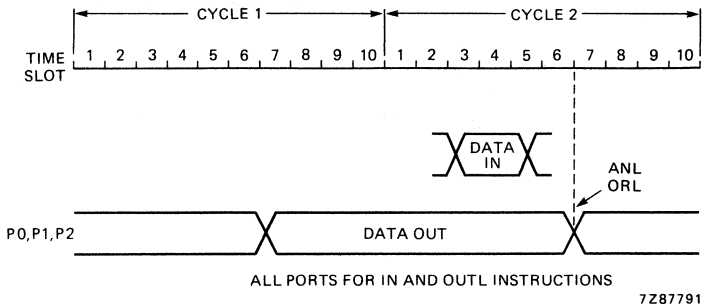


Fig. 9 Timing diagram of all ports on IN and OUTL instructions; for ANL and ORL instructions, the ports change on the time slot 7 of cycle 2.

Fig. 10 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source. Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current source provides sufficient current for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period) to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

In telephone applications this switched pull-up source may not be sufficient. Therefore the PCD3344 offers the possibility to select individually the 20 parallel port pins by the following mask options:

Option 1 – STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2 (1,5 mA). TR2 is active only during 1 clock cycle (0,28 μs at 3,58 MHz).

Option 2 – OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 11).

Option 3 – PUSH-PULL OUTPUT; drive capability of the output will be 1,5 mA (typ.) at V_{DD} = 3 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must be used only as outputs (Fig. 12).

Also, individual mask selection of the RESET state of these port pins can be achieved by appending the following options S and R to options 1, 2 or 3.

Option S-SET; after RESET this pin will be initialized to HIGH

Option R-RESET; after RESET this pin will be initialized to LOW.

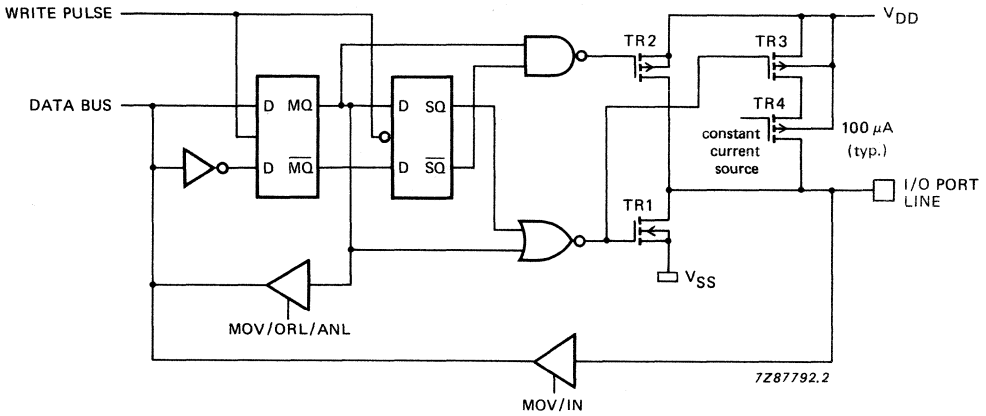


Fig. 10 Standard output with switched pull-up current source.

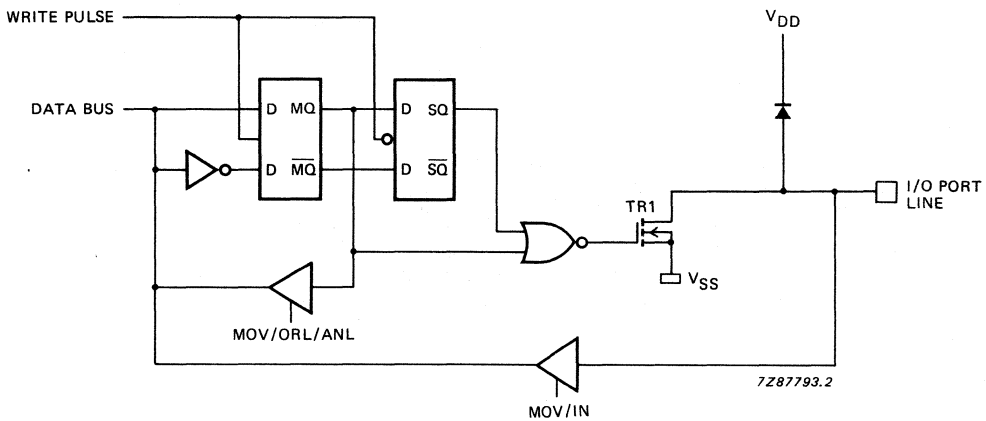


Fig. 11 Open drain output.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Parallel ports (continued)

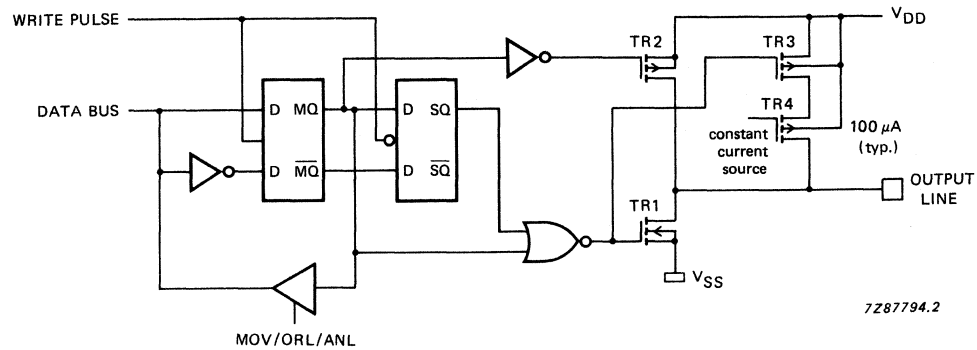


Fig. 12 Push-pull output.

Interrupts (see Fig. 13(a) and Fig. 13(b))

When an interrupt routine is entered, the contents of the program counter and bits 4, 6 and 7 of the PSW are saved in the program counter stack. The contents of the accumulator can only be saved by user software. Interrupt acknowledgement can be carried out by software via I/O ports. All interrupt routines must reside in memory bank 0; the SEL MB1, SEL MB2 and SEL MB3 instructions may not be used in an interrupt routine. An interrupt routine can only be terminated by the RETR (return and restore) instruction. During an interrupt routine, subroutine calls must be terminated by the RET instruction. Using the RETR instruction to terminate a subroutine called in an interrupt routine would terminate the interrupt routine prematurely and result in a wrong return address.

1. **External interrupt**

When the external interrupt is enabled, a HIGH-to-LOW transition on the CE/$\overline{TO}$ input initiates an external interrupt routine which forces a call to program memory location 3. The program counter points to the external interrupt vector address (003 H) between 2,6 and 3,6 machine cycles after the transition occurs. Interrupt latency depends on the instruction that is being executed when the transition occurs. External interrupts are latched in the External Interrupt Flag (EIF) even when they are not enabled. Execution of a DIS I instruction clears previously latched interrupts, the digital filter latch and the external interrupt flag.

2. **Timer/counter interrupt**

When the timer interrupt is enabled, a timer/counter overflow sets the Timer Interrupt Flag (TIF) and forces a CALL to location 7. The timer interrupts are only latched when they are enabled. The timer flag is set every time the timer/counter overflows and is not automatically reset when the timer/counter interrupt routine is called. It can only be cleared by the JTF and JNTF instructions or by a hardware RESET.

3. Simultaneous interrupts

If simultaneous interrupts occur their priority is as follows:

external (highest);
timer/counter (lowest).

An interrupt routine can only be interrupted by a hardware RESET and cannot be interrupted by other interrupts (which will be latched if enabled). When the interrupt routine is terminated by the RETR instruction, at least one instruction of the main program will be executed before another interrupt routine is entered.

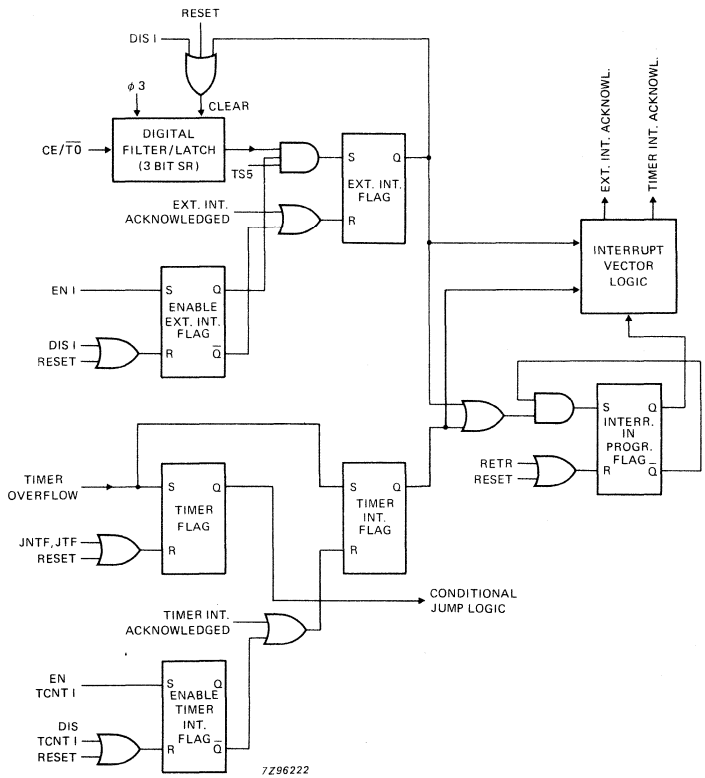


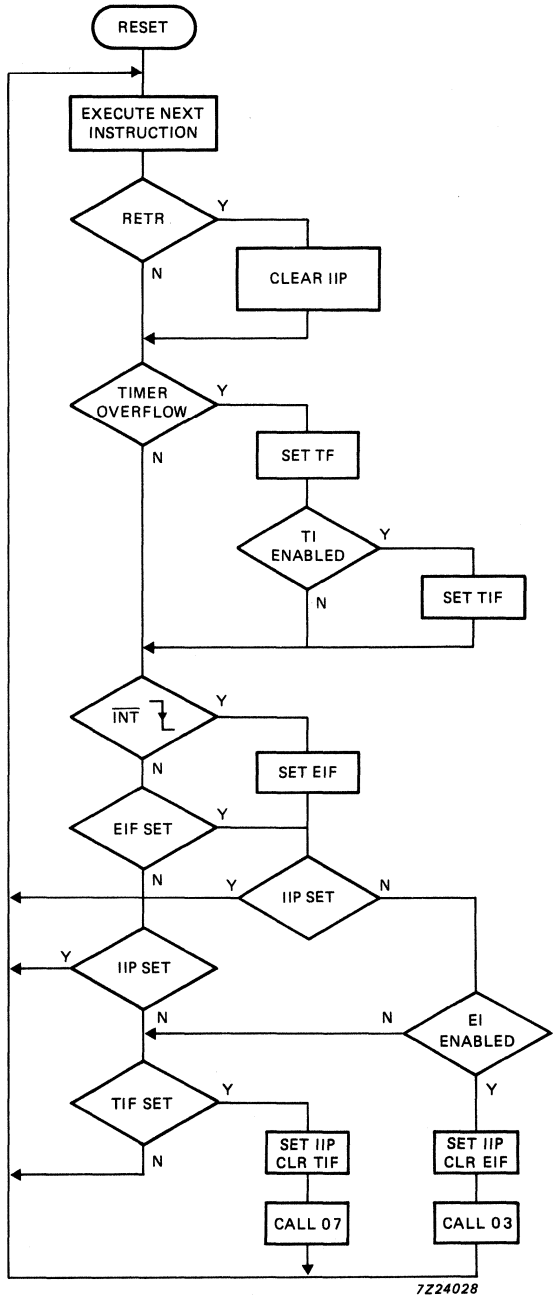
Fig. 13(a) Interrupt logic.

Notes to figure 13(a)

1. CE/$\overline{T0}$ positive edge is always latched in the digital filter/latch.
2. Correct interrupt timing is ensured when CE/$\overline{T0}$ is LOW for $>$ 4 CP followed by a HIGH for $>$ 7 CP.
3. When the interrupt in progress flag is set, further interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.
5. For all flip-flops, RESET overrules SET.

FUNCTIONAL DESCRIPTION (continued)

Interrupts (continued)



EI External Interrupt
TI Timer/counter Interrupt
EIF External Interrupt Flag
TF Timer Flag
IIP Interrupt In Progress flag

Fig. 13(b) Interrupt flowchart.

Oscillator (see Fig. 14)

The 3,58 MHz oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-voltage condition is present to prevent discharge of a weak back-up battery.

Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a HIGH level at either the CE/$\overline{T0}$ or RESET pin.

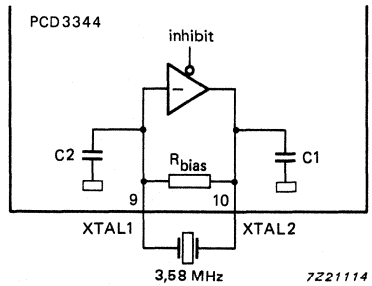


Fig. 14 Oscillator with integrated elements.

The oscillator has an output drive capability from pin 10 (XTAL2). An external clock can be applied to pin 9 (XTAL1). A machine cycle comprises 10 time slots, each time slot being 3 oscillator periods.

In telephony applications the 3,58 MHz crystal provides an 8,4 μs machine cycle. The range of the clock frequency is from 100 kHz up to a maximum which is a function of the supply voltage.

Timer/event counter (see Fig. 15)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 3 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin 8 (T1) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (182,6 kHz for an 8,4 μs machine cycle). When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump if timer flag = 1) or JNTF instruction. Overflow also generates an interrupt to the processor via setting of the Timer Interrupt Flag when the timer/event counter interrupt is enabled.

FUNCTIONAL DESCRIPTION (continued)

Timer/event counter (continued)

Table 3 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

* With prescaler select, PS = 0, the timer counts modulo-32 machine cycles, with PS = 1 it counts modulo-1 cycles (prescaler not used); prescaler cleared with STRT T, prescaler not readable.

** READ does not disturb the counting process.

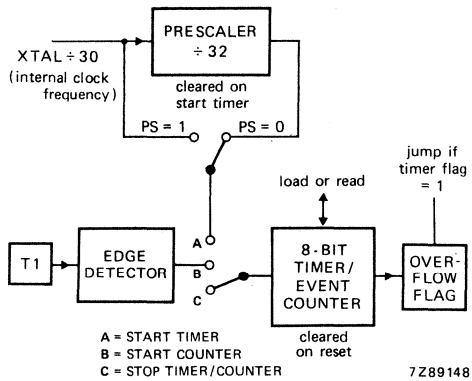


Fig. 15 Timer/event counter.

Program status word (see Fig. 16)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS); 0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS); 0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

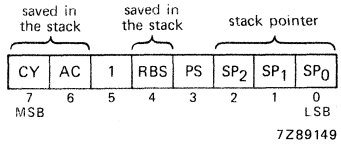


Fig. 16 Program status word.

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program counter (see Fig. 17).

A 12-bit program counter is used to facilitate 8 K bytes of ROM being addressed. The arrangement of the bits is shown in Figure 17. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 12 bits are saved in the stack during CALL and interrupt routines.

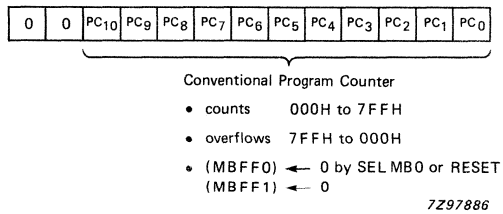


Fig. 17 Program counter.

Central processing unit

The PCD3344 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the CURRENT ROM page.

FUNCTIONAL DESCRIPTION (continued)

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program.
Table 4 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 4 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JNT0
	0	JT0*
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

* Because of the inverted interrupt input CE/$\overline{T0}$ the conditional jump JT0 is also inverted.

Test input T1 (pin 8)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for > 4 CP, followed by a HIGH for > 4 CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor ($R = \leqslant 100\ k\Omega$).
When T1 is not used pin 8 must be connected to V_{DD} or V_{SS}.

Reset (pin 11)

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory bank 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external and timer)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports according to reset states
- Cancels IDLE and STOP mode

After the voltage is applied to RESET an internal delay of 1866 CP is introduced before the microcontroller commences operation.

Power-on reset

The internal power-on reset circuit monitors the supply voltage V_{DD}. As long as V_{DD} remains below the internal reference level V_{ref} (typically 1,3 V), the oscillator is inhibited and RESET (pin 11) has an undefined level. When V_{DD} rises above V_{ref}, the oscillator is released and RESET is pulled HIGH to V_{DD} by TR1 for a period t_D (typically 50 μs). Note that the start-up time of the oscillator is typically 10 ms because of the narrow bandwidth of the crystal.

Three modes of power-on reset are possible:

1. If V_{DD} has a fast rise time, i.e. V_{DD} reaches its minimum value before the RESET signal finishes (t_D), then no additional circuit is required (see Figs 18 and 19). Note that the first instruction is executed after the oscillator start-up time plus 1866 clock periods.
2. If V_{DD} has a slow rise time then the RESET signal should be stretched by an external CR circuit (see Figs 20 and 21). In the event of a short drop in V_{DD}, the diode path discharges the capacitor rapidly to ensure a reliable power-on reset. The RESET signal should reach at least 70% of the final value of V_{DD} to ensure a correct reset. Given that the RESET voltage and V_{DD} rise exponentially, the above requirement is satisfied when the time constant of the RESET pulse is > 8 times the time constant of V_{DD}. If V_{DD} rises linearly then a RESET time constant > 2 times the rise time of V_{DD} is required.

   When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods (see Fig. 21). If the oscillator starts up prior to the completion of RESET then program execution begins 1866 clock periods after RESET goes LOW.
3. Fig. 22 shows an external reset applied during power-on. The external reset signal must remain HIGH until V_{DD} has reached its minimum operating value corresponding to the selected oscillator frequency. When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods (see Fig. 23). If the oscillator starts up prior to the completion of RESET then program execution begins 1866 clock periods after RESET goes LOW.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

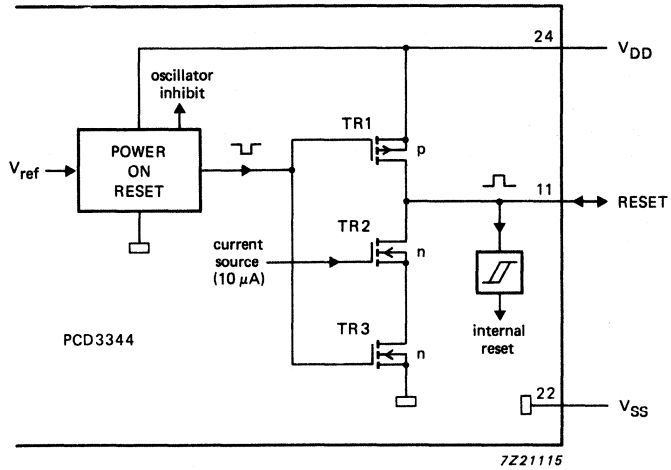


Fig. 18 Power-on reset configuration.

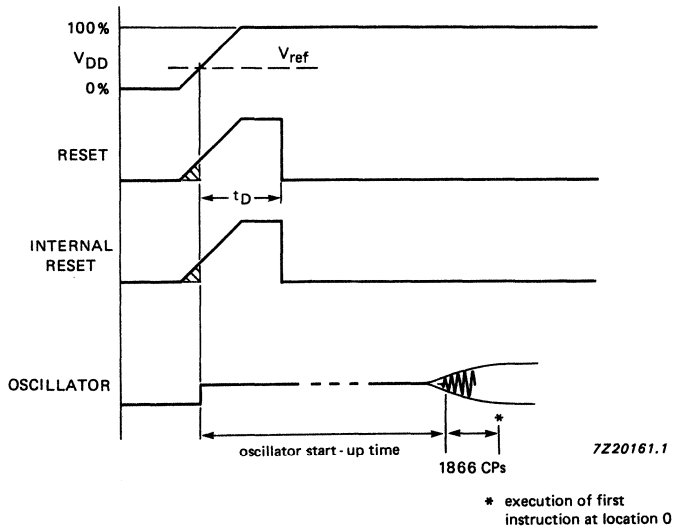


Fig. 19 Timing of power-on reset with fast rise time of V_{DD}.

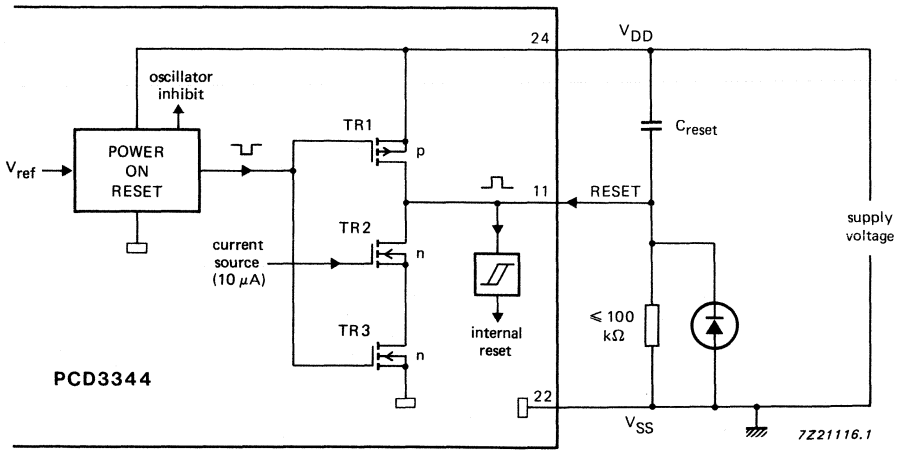


Fig. 20 Stretched power-on reset with external CR circuit.

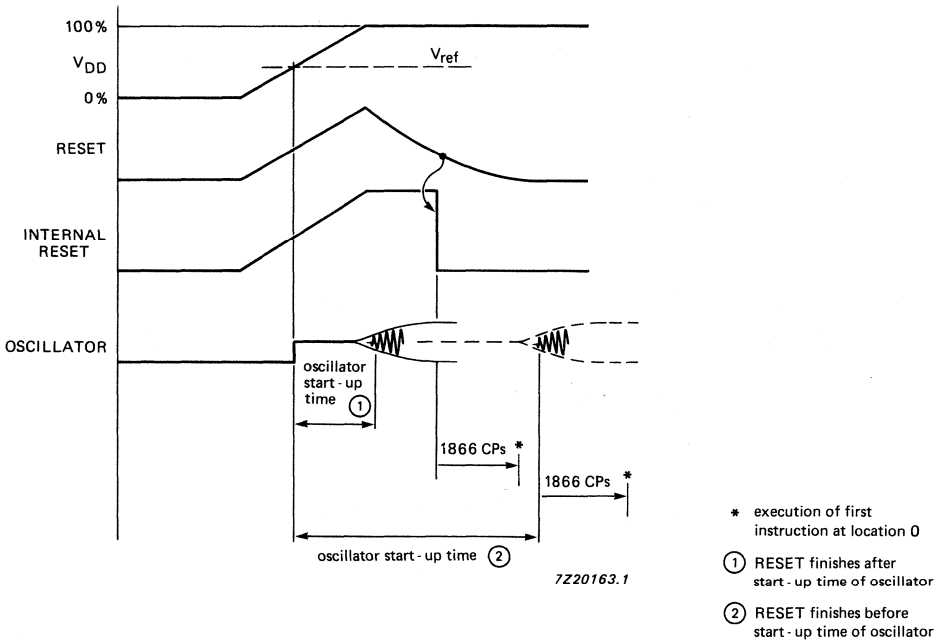


Fig. 21 Timing of power-on reset with a slowly rising V_{DD} and a stretched RESET pulse.

FUNCTIONAL DESCRIPTION (continued)

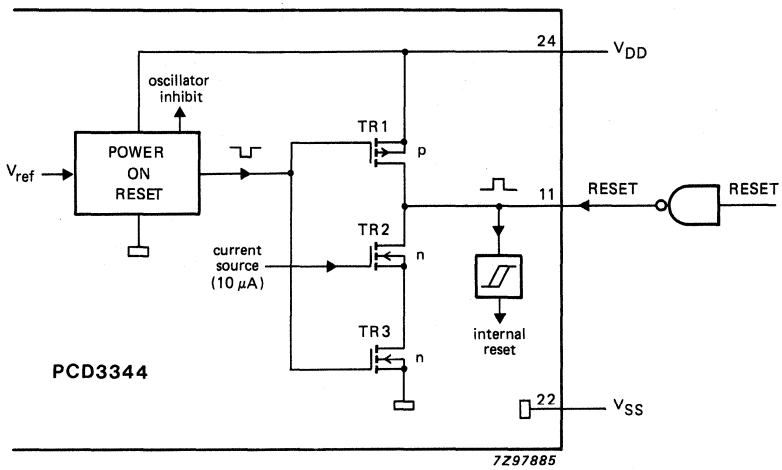


Fig. 22 External power-on reset configuration.

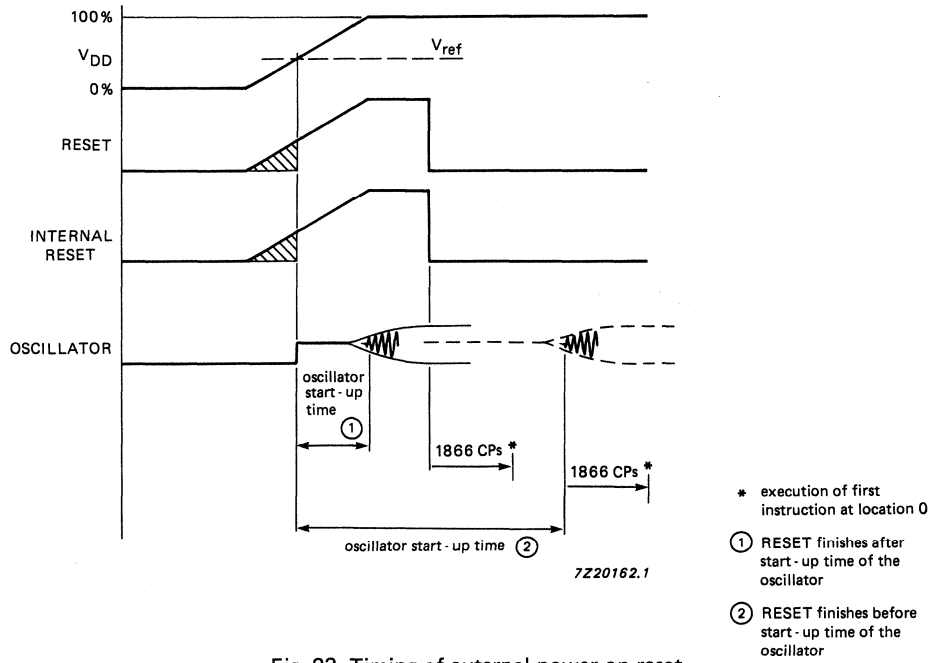


Fig. 23 Timing of external power-on reset.

INSTRUCTION SET

The PCD3344 instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for memory bank selection and derivative control. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 5 details the symbols and definition descriptions that are used in the instruction set of the PCD3344. Table 6 shows the instruction map and Table 7 gives the instruction set.

Table 5 Symbols and definitions used in Tables 6 and 7

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0 to 7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
D	mnemonic for 4-bit digit (nibble)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0 to 7)
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
Dx	derivative register (0 to H'FF')
←	is replaced by
↔	is exchanged with

INSTRUCTION SET (continued)

Table 6 PCD3344 instruction map

first hexadecimal character of opcode ↓

second hexadecimal character of opcode →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, # data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0 | 1 | 2							
1	INC @Rr 0 | 1		JB0 addr	ADDC A, # data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0	1	2	3	4	5	6	7
2	XCH A,@Rr 0 | 1		STOP	MOV A, # data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A,Rr 0	1	2	3	4	5	6	7
3	XCHD A,@Rr 0 | 1		JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A 0	1	2					
4	ORL A,@Rr 0 | 1		MOV A , T	ORL A, # data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0	1	2	3	4	5	6	7
5	ANL A,@Rr 0 | 1		JB2 addr	ANL A, # data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0	1	2	3	4	5	6	7
6	ADD A,@Rr 0 | 1		MOV T , A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0	1	2	3	4	5	6	7
7	ADDC A,@Rr 0 | 1		JB3 addr		CALL page 3			RR A	ADDC A,Rr 0	1	2	3	4	5	6	7
8				RET	JMP page 4				ORL Pp, # data 0 | 1 | 2					MOV Dx,A		
9			JB4 addr	RETR	CALL page 4		JNZ addr	CLR C	ANL Pp, # data 0 | 1 | 2							
A	MOV @Rr, A 0 | 1			MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0	1	2	3	4	5	6	7
B	MOV @Rr, # data 0 | 1		JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr, # data 0	1	2	3	4	5	6	7
C	DEC @Rr 0 | 1				JMP page 6	SEL RB0	JZ addr	MOV A, PSW	DEC Rr 0	1	2	3	4	5	6	7
D	XRL A,@Rr 0 | 1		JB6 addr	XRL A, # data	CALL page 6	SEL RB1		MOV PSW, A	XRL A,Rr 0	1	2	3	4	5	6	7
E	DJNZ @Rr,addr 0 | 1				JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr 0	1	2	3	4	5	6	7
F	MOV A,@Rr 0 | 1		JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0	1	2	3	4	5	6	7

Table 7 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

INSTRUCTION SET (continued)

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1})\leftarrow A_n$ $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data	r = 0–7	
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((R0_{0-3}))$ $(A_{0-3})\leftrightarrow((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3)\leftarrow(A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7})\leftarrow(A)$, $(A)\leftarrow((PC))$		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

DEVELOPMENT DATA

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1	
BRANCH	JMP addr	● 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0 address	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1 address			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0 : (PC_{0-7})←addr	
	JT0 addr	36 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JNT0 addr	26 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

INSTRUCTION SET (continued)

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4,6,7}$) (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) – 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) – 1 ($PSW_{4,6,7}$) + (PC)←((SP))	6

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
DERIVATIVE INPUT/OUTPUT	MOV Dx, A	8D	2/2	move accumulator contents to derivative register	(Dx)←(A) x = 0 to 255	8
	NOP	00	1/1	no operation		

Notes to Table 7

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).
5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 0000P23, P22, P21, P20.
8. Instructions for PCF84C00 only.

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 24	V_{DD}	−0,8	+8	V
Input voltage	any pin	V_I	−0,8	V_{DD} + 0,8	V
DC current	any input or output	$\pm I_I, \pm I_O$	–	10	mA
Total power dissipation	derate according to thermal resistance	P_{tot}	–	500	mW
Power dissipation	per output	P_O	–	50	mW
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−25	+70	°C
Operating junction temperature		T_j	–	+125	°C
Thermal resistance junction to ambient	SOT117	$R_{th\ j\text{-}a}$	–	120	K/W
	SOT136A	$R_{th\ j\text{-}a}$	–	150	K/W

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 100 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage operating		V_{DD}	2,5	–	6	V
STOP mode for RAM data retention		V_{DD}	1,0	–	6	V
Supply current (Fig. 25)						
operating with tone generator on	V_{DD} = 3 V	I_{DD}	–	1,2	–	mA
operating without tone generator	V_{DD} = 3 V	I_{DD}	–	600	–	μA
IDLE mode (Fig. 26)						
with tone generator on	V_{DD} = 3 V	I_{DD}	–	900	–	μA
without tone generator	V_{DD} = 3 V	I_{DD}	–	300	–	μA
STOP mode (Fig. 27)	note 1; V_{DD} = 1,8 V					
	T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
	T_{amb} = 55 °C	I_{DD}	–	–	5	μA
	T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O						
Switching level		V_{RESET}	–	1,3	–	V
Sink current	$V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs						
Input voltage LOW		V_{IL}	0	–	0,3 V_{DD}	V
Input voltage HIGH		V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Input leakage current	$V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs						
Output voltage LOW	V_I = V_{SS} or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW P12, P13, P14, P20, P21, P22, P23, (Fig. 28)	V_{DD} = 3 V; V_O = 0,4 V	I_{OL}	0,7	1,5	–	mA
for remaining ports (Fig. 29)	V_O = 0,4 V	I_{OL}	1,5	–	–	mA
Pull-up output source current HIGH (Fig. 30)	V_{DD} = 3 V;					
	V_O = 0,9 V_{DD}	$-I_{OH}$	10	–	–	μA
	V_O = V_{SS}	$-I_{OH}$	–	–	300	μA
Push-pull output source current HIGH	V_{DD} = 3 V;					
	V_O = V_{DD} −0,4 V	$-I_{OH}$	0,6	1,5	–	mA

Note 1

Crystal connected between XTAL1 and XTAL2; CE and T1 at V_{SS}.

TONE GENERATOR CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 100 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Tone output (Fig. 24)						
DTMF output voltage levels (r.m.s. values)						
HIGH group		$V_{HG(rms)}$	158	192	205	mV
LOW group		$V_{LG(rms)}$	125	150	160	mV
Frequency deviation		$\Delta f/f$	−0,6	–	+ 0,6	%
DC voltage level		V_{dc}	–	½ V_{DD}	–	V
Output impedance		$\|Z_O\|$	–	0,1	0,5	kΩ
Pre-emphasis of group		ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion	note 2; T_{amb} = 25 °C	THD	–	−25	–	dB

Note 2

Related to the level of the LOW group frequency component (CEPT CS 203)

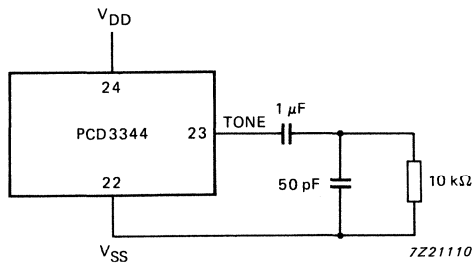


Fig. 24 Tone output test circuit.

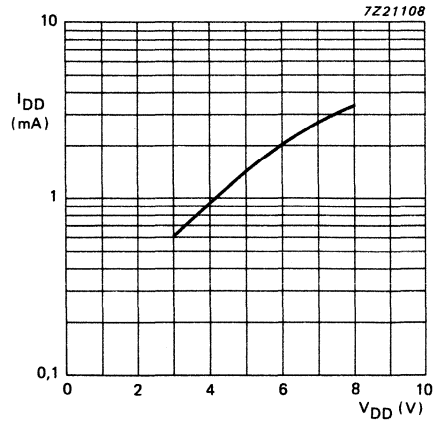


Fig. 25 Typical supply current (I_{DD}) in operating mode as a function of the supply voltage (V_{DD}); T_{amb} = 25 °C; clock frequency = 3,58 MHz; I_{DD} is increased by approximately 0,6 mA when the DTMF function is operating.

DEVELOPMENT DATA

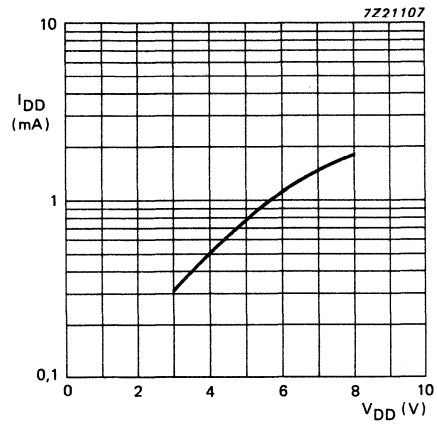
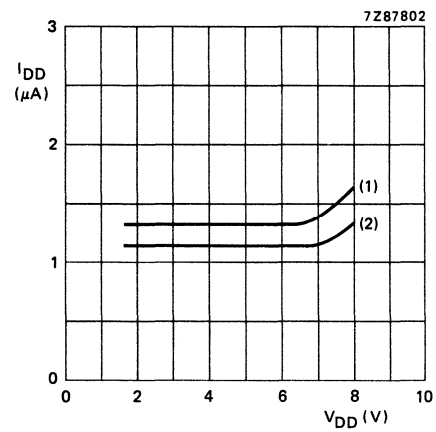
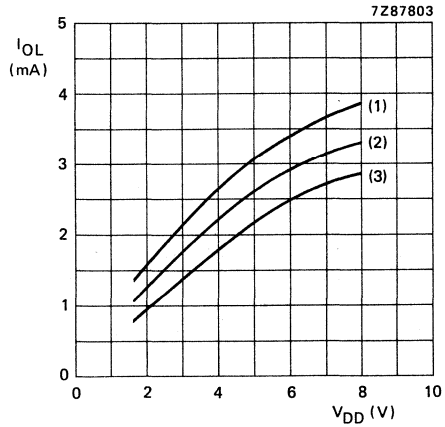


Fig. 26 Typical supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}); T_{amb} = 25 °C; clock frequency = 3,58 MHz.



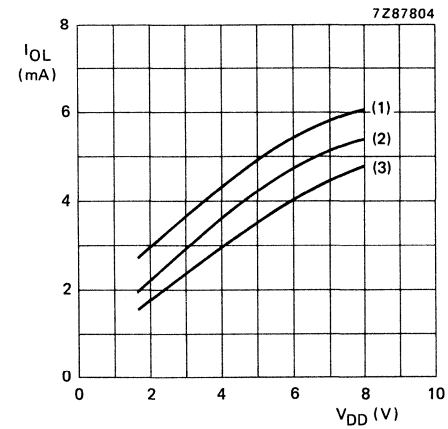
(1) T_{amb} = 25 °C
(2) T_{amb} = 70 °C

Fig. 27 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).



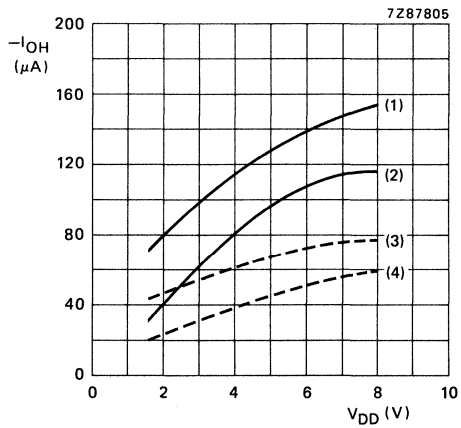
(1) $T_{amb} = -25$ °C
(2) $T_{amb} = 25$ °C
(3) $T_{amb} = 70$ °C

Fig. 28 Output sink current LOW (I_{OL}), for P12, P13, P14, P20, P21, P22, P23 as a function of supply voltage (V_{DD}); $V_O = 0{,}4$ V.



(1) $T_{amb} = -25$ °C
(2) $T_{amb} = +25$ °C
(3) $T_{amb} = +70$ °C

Fig. 29 Output sink current LOW (I_{OL}), for remaining ports as a function of supply voltage (V_{DD}); $V_O = 0{,}4$ V.



(1) $T_{amb} = 25$ °C; $V_O = V_{SS}$
(2) $T_{amb} = 25$ °C; $V_O = 0{,}9\ V_{DD}$
(3) $T_{amb} = 70$ °C; $V_O = V_{SS}$
(4) $T_{amb} = 70$ °C; $V_O = 0{,}9\ V_{DD}$

Fig. 30 Output source current HIGH ($-I_{OH}$) as a function of supply voltage (V_{DD}).

APPLICATION INFORMATION

A block diagram of an electronic featurephone built around the PCD3344 is shown in Figure 31. It comprises the following dedicated telephony ICs:

- TEA1060/1061/1067/1068 transmission circuit for telephony
- PCF8576 or PCF8577 2 LCD drivers in LCD module MB7020160
- PCF8571 1 K RAMs with Serial I/O; the number of RAMs depends on the required amount of stored telephone numbers
- PCD3360 programmable multi-tone ringer

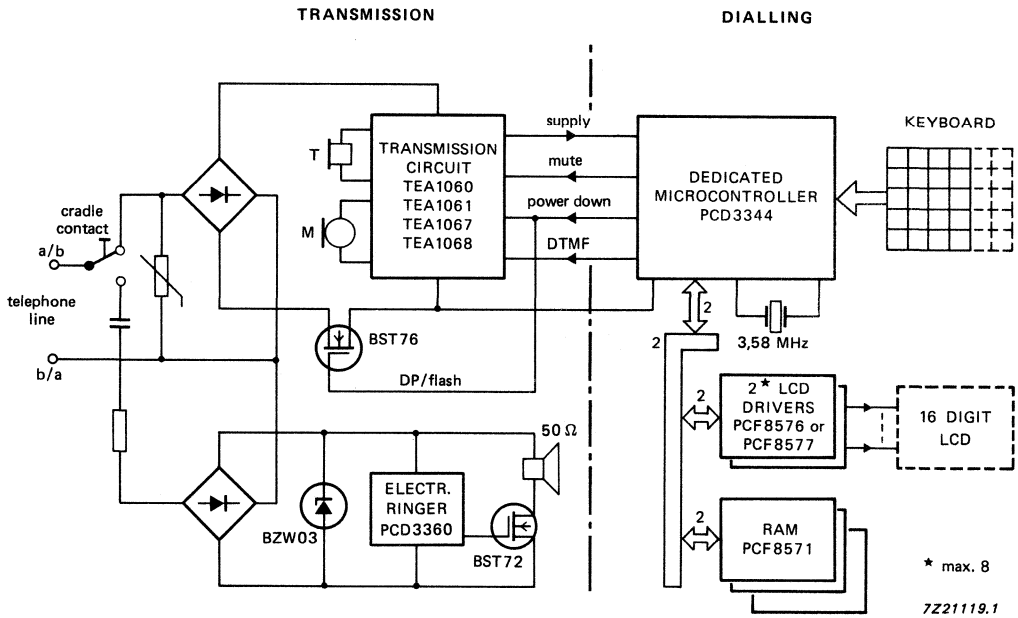


Fig. 31 Block diagram of electronic featurephone with common line interface.

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The PCD3346 is a single-chip 8-bit microcontroller manufactured in CMOS technology. The PCD3346 is a member of the PCD33XX family and as such has special on-chip features for telephony applications.

The PCD3346 has 20 quasi-bidirectional I/O port lines, a serial I/O interface, a single-level vectored interrupt circuit, two 8-bit timer event counters and on-board clock oscillator and clock circuits. The PCD3346 also incorporates 256 bytes of EEPROM permitting intermediate data storage without the need for battery back-up.

The instruction set is based on that of the MAB8048 and is instruction set compatible with the MAB8400 family. The PCD3346 has bit handling abilities for both binary and BCD arithmetic.

Features

- 8-bit CPU, ROM, EEPROM, RAM, I/O in a single 28-lead DIL or SO package
- 4 K ROM bytes
- 128 RAM bytes
- 256 bytes EEPROM
- 20 quasi-bidirectional I/O port lines
- 2 x 8-bit programmable timers
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter, serial I/O and derivative port
- I^2C hardware interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- Clock frequency 450 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2.5 V to 6.0 V
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals (e.g. PCD3312 DTMF generator)
- Individual mask configuration of all port lines for: pull-up, push-pull or open drain
- Power-on-reset circuit and low supply voltage detection
- Individual mask selection of reset state for all ports
- Operating temperature range: −25 to + 70 °C

LIFE SUPPORT APPLICATIONS

This product is not designed for use in life support appliances, devices, or systems where malfunction of this product can reasonably be expected to result in personal injury. Philips customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PACKAGE OUTLINES

PCD3346P: 28-lead DIL; plastic (SOT117).
PCD3346T: 28-lead mini-pack; plastic (SO28; SOT136A).

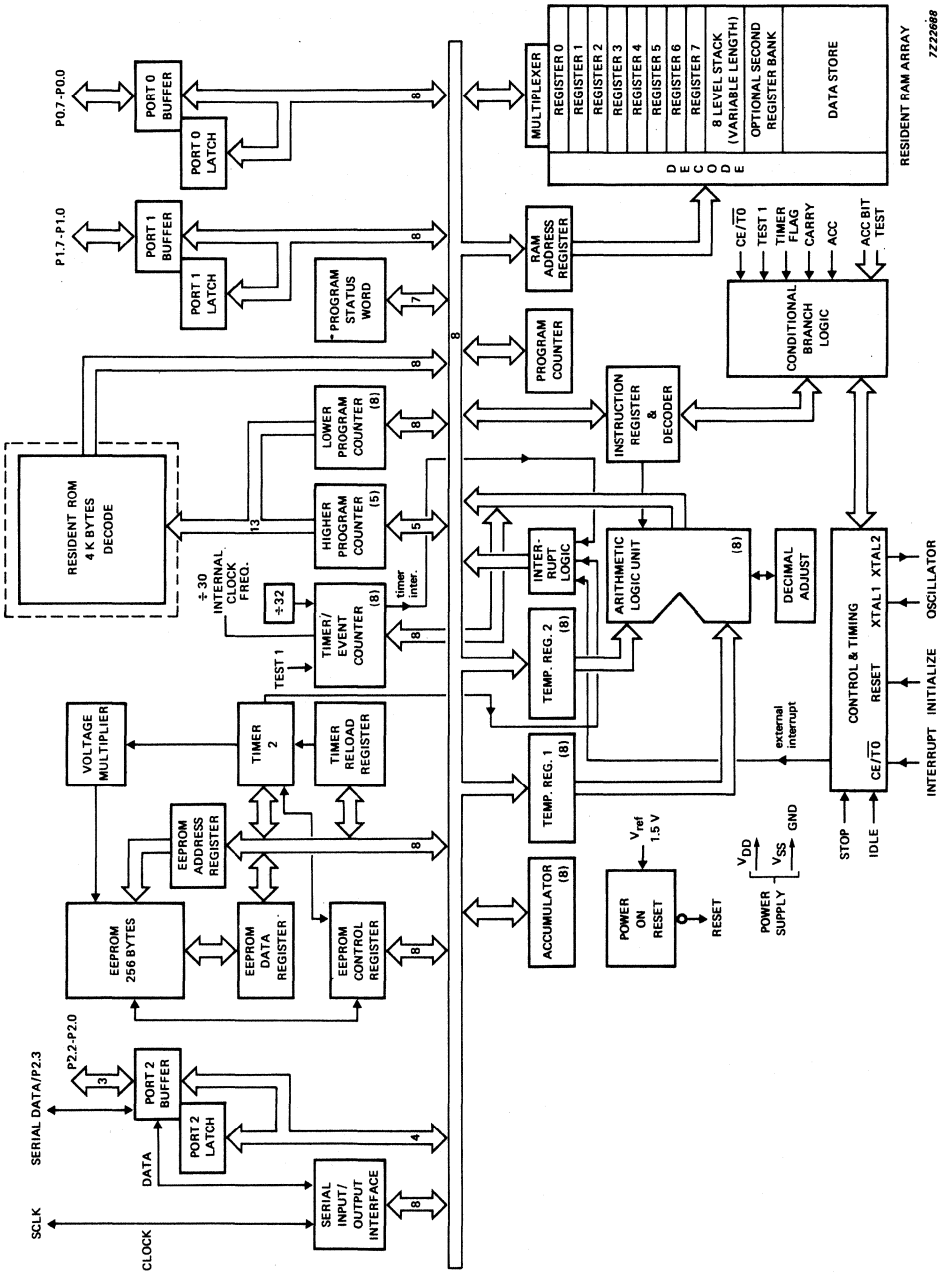


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

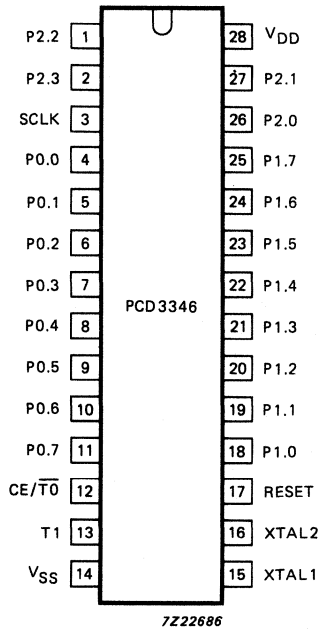


Fig. 2 Pinning diagram.

PIN DESIGNATION

Pin	symbol	type	function
3	SCLK	I/O	Clock: bidirectional clock for serial I/O.
4-11	P00-P07	I/O	Port 0: 8-bit quasi-bidirectional I/O port.
12	CE/$\overline{T0}$	I	Interrupt/Test 0: external interrupt input (sensitive to positive-going edge)/test input pin; when used as a test input directly tested by conditional branch instruction JT0 and JNT0.
13	T1	I	Test 1: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
14	V_{SS}	I	Ground: circuit earth potential.
15	XTAL1	I	Crystal input: connection to timing component (crystal) which determines the internal oscillator frequency; also the input for an external clock source.
16	XTAL2	I/O	Connection to other side of timing component.
17	RESET	I/O	Reset input: used to initialize the processor (active HIGH), or output of power-on-reset circuit.
18-25	P10-P17	I/O	Port 1: 8-bit quasi-bidirectional I/O port.
26,27, 1,2	P20-P23	I/O	Port 2: 4-bit quasi-bidirectional I/O port. P23 is the serial data input/output in serial I/O mode.
28	V_{DD}	I	Power supply: 2.5 V to 6.0 V.

FUNCTIONAL DESCRIPTION

Emulation of PCD3346

Emulation of the PCD3346 can be achieved using the piggyback version PCA3346B.

Program memory

The program memory consists of 4 K bytes, in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 3 shows the program memory map.

Four program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine,
- Location 5; contains the first byte of a serial I/O and derivative interrupt service subroutine,
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using the unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory

Data memory consists of 128 bytes, random-access data memory (RAM). Allocations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 4 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

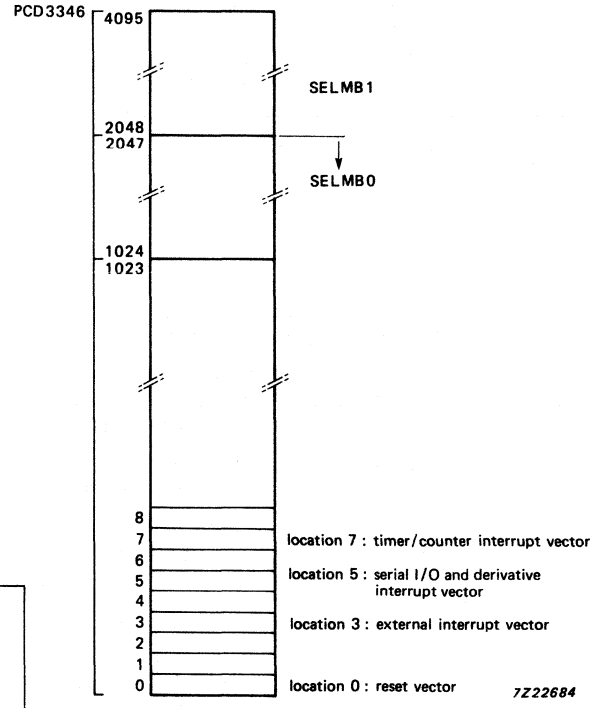


Fig. 3 Program memory map.

DEVELOPMENT DATA

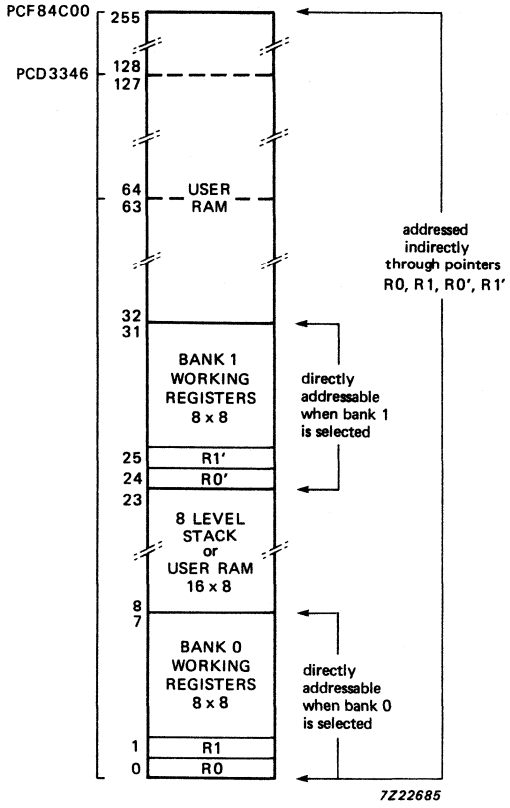


Fig. 4 Data memory map.

FUNCTIONAL DESCRIPTION (continued)

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 5) enables the microcontroller to keep track of the return addresses and status prior to interrupts or CALL instructions by storing the contents of the program counter before servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with the next return address and status.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11, ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If all 8 levels of subroutine and interrupt nesting are not used, the unused portion of the stack may be used as any other indirectly addressable RAM locations.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter during an interrupt CALL is not the same as the value saved during a normal CALL to subroutine. During an interrupt CALL, the program counter return address is saved; during a subroutine CALL, the saved program counter value is one less than the program counter return address.

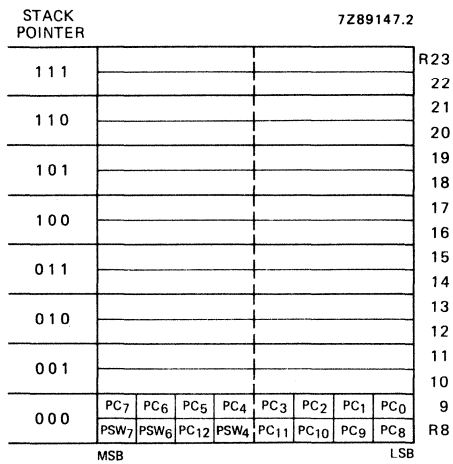


Fig. 5 Program counter stack.

EEPROM memory

The PCD3346 has 256 bytes of Electrically Eraseable Programmable Read Only Memory on-chip. On-chip EEPROM makes register retention possible without battery back-up. The 256 bytes of EEPROM are arranged as 64 pages. Each page is a single row of 32 bits, i.e. 4 bytes. This organisation makes it possible to read and erase/write in single page and byte mode. Addressing is performed on-chip using an 8-bit address decoder; the upper six bits select the page and the lowest two a byte on that page. The EEPROM address register is auto-incremented within the page which simplifies the read/write operation. Auto-increment is active during read and write functions, but is inactive during erase mode. Overflow during auto-increment leaves the register at 00000000.

The EEPROM is interfaced with the CPU via the derivative registers. Table 1 shows the instructions that control the derivative registers.

Table 1 Derivative register instruction set.

The PCD3346 has an additional 4 instructions to handle the derivative registers, these are:

Mnemonic	description	opcode (hex)	function x = 1 to 6
MOV A,Dx	move derivative register contents to accumulator	8C Dx	(A) <– (Dx)
MOV Dx,A	move accumulator contents to derivative register	8D Dx	(Dx) <– (A)
ANL Dx,A	AND derivative register with accumulator	8E Dx	(Dx) <– (Dx) AND (A)
ORL Dx,A	OR derivative register with accumulator	8F Dx	(Dx) <– (Dx) OR (A)

Each instruction is 2 cycles, 2 bytes. The second byte selects the derivative register to be manipulated (1 to 6) e.g. data transport from accumulator to derivative register D01 is performed by the two byte opcode 8 D 01.

For the PCD3346 six derivative registers are required and these are given in Table 2.

Table 2 PCD3346 derivative registers

name	derivative address	function
ADD1	01H*	contains the EEPROM array address
DATR	03H	contains the read or write data
EPCR	04H	EEPROM control register
RELR	05H	timer T2 reload
T2	06H	contents of timer T2

* For larger EEPROMs a second address register (ADD2) is necessary to accommodate the higher part of the EEPROM address. To ensure uniformity of derivative registers, a derivative address (02H) should be reserved for the high address part.

FUNCTIONAL DESCRIPTION (continued)

Table 3 EEPROM control register

EPCR (04H)	STT2	EIT2	TF2	EWP	MC3	MC2	MC1	MC0
	7	6	5	4	3	2	1	0

EPCR is a derivative R/W register containing the status of the EEPROM interface and timer T2.

Abbreviations used

Bit		Function
STT2	start timer T2	Setting this bit clears the pre-scaler and starts timer T2 in the general purpose mode. Timer T2 in the general purpose mode does not affect the EEPROM interface. T2 is loaded with the value in the RELR register at both start up and underflow. Setting STT2 to zero, stops Timer T2 and the pre-scaler, clears the pre-scaler and then reloads Timer T2.
EIT2	enable interrupt	When this bit is set and the SIO enabled, a derivative interrupt request is generated when TF2 is set. No interrupt request will be generated if EIT2 is set to zero.
TF2	timer flag T2	This bit is set by hardware when Timer T2 underflows and a derivative interrupt is requested if the SI is enabled (Fig. 6). TF2 must be cleared by software.
EWP	erase/write cycle in progress	This bit is set by software at the beginning of an erase or write cycle in the byte mode. It must be set by software in the page mode. It is cleared by hardware when the erase or write cycle has expired.
MCn	mode control bits	Four bits which control the working mode of the EEPROM. The truth table is given in Table 4.

Table 4 Truth table for EEPROM interface control bits

EWP	MC3	MC2	MC1	MC0	function
0	0	0	0	0	read byte
1	0	1	1	0	write byte
1	1	0	0	1	erase/write byte
1	1	1	0	0	erase page
0/1*	0	1	0	1	write page
1	1	0	1	0	erase bulk

Other bit patterns have no effect upon the interface. Bits MC3 to MC0 can be read and written by software, but are also cleared by hardware after each erase or write cycle has expired.

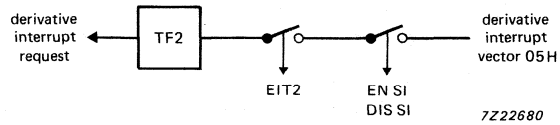


Fig. 6 Organization of a derivative interrupt.

Timer T2

Timer T2 determines the period of the erase and write timing cycles. Both times are the same, and are required to be of a fixed duration independent of the oscillator frequency. This requirement is fulfilled by T2 which is programmable timer with reload register RELR. Timer T2 is clocked via a 4-bit pre-scaler, which in turn is serviced by the processor clock ($f_{osc}/30$).

This means that T2 is decremented every 480 oscillator periods.
Erase and write times are both of **10 ms duration. The value for the RELR is to be calculated according** to the following formula. Table 5 gives examples of the RELR values for different XTAL frequencies.

$$(RELR) = \frac{f_{XTAL}}{480} \cdot 10\ ms$$

RELR is a R/W derivative register. At the beginning of a read/write cycle, Timer 2 is loaded with the contents of RELR and the count started. Underflow of the timer signals that the erase cycle has finished and that Timer T2 is reloaded once more with the contents of RELR. The next underflow will signify the end of the write cycle and the counter will be switched off. Erase and write times are both of **10 ms duration.**

* EWP = 0 selects write page mode, EWP = 1 executes write page.

FUNCTIONAL DESCRIPTION (continued)

Table 5 RELR values for various XTAL frequencies

f_{xtal}	timer 2 clocking (after 4-bit pre-scaler)	RELR value for 10 ms duration
450 kHz	1.1 ms	10
1 MHz	0.48 ms	21
3.58 MHz	0.134 ms	75
10 MHz	0.048 ms	209

Timer T2 may also be used as a general purpose timer. It is started by setting the STT2 bit in register EPCR, which loads the contents of RELR into the timer. At overflow, the interrupt flag T2 is set and the timer auto-reloaded with RELR. Timer T2 can be read "on-the-fly" and is addressed as derivative register T2. The following instructions demonstrate control of the timer in the general purpose mode.

```
                        ; TF2 must be cleared
MOV A, #_timevalue      ; time to be down-counted
MOV RELR, A             ; load derivative register RELR
EN SI                   ; enable SI interrupt
MOV A, #STT2+EIT2       ; start counter and enable derivative interrupt
ORL EPCR, A             ; load status in derivative control register
```

When the timer underflows, an interrupt call to ROM address 5 will be generated (SI interrupt) and appropriate actions will be decided by software. The content of timer can only be read "on-the-fly" using the instruction MOV A, D6.

Read EEPROM

Reading data from the EEPROM is possible only when no erase/write action is in progress. The read operation of a data byte is performed as follows:

- load EEPROM address
- load EPCR (not necessary when the MCn bits are already set to read mode)
- read data register

A program example could be:

```
MOV A, #_address        ; load EEPROM read address
MOV ADD1, A             ; send address to ADD1 register
MOV A, DATR             ; load data from EEPROM to accumulator
MOV Rm, A               ; store data
```

After executing the third instruction, the ADD1 address register is auto-incremented and the next byte can be read by repeating the last two instructions.

The erase/write operation

There are five erase/write modes controlled by the MCn bits in register EPCR:

- write byte
- erase/write byte
- erase page
- write page
- erase bulk

Each write or erase action takes 10 ms, this value must be loaded into the RELR register before starting any write/erase action, e.g.:

```
MOV A, #_RELR value     ; load appropriate 10 ms value according to fXTAL
                        ; frequency into accumulator
MOV RELR, A             ; load RELR register
```

A new erase or write operation can be started if no previous erase or write operation is in progress.

Write byte

A write operation may be started only if the addressed byte has been erased. The write operation is as follows:

- load EEPROM address
- load data
- load EPCR

The last instruction sets the operation mode and starts Timer T2, the address register is incremented and an interrupt is generated when the 10 ms count is reached.

Erase/write byte

The erase/write operation clears the addressed byte and writes the new. The erase/write operation is as follows:

- load EEPROM address
- load data
- load EPCR

The last instruction sets the operation mode and starts Timer T2, the address register is incremented and an interrupt is generated when the 2 x 10 ms count is reached.

Erase page

In this mode a complete four byte page will be erased. This operation requires only that the first byte of the page be addressed, after which the entire page will be erased. The erase page operation is as follows:

- load EEPROM with address of first byte of any page
- load EPCR

The last instruction starts Timer T2 and an interrupt is generated after the 10 ms period has elapsed.

FUNCTIONAL DESCRIPTION (continued)

* Piggybacks and SDS probes only (it is recommended to do it always, also for ROM code).

If the EPCR-register is checked before any erase/write operation, a dummy read of the EEPROM data register is neccessary for technical reasons. Please note that the EEPROM address register ADD1 will be autoincremented by one due to the dummy read.

Example.

```
LABEL1      MOV A, D4                    ; EPCR check
            test EWP- bit, jump to LABEL1 ; busy wait
            MOV A, D3                    ; dummy read
            .
            .
            MOV A, value                 ; choose e/w operation
            MOV D4, A                    ; start e/w operation
```

Write page

A write page operation can only be started if the addressed page is empty (erased). If the page is not empty an erase page must be executed beforehand. The write page operation is as follows:

- load EPCR (select write page mode)
- load ADD1 with address of first byte of any page
- load four data bytes (EEPROM address register auto-increments after each load except after fourth byte*)
- load EPCR (start write page)

The last instruction starts Timer T2 and an interrupt is generated after the 10 ms period has elapsed.

Given that an erase page cycle has been executed, a write page program is as follows:

```
MOV A, #MC2+MC0          ;
MOV EPCR, A              ; select write page mode
MOV A, #_address         ; EEPROM start address to accumulator
MOV ADD1, A              ; address to derivative address register

MOV A, R1                ; byte to be written to accumulator
MOV DATR, A              ; write 1st byte, address register auto-incremented
MOV A, R2                ; byte to be written to accumulator
MOV DATR, A              ; write 2nd byte, address register auto-incremented
MOV A, R3                ; byte to be written to accumulator
MOV DATR, A              ; write 3rd byte, address register auto-incremented
MOV A, R4                ; byte to be written to accumulator
MOV DATR, A              ; write 4th byte

MOV A, #EWP+MC2+MC0      ; set write page mode and execute bit in accumulator
MOV EPCR,A               ; start cycle
```

The last instruction sets the operation mode and starts Timer T2, the address register is incremented and an interrupt is generated at Timer T2 underflow.

* Note that data cannot be addressed (read or write) over a page limit.

Bulk erase

In the bulk erase mode the complete EEPROM is erased. The bulk erase operation is as follows:

– Load EPCR.

After start of bulk erase Timer T2 is started and an interrupt is generated at underflow. Below is an example of a program for a bulk erase:

```
MOV A,#EWP+MC3+MC1      ; set the bulk erase mode in accumulator
MOV EPCR,A              ; load EPCR and start erase cycle
```

Timer T2 is started and an interrupt is generated at Timer T2 underflow.

FUNCTIONAL DESCRIPTION (continued)

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (01H), the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode via a RESET or one of three interrupts if they are enabled. If the interrupt is not enabled, the microcontroller will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 7).

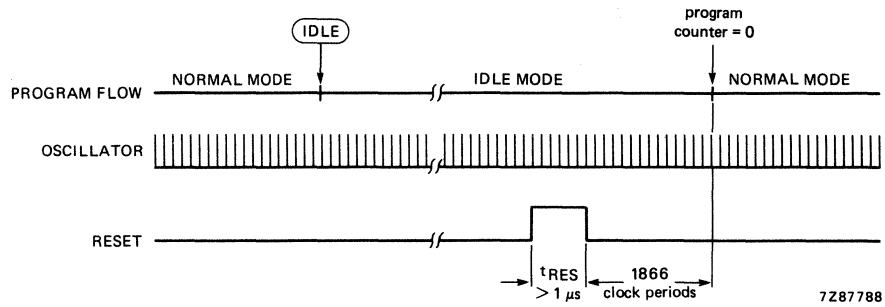


Fig. 7 Exit from IDLE mode via a RESET.

Any erase/write cycle in progress during IDLE mode will be completed. The interrupt request generated at the end of the erase/write cycle, if enabled, wakes up the microcontroller returning it to the normal mode.

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A LOW to HIGH transition on the external interrupt pin (CE/$\overline{TO}$) reactivates the microcontroller. A HIGH level applied to CE/$\overline{TO}$ will reactivate the microcontroller only in the STOP mode. Thus if CE/$\overline{TO}$ was HIGH before the microcontroller entered the IDLE mode, it must go LOW before the microcontroller can be reactivated (see fig. 8).

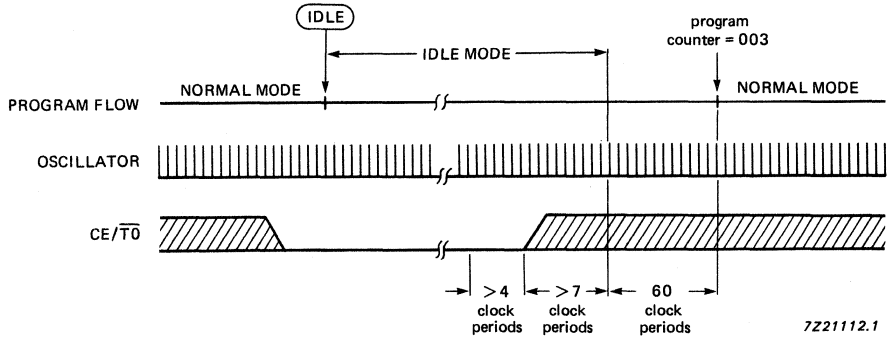


Fig. 8 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when CE/$\overline{T0}$ is LOW for at least 4 CP (clock periods) and then HIGH for 7 CP. After the initial forced CALL 003H operation (60 CP), the program continues with the external interrupt service routine. During the STOP mode, the address of the instruction immediately following the instruction that caused the microcontroller to enter the IDLE mode is present on the address bus.

STOP mode

Before entering the STOP mode bit EWP of the EPCR register must be set to logic 0.

The microcontroller enters the STOP mode via the STOP instruction (22H). The oscillator is switched off and the internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied, an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 9).

Note: the start-up time of a crystal oscillator is measured in milliseconds, and the 1866 CP count begins after this start-up time.

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

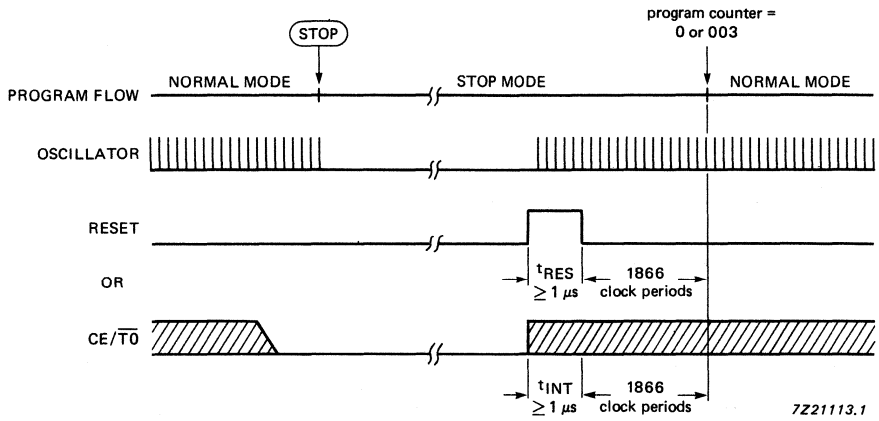


Fig. 9 Entering and exiting the STOP mode.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin HIGH, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a HIGH level applied at the CE/$\overline{T0}$ pin.
Note: When exiting the STOP mode via an interrupt, a further instruction in the main program series is executed prior to entering the interrupt routine.

If the CE/$\overline{T0}$ level is active during the STOP instruction then no STOP is executed.

A HIGH level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode. During the STOP mode, the address of the instruction immediately following the last STOP instruction is present on the address bus.

FUNCTIONAL DESCRIPTION (continued)

I/O facilities

The PCD3346 has 23 I/O lines arranged as:

- Port 0 8-bit parallel port (P0.0 to P0.7)
- Port 1 8-bit parallel port (P1.0 to P1.7)
- Port 2 4-bit parallel port (P2.0 to P2.3)
- SCLK serial I/O clock line
- CE/$\overline{T0}$ external interrupt and test input. When used as a test input can be directly tested by conditional branch instructions JT0 and JNT0
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

Parallel ports

Parallel port lines can be individually configured as outputs or inputs; their structure is quasi-bidirectional. Output data written to a port is latched and remains unchanged until rewritten. Input data is not latched and must be present until read by an input instruction.

Input lines are fully CMOS compatible; output lines can drive one TTL or CMOS load.

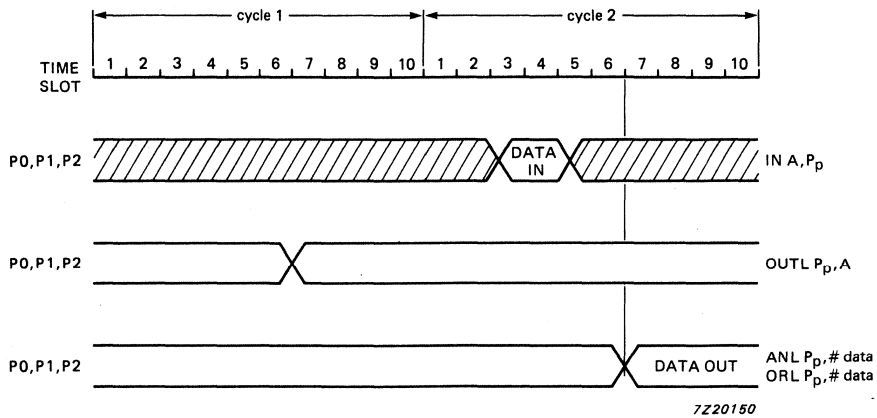


Fig. 10 Timing diagram for all ports using IN, OUTL, ANL and ORL instructions.

Figure 10 shows the timing diagram for all ports using IN, OUTL, ANL and ORL instructions. For the OUTL instruction data changes on time slot 7 of cycle 1. For the ANL and ORL instructions, the ports change on time slot 7 of cycle 2.

Figure 11 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source.

Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current source is sufficient for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

When a logic 1 is written to a port line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to a port line will not switch TR2 on. This ensures that the port lines can be pulled LOW when configured as inputs.

When a logic 0 is written to a port line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the port line; otherwise TR1 will remain low impedance.

PCD3346 mask options make it possible for each individual port line to be configured as one of the following:

1. STANDARD PORT: quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2. TR2 is only active during 1 clock cycle (Fig. 11).
2. OPEN DRAIN: quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 12). When an open drain port is unused it must be connected to V_{SS}.
3. PUSH-PULL OUTPUT: the outputs can sink or source 1,6 mA (min.) at V_{DD} = 5 V. These pins may not be used as inputs (Fig. 13). The contents of the port latch may be read using the IN A,pp instruction.

Individual mask selection of the pin's state following a RESET can be achieved by appending option S or R to options 1, 2 or 3.

Option S-SET; following RESET the pin will be set HIGH.

Option R-RESET; following RESET the pin will be set LOW.

DEVELOPMENT DATA

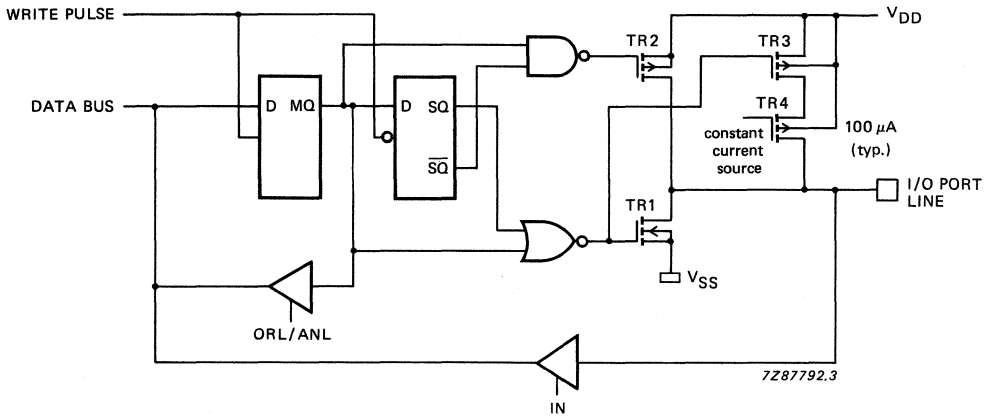


Fig. 11 Standard output with switched pull-up current source.

FUNCTIONAL DESCRIPTION (continued)

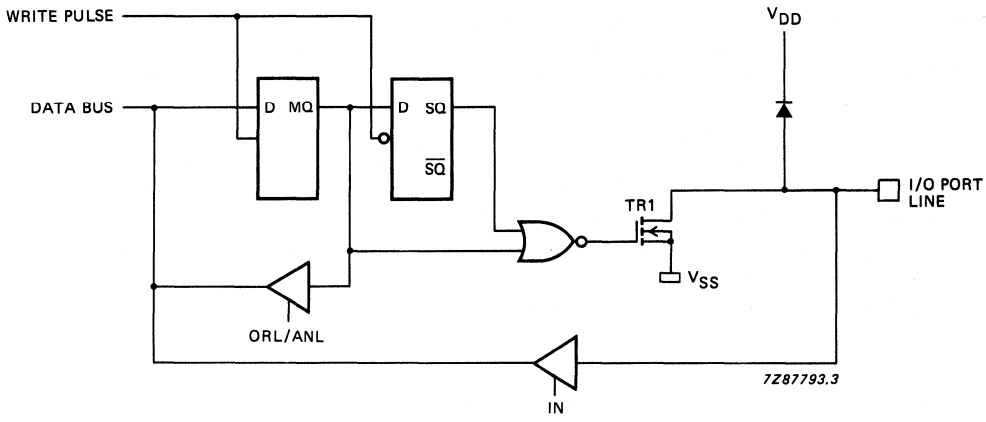


Fig. 12 Open drain output.

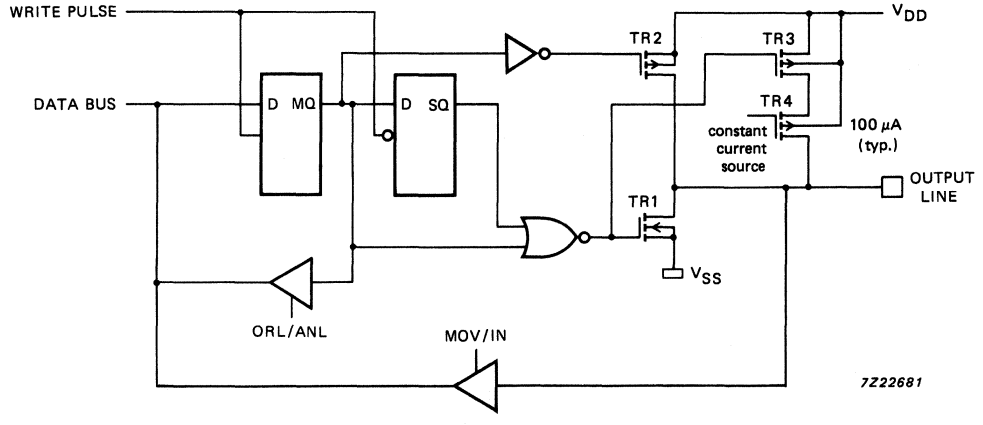


Fig. 13 Push-pull output.

Serial I/O (SIO)

The PCD3346 has an on-chip serial I/O interface tailored for I^2C-bus communications. The SIO interface is a versatile feature in intelligent telephone circuitry.

Where a normal microcontroller must regularly monitor the serial data bus for the presence of data, this serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the CPU only when a complete byte is received. It then reads the data byte in one instruction.

During transmission the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data. The microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

The design of the PCD3346 serial I/O system allows any number of devices from the PCF8500 family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCD3346 is switched off. This means that the serial I/O logic will remain in the state it was in when the STOP mode was entered. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction.

After a reset, the first 30 clock pulses of the 1866 pulse initiation phase reset the serial I/O interface and set P2.3/SDA and SCLK HIGH.

Serial I/O interface

Figure 14 shows the serial I/O interface. The clock line of the serial bus has exclusive use of the SCLK pin while the data line shares the SERIAL DATA pin with I/O line P2.3. When the serial I/O is enabled, P2.3 is disabled as a parallel port line; (P2.3 and SCLK are open drain; when unused these lines must be connected to V_{SS}).

FUNCTIONAL DESCRIPTION
(continued)

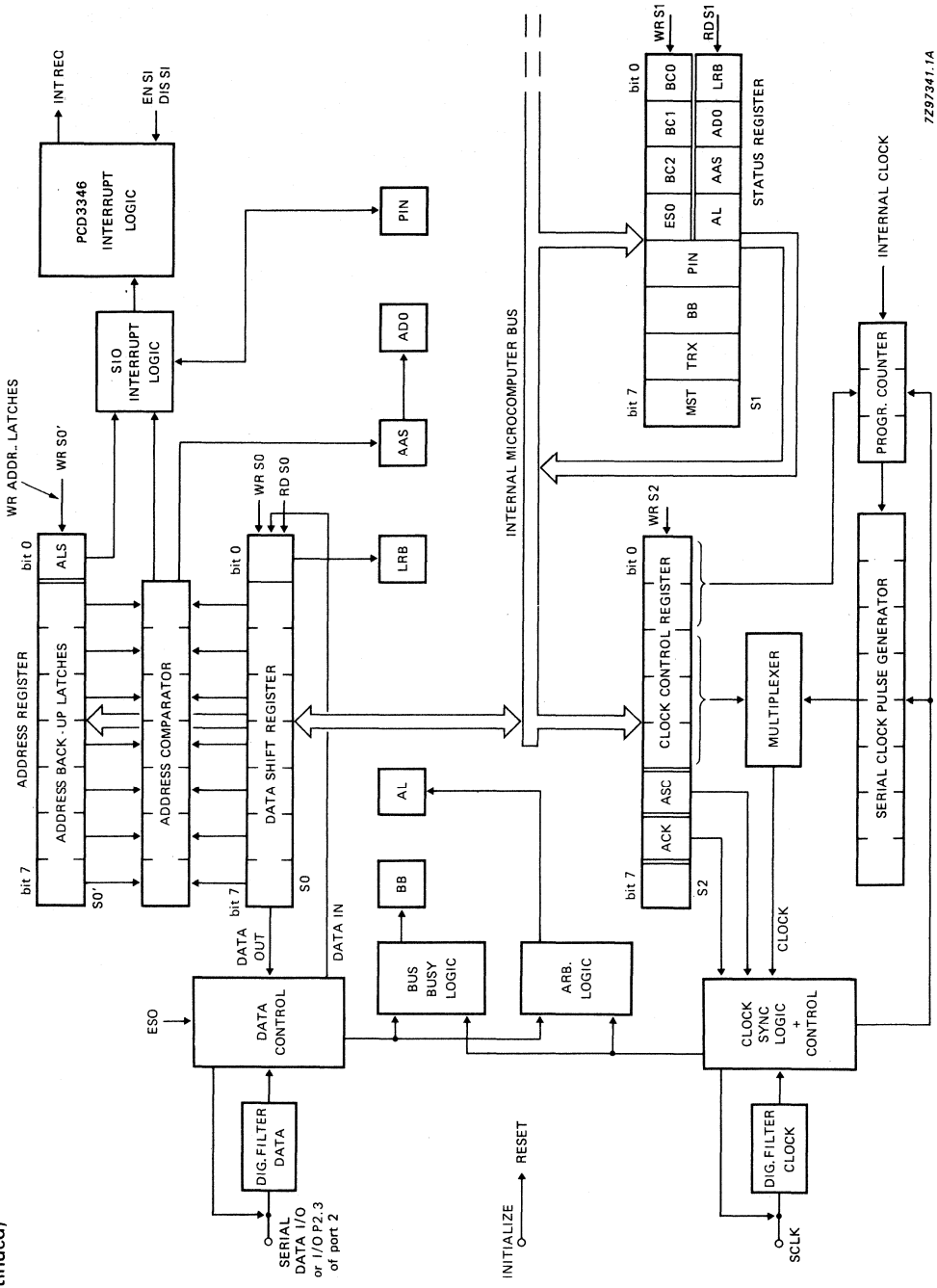


Fig. 14 Serial I/O interface.

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register (SO')

Data shift register (S0)

Register S0 converts serial data to parallel format and vice versa. An interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while status bits can only be read.

MST and TRX (see Table 6)

These bits determine the operating mode of the serial I/O interface.

Table 6 Operating modes of the serial I/O interface

MST	TRX	operating mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy.

This flag indicates the status of the bus.

PIN: Pending Interrupt NOT

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial output

The ESO flag enables/disables the serial I/O interface: ESO = '1' enables, ESO = '0' disables. ESO can only be written by software.

BC0, BC1 and BC2

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

FUNCTIONAL DESCRIPTION (continued)

AAS: Addressed As Slave

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

Serial clock control word (S2)

Bits 0 to 4 of the clock register S2 determine the frequency of the serial clock signal. When a 6 MHz crystal is used, the frequency of the serial clock can be varied between 1 kHz and 154 kHz (see Table 7). An asymmetrical clock with a HIGH-to-LOW ratio of 3 : 1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O. S2 is a write only register.

Address register (S0)

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, # data instructions, but only when ESO = logic 0.

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt request is still indicated by PIN in S1, but the interrupt will not be serviced.

DEVELOPMENT DATA

Table 7 SIO clock pulse frequency control when using a 3.58 MHz, 6 MHz or 10 MHz crystal

hexadecimal S20-S24 code	divisor	f_{XTAL} (3.58 MHz) f_{SCLK} (kHz) **	f_{XTAL} (6 MHz) f_{SCLK} (kHz) **	f_{XTAL} (10 MHz) f_{SCLK} (kHz) **
0	not allowed			
1	39	92	*154	*256
2	45	80	*133	*222
3	51	70	*118	*196
4	63	57	95	*159
5	75	48	80	*133
6	87	41	69	*115
7	99	36	61	*101
8	123	29	49	81
9	147	24	41	68
A	171	21	35	58
B	195	18	31	51
C	243	15	25	41
D	291	12	21	34
E	339	11	18	29
F	387	9.2	16	26
10	483	7.4	12	21
11	579	6.2	10	17
12	675	5.3	8.9	15
13	771	4.6	7.8	13.4
14	963	3.7	6.2	10.4
15	1155	3.1	5.2	8.7
16	1347	2.7	4.5	7.4
17	1539	2.3	3.9	6.5
18	1923	1.9	3.1	5.2
19	2307	1.6	2.6	4.3
1A	2691	1.3	2.2	3.7
1B	3075	1.2	2.0	3.3
1C	3843	0.93	1.6	2.6
1D	4611	0.78	1.3	2.2
1E	5379	0.67	1.1	1.9
1F	6147	0.58	1.0	1.6

* Not permitted for I^2C operation.

** Maximum clock frequency for the I^2C-bus is 100 kHz.

FUNCTIONAL DESCRIPTION (continued)

Interrupts

When an interrupt routine is entered, the contents of the program counter and bits 4, 6 and 7 of the PSW are saved in the program counter stack. The contents of the accumulator can only be saved by user software. Interrupt acknowledgement may be carried out by software via I/O ports. All interrupt routines must reside in memory bank 0; the SEL MB instructions may not be used within an interrupt routine. An interrupt routine can only be terminated by the RETR (return and restore) instruction. During an interrupt routine, subroutine calls must be terminated by the RET instruction. Using the RETR instruction to terminate a subroutine called in an interrupt routine would terminate the interrupt routine prematurely and result in a wrong return address.

External Interrupts

When the external interrupt is enabled and no interrupt routine is in progress, a LOW-to-HIGH transition on the CE/$\overline{T0}$ pin sets the External Interrupt Flag (EIF) and initiates the external interrupt routine by forcing a CALL to program memory location 3.* The program counter points to the external interrupt vector address (003 H) between 2,6 and 3,6 machine cycles after the transition occurs. Interrupt latency depends on the instruction that is being executed when the transition occurs. If an interrupt routine is already in progress, an external interrupt request is stored in the External Interrupt Flag (EIF). When the external interrupt has been disabled, the request is still latched into the digital filter. Execution of a DIS I instruction cancels stored interrupt requests by clearing both the digital filter latch and the external interrupt flag.

An additional external interrupt can be created by enabling the timer/counter interrupt and loading FFH into the counter (one less than overflow). If the event counter mode is enabled by executing the STRT CNT instruction, a LOW-to-HIGH transition on the T1 input will then initiate an interrupt routine by forcing a call to the timer/counter interrupt vector (location 7).

SIO Interrupt

An interrupt request from the SIO hardware will set the PIN flag to its active LOW state. This action is independent of the Enable SIO interrupt flag. When the SIO interrupt is enabled, the active LOW PIN flag will invoke the SIO interrupt routine by forcing a CALL to program memory location 5. After the SIO interrupt is initiated , the PIN flag is not automatically reset HIGH. PIN must be cleared by software during the interrupt routine.

Timer/Counter Interrupt

When no interrupt is in progress and the timer/counter is enabled, a timer/counter overflow sets the Timer Interrupt Flag (TIF). This initiates the timer interrupt routine by forcing a CALL to program memory location 7.** If an interrupt routine is in progress, the interrupt request is stored in the timer interrrupt flag only if the timer interrupt has been enabled. Execution of a DIS TCNTI instruction cancels a previously stored interrupt request. The timer flag (TF) is set every time the timer/counter overflows and is not automatically reset when the timer/counter interrupt routine is called. It can only be cleared by the JTF and JNTF instructions or by a hardware RESET.

* This CALL clears the EIF flag.
** This CALL clears the TIF flag.

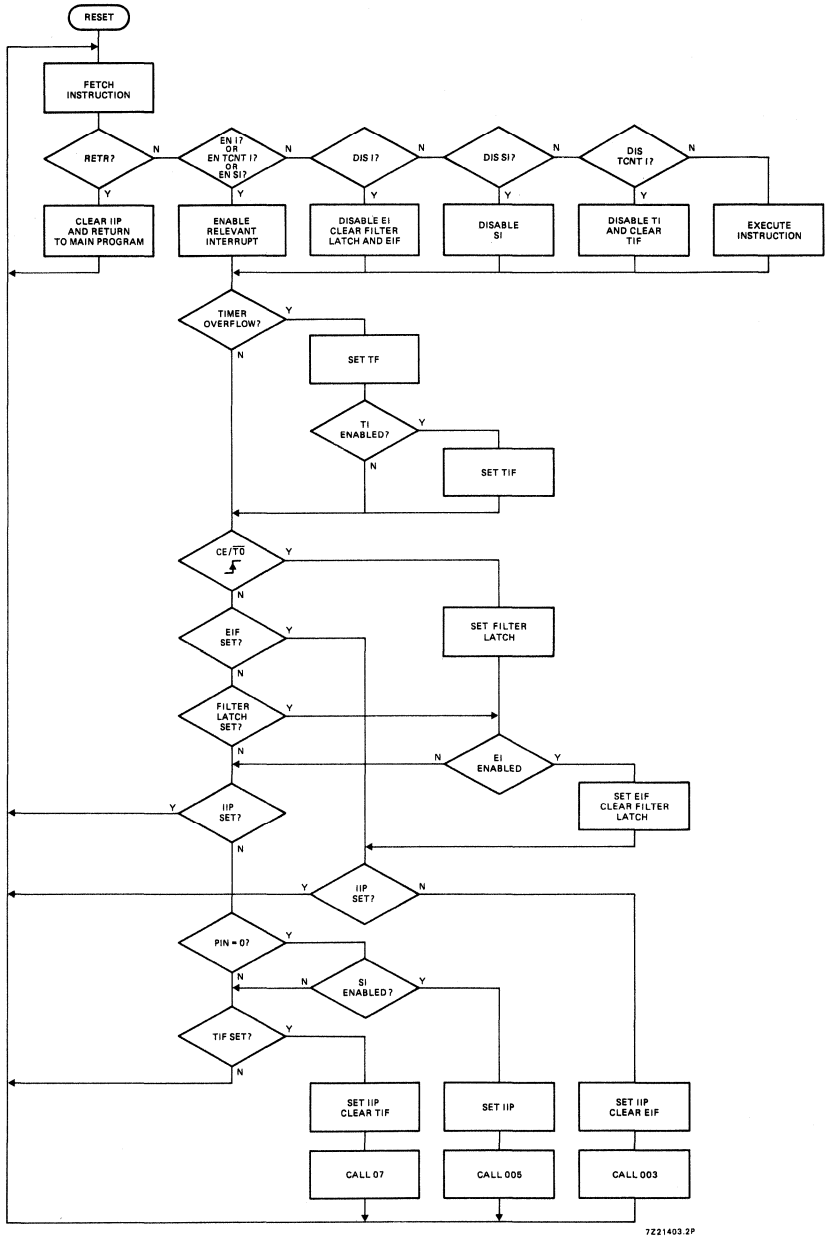
Interrupt Priority

If simultaneous interrupts occur, their priority is as follows:

External (highest)
SIO
Timer/Counter (lowest)

An interrupt routine can only be interrupted by a hardware RESET and cannot be interrupted by other interrupts (which will be latched). When the interrupt routine is terminated by the RETR instruction, at least one instruction of the main program will be executed before another interrupt routine is entered.

FUNCTIONAL DESCRIPTION (continued)



EI	External Interrupt	TF	Timer Flag
SI	Serial Interrupt	TIF	Timer Interrupt Flag
TI	Timer/counter Interrupt	PIN	Pending Interrupt Not (SIO)
EIF	External Interrupt Flag	IIP	Interrupt In Progress Flag

Fig. 15 (a) Flow chart illustrating the interrupt handling sequence.

DEVELOPMENT DATA

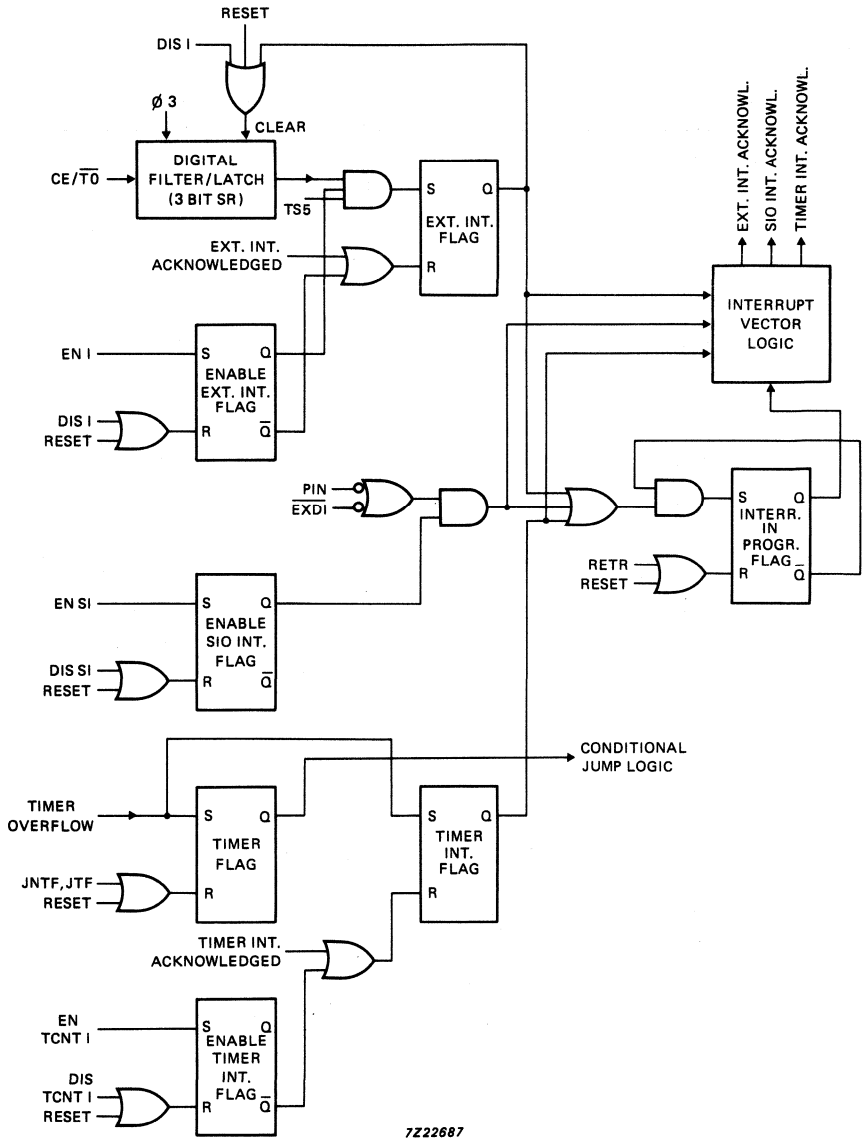


Fig. 15 (b) Simplified schematic of interrupt logic, to be used in conjunction with the functional description.

Notes to Figure 15

1. The positive edge of CE/$\overline{T0}$ is always latched in the digital filter/latch.
2. Correct interrupt timing is ensured when CE/$\overline{TO}$ is LOW for >4 CP followed by a HIGH for >7 CP.
3. When the interrupt in progress flag is set, further external and timer interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.
5. For all flip-flops, RESET overrules SET.

FUNCTIONAL DESCRIPTION (continued)

Oscillator (see Fig. 16)

The oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-supply voltage condition is present to prevent discharge of a weak back-up battery. Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a HIGH level at the CE/$\overline{T0}$ pin or a HIGH level at the RESET pin.

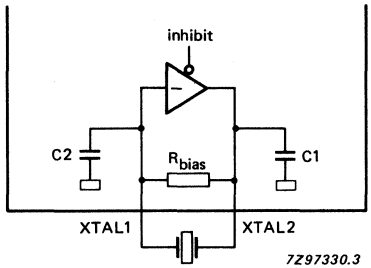


Fig. 16 Oscillator with integrated elements.

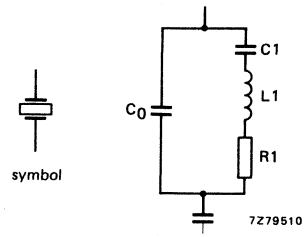


Fig. 17 Crystal unit equivalent circuit.

The values of crystal series resistance R1 and the crystal's total load capacitance C_L (C_0 + wiring + external capacitors) must not be above the curve (Fig. 18) for the corresponding frequency.
Note: if external capacitors are connected to XTAL1 and XTAL2, they must be of equal value.

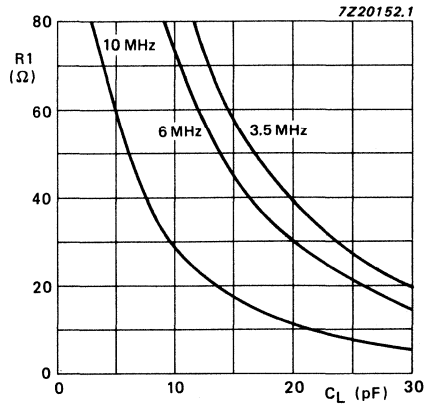


Fig. 18 Crystal circuit criteria.

XTAL2 is the output of the inverting amplifier. An external clock can be applied to XTAL1.
A machine cycle consists of 10 time slots; each time slot is 3 oscillator periods.

In telephony applications the 3.58 MHz crystal provides an 8.4 μs machine cycle.

DEVELOPMENT DATA

Timer/event counter (see Fig. 19)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 8 shows the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin T1 are counted. The counter is incremented during a machine cycle only if the falling edge occurs during the first 7 time slots; otherwise it is incremented during the next cycle. The maximum rate at which the counter may be incremented is once every machine cycle. When the counter overflows, the Timer flag is set. The flag can be tested and reset using the JTF (jump if Timer flag = logic 1) or JNTF (jump if Timer flag = logic 0) instruction. Overflow also generates an interrupt request to the microcontroller by setting the Timer Interrupt Flag when the timer/event counter interrupt is enabled.

Table 8 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

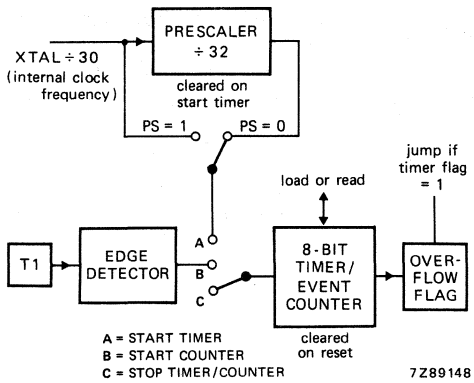


Fig. 19 Timer/event counter.

* With prescaler select (PS) = logic 0, the timer is incremented every 32 machine cycles; with PS = logic 1 the timer is incremented every machine cycle (prescaler not used), the prescaler is cleared by the STRT T instruction and is not readable.

** READ does not disturb the counting process.

FUNCTIONAL DESCRIPTION (continued)

Program status word (see Fig. 20)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS);
  0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS);
  0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that the previous operation resulted in an overflow of the accumulator

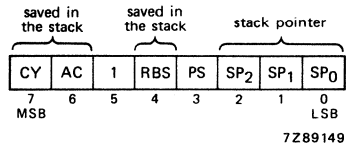


Fig. 20 Program status word.

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by the SEL RB instructions, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt service routine and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt service routine.

Program counter (see Fig. 21)

The 13-bit program counter is able to address 8 K bytes of ROM. The arrangement of the bits is shown in Fig. 21. During an interrupt subroutine PC 11 and PC 12 are forced to logic 0. All 13 bits are saved in the stack during CALL and interrupt routines.

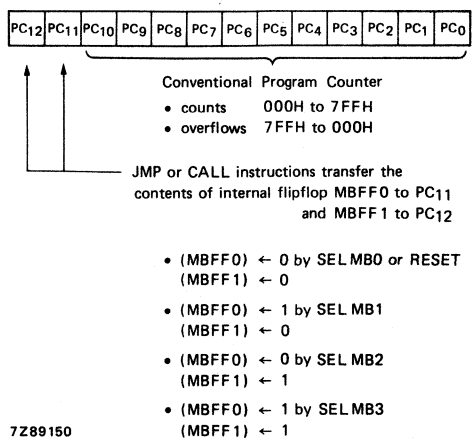


Fig. 21 Program counter.

Central processing unit

The PCD3346 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the microcontroller enables several conditions, internal and external to the microcontroller, to be tested by the user's program. Table 9 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 9 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JNT0
	0	JT0 *
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

* Because of the inverted interrupt input CE/$\overline{T0}$ the conditional jump JT0 is also inverted.

FUNCTIONAL DESCRIPTION (continued)

Test input T1

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for $>$ 4 CP, and then HIGH for $>$ 4 CP. A transition can be recognized every 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. When T1 is not used, it must be tied to V_{DD} or V_{SS}.

Power-on-reset

The internal power-on reset circuit monitors the supply voltage V_{DD}. As long as the supply voltage remains below the internal reference level V_{ref} (typically 1.5 V), the oscillator is inhibited and RESET has an undefined level. When V_{DD} rises above the internal reference level, the oscillator is released and RESET is pulled high to V_{DD} by TR1 for a period t_D (typically 50 μs).

N.B. Because of the narrow bandwidth of the crystal, the start-up time of the oscillator is typically 10 ms.

Three applications of power-on-reset are possible:

1. If V_{DD} can be switched with a fast rise time i.e. V_{DD} reaches its minimum operating value (corresponding to the selected oscillator frequency) before the RESET signal has finished (t_D), then no extra components are required (see Figs 22 and 23). Note that the first instruction is executed after the oscillator start-up time plus 1866 clock periods have elapsed.
2. If V_{DD} has a slow rise time then the RESET signal should be stretched by an external RC circuit (see Figs 24 and 25). In the event of a short drop in the supply voltage, the diode path rapidly discharges the capacitor to ensure a reliable power-on-reset. To ensure a correct reset, the RESET signal should reach at least 70% of the final value of V_{DD}. Given that the RESET voltage and V_{DD} rise exponentially, the above requirement is satisfied when the time constant τ of the RESET pulse is $>$ 8 times the time constant of V_{DD}. If V_{DD} rises linearly, then a RESET time constant $>$ 2 times the rise time of V_{DD} is required.

   When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 25). If the oscillator is started up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.
3. Fig. 26 shows an external reset during power-on. The external reset signal must remain HIGH until V_{DD} has reached its minimum operating value corresponding to the selected oscillator frequency. When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 27). If the oscillator is started-up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.

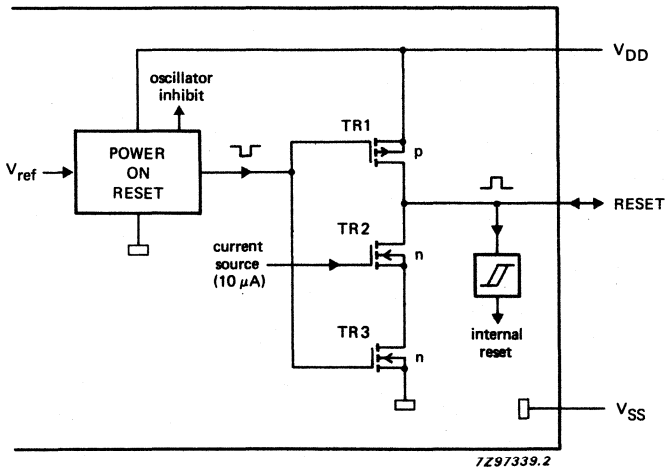


Fig. 22 Power-on-reset configuration.

DEVELOPMENT DATA

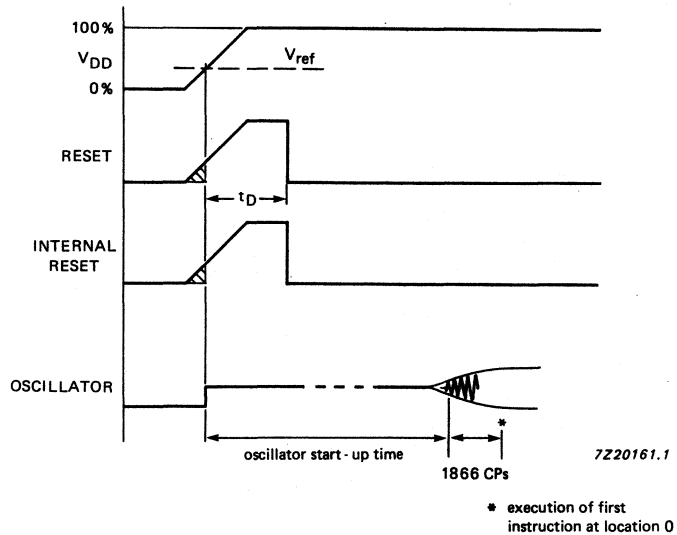


Fig. 23 Timing of power-on-reset with fast rise time.

FUNCTIONAL DESCRIPTION (continued)

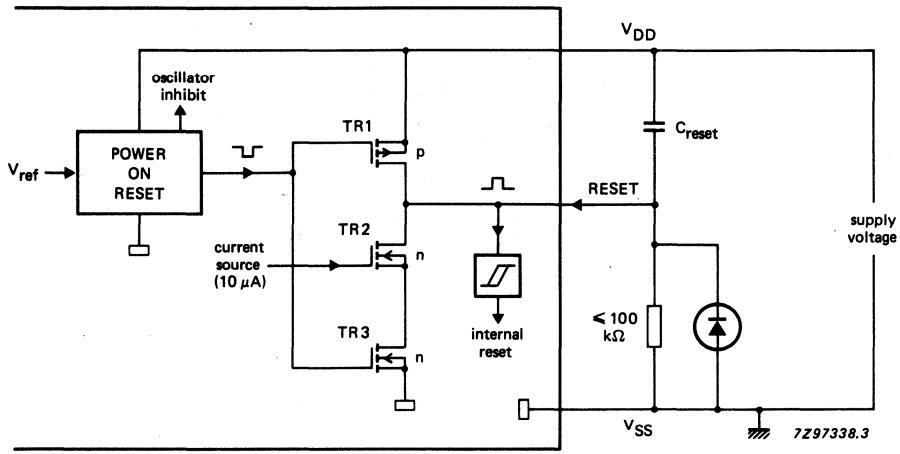


Fig. 24 Stretched power-on-reset with external components.

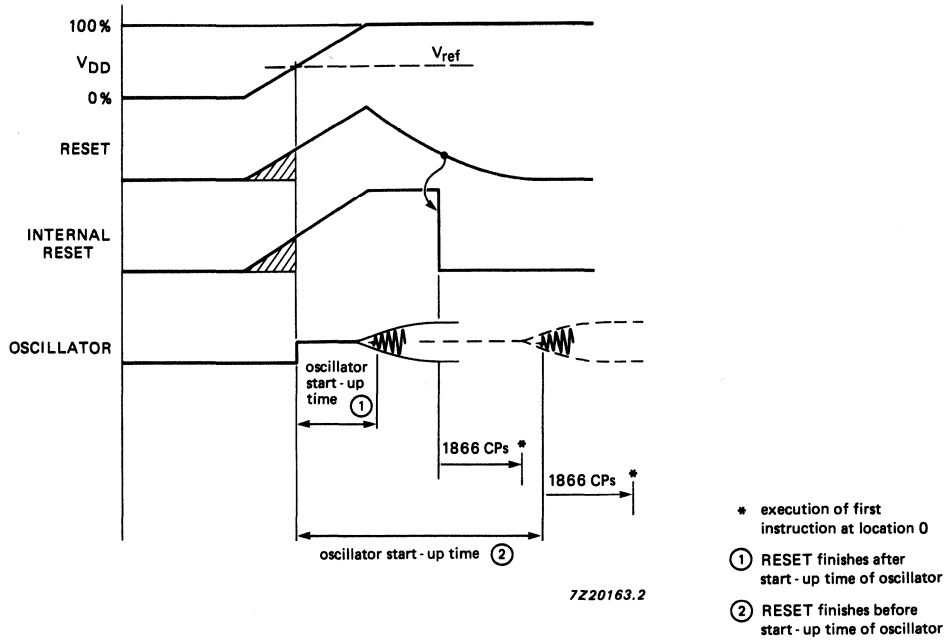


Fig. 25 Timing of power-on-reset with a slowly rising V_{DD} and a stretched RESET pulse.

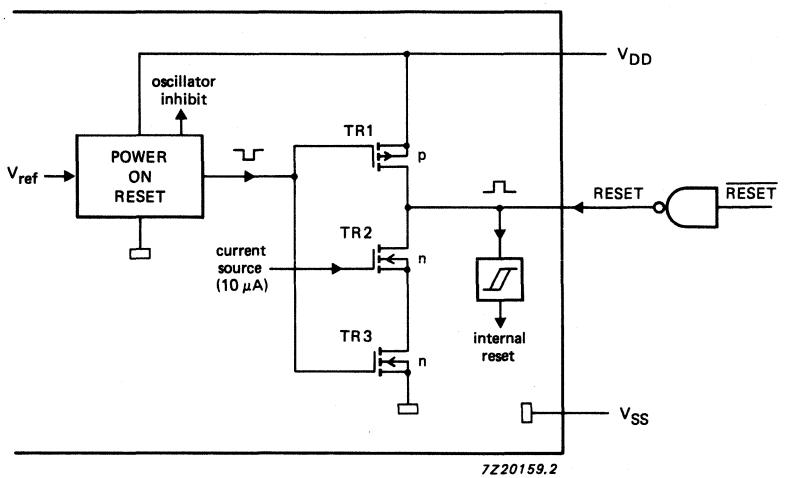


Fig. 26 External power-on-reset configuration.

DEVELOPMENT DATA

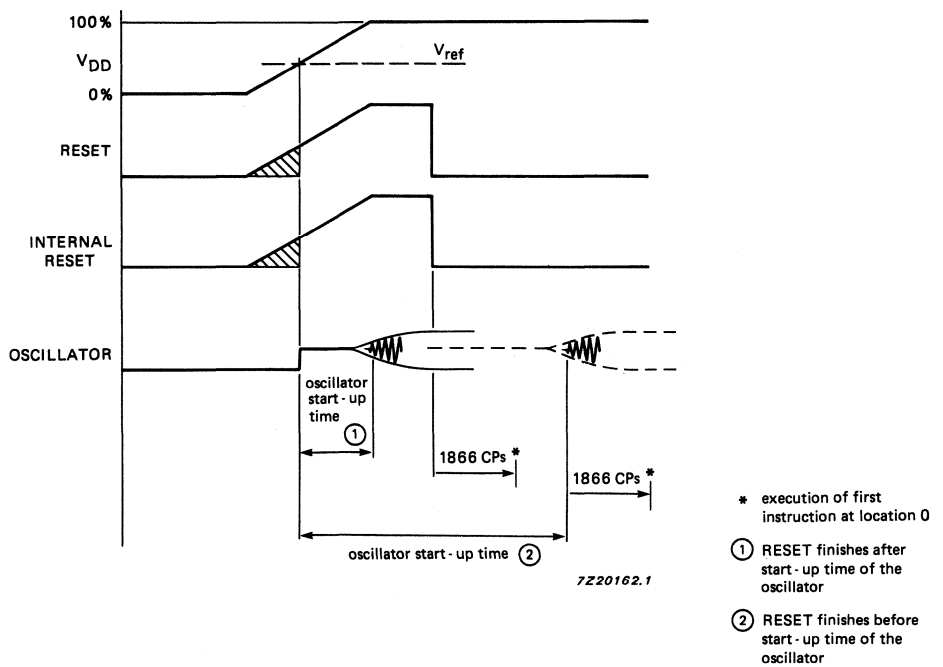


Fig. 27 Timing of external power-on-reset.

INSTRUCTION SET

The instruction set consists of over 80 one and two byte instructions. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 12 contains the instruction set. Table 11 shows the instruction map and Table 10 details the symbols that are used.

Table 10 Symbols and definitions used in Table 12

symbol	description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0-7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
Dx	mnemonic derivative register (x = 0 ... 255)
direct	8-bit derivative register address
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0-7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

Table 11 Instruction map

first hexadecimal character of opcode ↓ / second hexadecimal character of opcode →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, # data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	IN A,Pp 1	IN A,Pp 2		MOV A,Sn 0	MOV A,Sn 1		
1	INC @Rr 0	INC @Rr 1	JB0 addr	ADDC A, # data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0	INC Rr 1	INC Rr 2	INC Rr 3	INC Rr 4	INC Rr 5	INC Rr 6	INC Rr 7
2	XCH A,@Rr 0	XCH A,@Rr 1	STOP	MOV A, # data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A,Rr 0	XCH A,Rr 1	XCH A,Rr 2	XCH A,Rr 3	XCH A,Rr 4	XCH A,Rr 5	XCH A,Rr 6	XCH A,Rr 7
3	XCHD A,@Rr 0	XCHD A,@Rr 1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A 0	OUTL Pp,A 1	OUTL Pp,A 2		MOV Sn,A 0	MOV Sn,A 1	MOV Sn,A 2	
4	ORL A,@Rr 0	ORL A,@Rr 1	MOV A, T	ORL A, # data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0	ORL A,Rr 1	ORL A,Rr 2	ORL A,Rr 3	ORL A,Rr 4	ORL A,Rr 5	ORL A,Rr 6	ORL A,Rr 7
5	ANL A,@Rr 0	ANL A,@Rr 1	JB2 addr	ANL A, # data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0	ANL A,Rr 1	ANL A,Rr 2	ANL A,Rr 3	ANL A,Rr 4	ANL A,Rr 5	ANL A,Rr 6	ANL A,Rr 7
6	ADD A,@Rr 0	ADD A,@Rr 1	MOV T, A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0	ADD A,Rr 1	ADD A,Rr 2	ADD A,Rr 3	ADD A,Rr 4	ADD A,Rr 5	ADD A,Rr 6	ADD A,Rr 7
7	ADDC A,@Rr 0	ADDC A,@Rr 1	JB3 addr		CALL page 3			RR A	ADDC A,Rr 0	ADDC A,Rr 1	ADDC A,Rr 2	ADDC A,Rr 3	ADDC A,Rr 4	ADDC A,Rr 5	ADDC A,Rr 6	ADDC A,Rr 7
8				RET	JMP page 4	EN SI			ORL Pp, # data 0	ORL Pp, # data 1	ORL Pp, # data 2		MOV A, Dx	MOV Dx, A	ANL Dx, A	ORL Dx, A
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,# data 0	ANL Pp,# data 1	ANL Pp,# data 2		MOV Sn,# data 0	MOV Sn,# data 1	MOV Sn,# data 2	
A	MOV @Rr,A 0	MOV @Rr,A 1		MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0	MOV Rr,A 1	MOV Rr,A 2	MOV Rr,A 3	MOV Rr,A 4	MOV Rr,A 5	MOV Rr,A 6	MOV Rr,A 7
B	MOV @Rr, #data 0	MOV @Rr, #data 1	JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr, # data 0	MOV Rr, # data 1	MOV Rr, # data 2	MOV Rr, # data 3	MOV Rr, # data 4	MOV Rr, # data 5	MOV Rr, # data 6	MOV Rr, # data 7
C	DEC @Rr 0	DEC @Rr 1			JMP page 6	SEL RB0	JZ addr	MOV A, PSW	DEC Rr 0	DEC Rr 1	DEC Rr 2	DEC Rr 3	DEC Rr 4	DEC Rr 5	DEC Rr 6	DEC Rr 7
D	XRL A,@Rr 0	XRL A,@Rr 1	JB6 addr	XRL A,# data	CALL page 6	SEL RB1		MOV PSW, A	XRL A,Rr 0	XRL A,Rr 1	XRL A,Rr 2	XRL A,Rr 3	XRL A,Rr 4	XRL A,Rr 5	XRL A,Rr 6	XRL A,Rr 7
E	DJNX @Rr, addr 0	DJNX @Rr, addr 1			JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr 0	DJNZ Rr, addr 1	DJNZ Rr, addr 2	DJNZ Rr, addr 3	DJNZ Rr, addr 4	DJNZ Rr, addr 5	DJNZ Rr, addr 6	DJNZ Rr, addr 7
F	MOV A,@Rr 0	MOV A,@Rr 1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0	MOV A,Rr 1	MOV A,Rr 2	MOV A,Rr 3	MOV A,Rr 4	MOV A,Rr 5	MOV A,Rr 6	MOV A,Rr 7

INSTRUCTION SET (continued)

Table 12 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) – 1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1}) \leftarrow A_n$ $(A_0) \leftarrow (C), (C) \leftarrow (A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (C), (C) \leftarrow (A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7}) \leftrightarrow (A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3}) \leftrightarrow ((R0_{0-3}))$ $(A_{0-3}) \leftrightarrow ((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3) \leftarrow (A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7}) \leftarrow (A), (A) \leftarrow ((PC))$		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

INSTRUCTION SET (continued)

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) − 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) − 1 ((R1))←((R1)) − 1	
BRANCH	JMP addr	● 4 addr	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* addr	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) − 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0	2/2	decrement RAM data, addressed by Rr, by 1 and jump if not zero to addr	((R0))←((R0)) − 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1			((R1))←((R1)) − 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 addr	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 addr	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 addr	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 addr	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 addr	2/2	jump to addr if A is NOT zero	if A ≠ 0 : (PC_{0-7})←addr	
	JT0 addr	36 addr	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JNT0 addr	26 addr	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JT1 addr	56 addr	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 addr	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 addr	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 addr	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	10
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	10
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	10
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 addr	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4, 6, 7}$) (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) – 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) – 1 ($PSW_{4, 6, 7}$) + (PC)←((SP))	6

INSTRUCTION SET (continued)

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)		7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)		
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data		
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data		
DERIVATIVE INPUT/OUTPUT	MOV A, Dx	8C direct	2/2	move derivative register contents to accumulator	(A)←(Dx)	x = 1 to 6	
	MOV Dx, A	8D direct	2/2	move accumulator contents to derivative register	(Dx)←(A)	x = 1 to 6	
	ANL Dx, A	8E direct	2/2	AND derivative register with accumulator	(Dx)←(Dx) AND (A)	x = 1 to 6	
	ORL Dx, A	8F direct	2/2	OR derivative register with accumulator	(Dx)←(Dx) OR (A)	x = 1 to 6	

SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	9
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	
	MOV S_n, #data	9C data 9D data 9E data	2/2	move immediate data to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 12

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of a JTF or JNTF instruction resets the Timer Flag (TF).

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 5, 6, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 0000, P2.3, P2.2, P2.1, P2.0.
8. Instructions for 84C00T only.
9. (S1) has a different meaning for read and write operation, see serial I/O interface.
10. SEL MB1, SEL MB2 and SEL MB3 may not be used within interrupt routines.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltages	V_{DD}	−0.8	+ 8	V
All input voltages	V_I	0.5	V_{DD} + 0.5	V
DC current into any input or output	$\pm I_I$ $\pm I_O$	–	10	mA
Total power dissipation (see note)	P_{tot}	–	500	mW
Power dissipation per output	P_O	–	50	mW
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Operating junction temperature	T_j	–	125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

THERMAL RESISTANCE

From junction to ambient

SOT117	$R_{th\ j\text{-}a}$	=	120 K/W
SOT136A	$R_{th\ j\text{-}a}$	=	150 K/W

DC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage operating (see Fig. 28)	V_{DD}	2.5	–	6	V
Supply current operating (see Fig. 29 and note 2)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	2.0	3.5	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	1.2	2.4	mA
at V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	I_{DD}	–	0.4	0.8	mA
IDLE mode (see Fig. 30 and note 2)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	1.0	2.0	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	0.7	1.2	mA
at V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	I_{DD}	–	0.25	0.4	mA
STOP mode (see Fig. 36 and notes 1 and 2)					
at V_{DD} = 2.5 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
EEPROM Erase/Write cycle limitation*		10^4			
EEPROM data retention time	T_{RET}	10	–	–	years
RESET I/O					
Switching level	V_{RESET}	–	1.5	–	V
Sink current at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	0.3 V_{DD}	V
Input voltage HIGH	V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Input leakage current at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW at $V_I = V_{SS}$ or V_{DD}; $\|I_O\| < 1$ μA	V_{OL}	–	–	0.05	V
Output sink current LOW at V_{DD} = 3 V; V_O = 0.4 V					
except P2.3/SDA, SCLK (see Fig. 32)	I_{OL}	0.7	1.5	–	mA
P2.3/SDA, SCLK (see Fig. 33)	I_{OL}	1.5	–	–	mA
Pull-up output source current HIGH (see Fig. 34)					
at V_{DD} = 3 V; V_O = 0.9 V_{DD}	$-I_{OH}$	10	–	–	μA
at V_{DD} = 3 V; V_O = V_{SS}	$-I_{OH}$	–	–	300	μA
Push-pull output source current HIGH at V_{DD} = 3 V; V_O = V_{DD} − 0.4 V	$-I_{OH}$	0.7	1.5	–	mA

* Verified on sampling bases.

Notes to the DC characteristics

1. Crystal connected between XTAL1 and XTAL2; T1 and CE both tied to V_{SS}.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; all outputs disconnected, all open-drain outputs connected to V_{SS}.

AC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C. All voltages with respect to V_{SS} unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Rise time all outputs (note 1)	t_R	–	30	–	ns
Fall time all outputs (note 1)	t_F	–	30	–	ns
Cycle time (= 30 CP; note 2)	t_{CY}	3	–	67	μs

Notes to the AC characteristics

1. At V_{DD} = 5 V; T_{amb} = + 25 °C; C_L = 50 pF.
2. 1 Time slot (TS) = 3 CP, 1 clock pulse (CP) = $1/f_{XTAL}$.

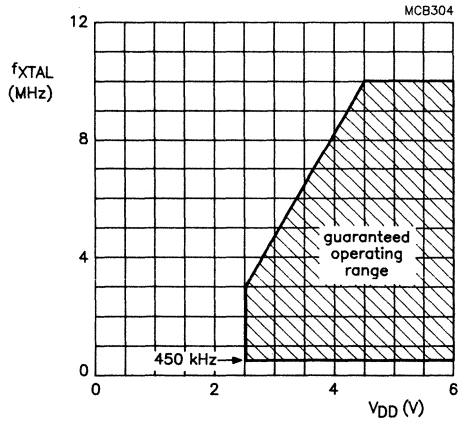
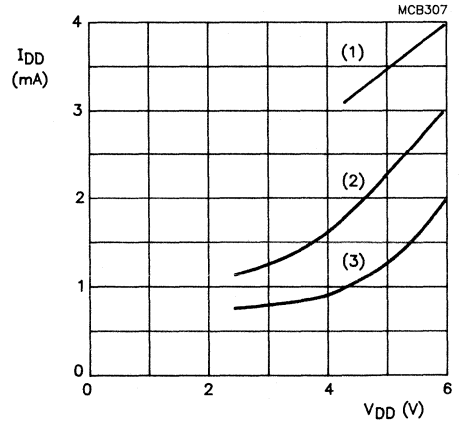


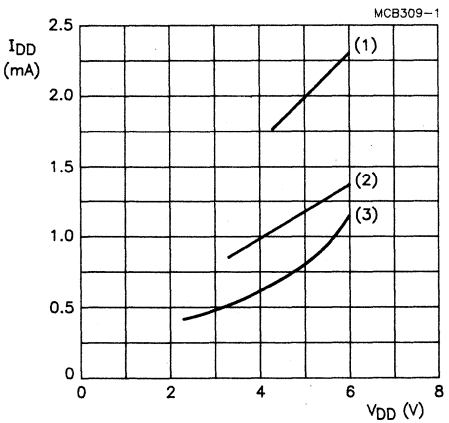
Fig. 28 Maximum clock frequency (F_{XTAL}) as a function of the supply voltage (V_{DD}).



(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3.58 MHz

Fig. 29 Maximum supply current (I_{DD}) in operation mode as a function of the supply voltage (V_{DD}).

DEVELOPMENT DATA



(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3.58 MHz

Fig. 30 Maximum supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}).

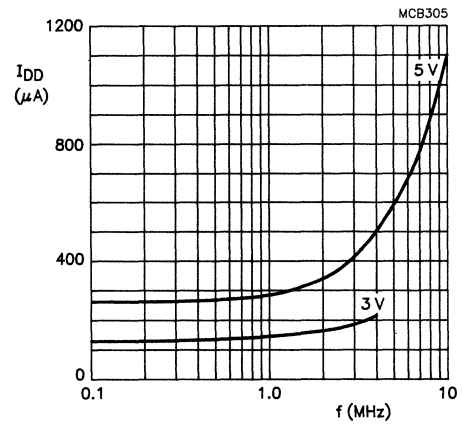


Fig. 31 Typical supply current during IDLE mode as a function of frequency at V_{DD} = 3 V and V_{DD} = 5 V.

AC CHARACTERISTICS (continued)

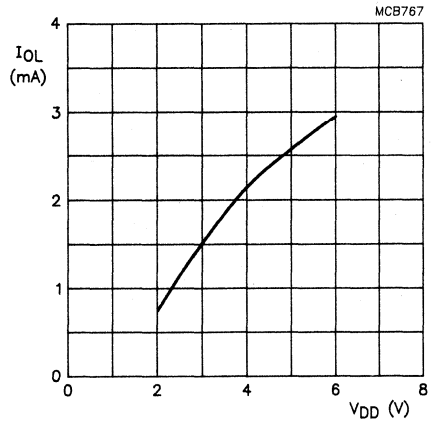


Fig. 32 Typical output sink current (I_{OL}), outputs P0.0 to P0.7 and P2.0 to P2.2, as a function of the supply voltage (V_{DD}); V_O = 0.4 V.

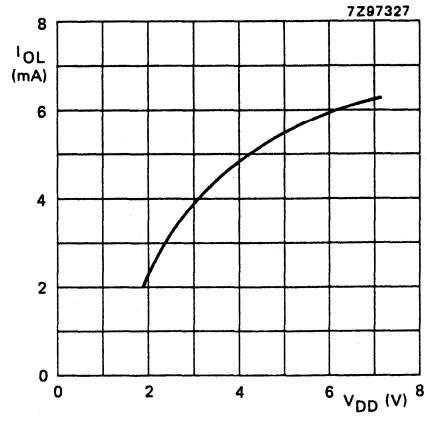
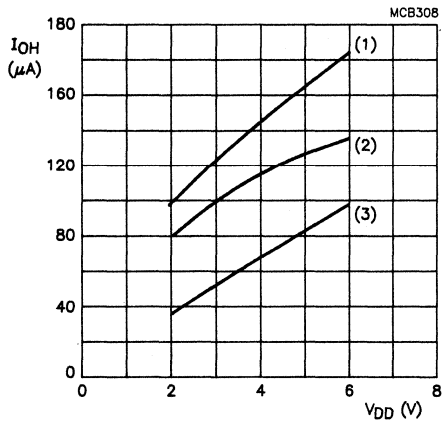


Fig. 33 Typical output sink current (I_{OL}), outputs P2.3/SDA and SCLK, as a function of the supply voltage (V_{DD}); V_O = 0.4 V.



(1) $V_O = V_{SS}$
(2) $V_O = 0.7\ V_{DD}$
(3) $V_O = 0.9\ V_{DD}$

Fig. 34 Typical output source current ($-I_{OH}$) as a function of the supply voltage (V_{DD}).

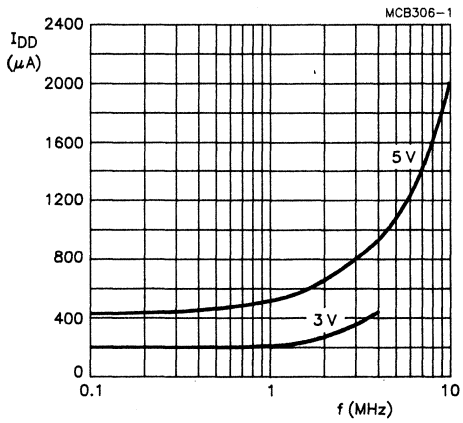
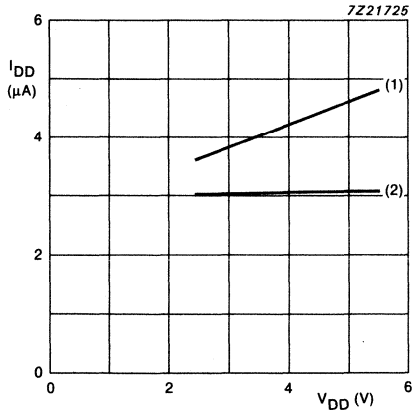


Fig. 35 Typical supply current during operating mode as a function of frequency at V_{DD} = 3 V and V_{DD} = 5 V.



(1) T_{amb} = 85 °C
(2) T_{amb} = 25 °C

Fig. 36 Typical supply current (I_{DD}) in STOP modes as a function of the supply voltage (V_{DD}).

Table 13 Input timing shown in Fig. 37

symbol	timing
t_{BUF}	$\geqslant 14t_{XTAL}$
$t_{HD;STA}$	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
$t_{SU:STO}$	$\geqslant 14t_{XTAL}$
$t_{HD;DAT}$	> 0
$t_{SU;DAT}$	$\geqslant 250$ ns
t_{RD}	$\leqslant 1\ \mu s$
t_{RC}	$\leqslant 1\ \mu s$
t_{FD}	$\leqslant 1\ \mu s$
t_{FC}	$\leqslant 0.3\ \mu s$

Notes to Table 13

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 167 ns for f_{XTAL} = 6 MHz
These figures apply to all modes.

DEVELOPMENT DATA

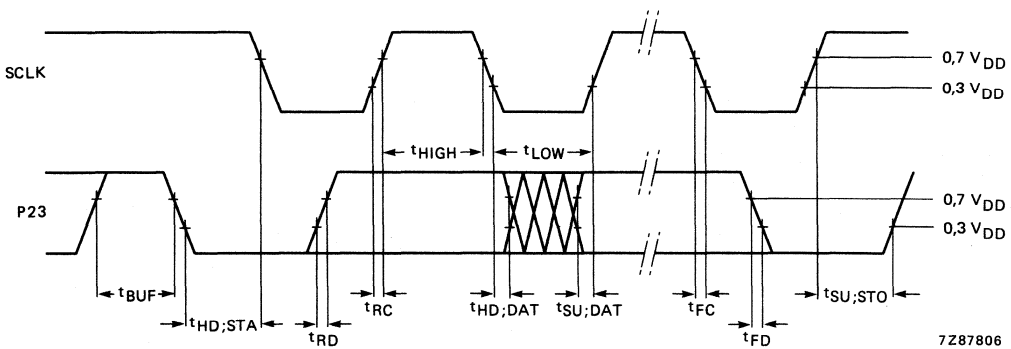


Fig. 37 Timing requirements for the P2.3 and SCLK *input* signals.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

AC CHARACTERISTICS (continued)

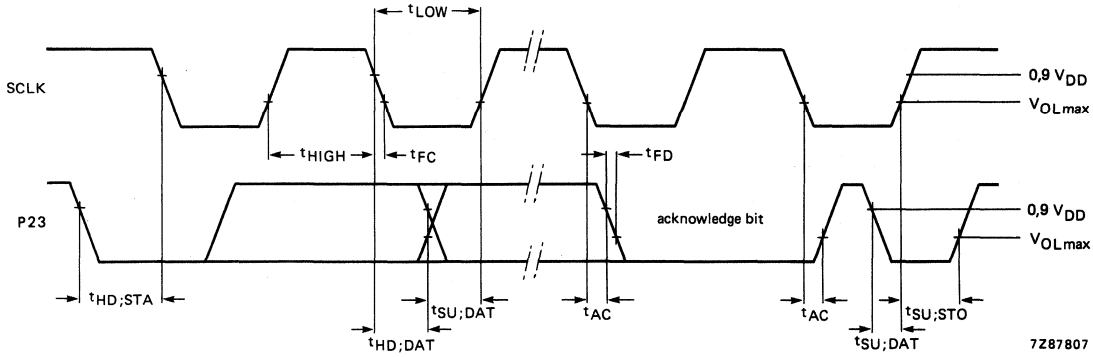


Fig. 38 Timing requirements for the P2.3 and SCLK *output* signals.

Table 14 Output timing shown in Fig. 38

symbol	timing	
	normal mode (ASC in S2 = 0)	low-speed mode (ASC in S2 = 1)
$t_{HD;STA}$	½ (DF + 9) t_{XTAL}	¾ (DF + 9) t_{XTAL}
t_{HIGH}	½ (DF) t_{XTAL}	¾ (DF) t_{XTAL}
t_{LOW}	½ (DF) t_{XTAL}	¼ (DF) t_{XTAL}
$t_{SU;STO}$	½ (DF − 3) t_{XTAL}	¼ (DF − 3) t_{XTAL}
$t_{HD;DAT}$ (slave transmitter) any DF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{HD;DAT}$ (master transmitter) for DF $\leqslant$ 51)	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	– –
for DF $\leqslant$ 99	– –	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter) for DF > 51	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$	– –
for DF > 99	– –	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
t_{FD}, t_{FC}	$\leqslant$ 100 ns at C_b = 400 pF	$\leqslant$ 100 ns at C_b = 400 pF

Notes to Table 14

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL}) = 167 ns for f_{XTAL} = 6 MHz.
DF = divisor (see Table 7 Serial I/O section).
C_b = the maximum bus capacitance for each line.

CMOS MICROCONTROLLER WITH ON-CHIP DTMF GENERATOR

GENERAL DESCRIPTION

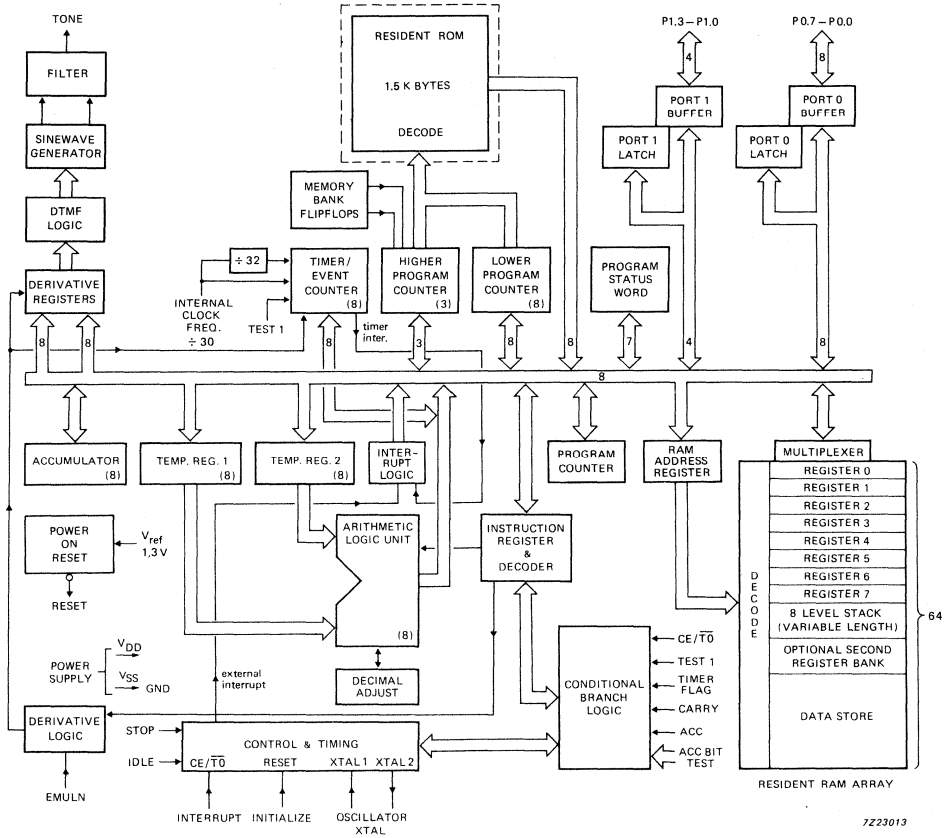
The PCD3347 is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD33XX family. It has an on-chip dual tone multi-frequency (DTMF) generator and other features for application in telephone sets. For further detailed information, see PCD33XX family specification.

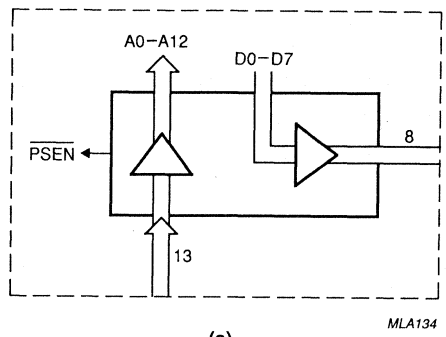
Features

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead DIL or SO package
- 1536 ROM bytes
- 64 RAM bytes
- On-chip DTMF tone generator
- On-chip voltage reference for supply and temperature-independent tone output
- On-chip filtering for low output distortion (CEPT CS203 compatible)
- 12 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles
- Clock frequency 3,58 MHz
- Single supply voltage from 2,5 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3347P: 20-lead DIL; plastic (SOT146).
PCD3347T: 20-lead mini-pack; plastic (SO20; SOT163A).





(a)

Fig. 1 PCD3347 block diagram: the function in the dotted outline is replaced as shown in (a) for the PCD3344B 'piggy-back' version.

PINNING (for normal operation)

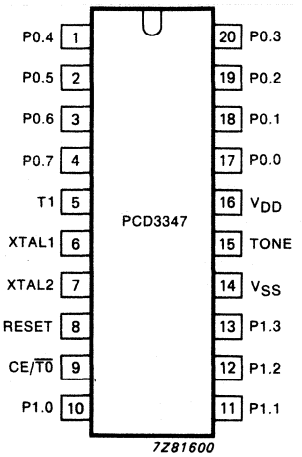


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

PIN DESIGNATION

17-20, 1-4	P0.0-P0.7	Port 0: 8-bit quasi-bidirectional I/O port.
5	T1	Test 1: test input, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter using the STRT CNT instruction.
6	XTAL1	Crystal input: connection to the timing component (crystal) which determines the frequency of the internal oscillator; is also the input for an external clock source.
7	XTAL2	Connection to other side of timing component.
8	RESET	Reset input (active HIGH): used to initialize the processor or output of the power-on-reset circuit.
9	CE/$\overline{T0}$	Interrupt/Test 0: external interrupt input (sensitive to positive-going edge)/test input pin. When used as a test input is directly tested by conditional branch instructions JT0 and JNT0.
10-13	P1.0-P1.3	Port 1: 4-bit quasi-bidirectional I/O port.
14	V_{SS}	Ground: circuit earth potentional.
15	TONE	Tone output: single or dual tone frequency output with on-chip filtering for low output distortion (CEPT CS203 compatible). This generator is controlled via the internal processor bus.
16	V_{DD}	Power supply: 2,5 to 6 V.

FUNCTIONAL DESCRIPTION

Program memory PCD3347

The program memory comprises 1536 bytes (8-bit words) in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 3 shows the program memory map.

Three program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine,
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

The program memory is divided into location 'pages', each of 256 bytes. This division applies only for conditional branches. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory PCD3347

Data memory consists of 64 bytes (8-bit words) of random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 4 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently-addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 5) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with next generated return address.

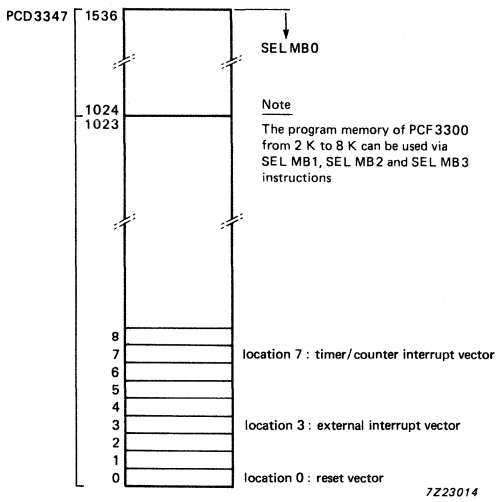


Fig. 3 Program memory map.

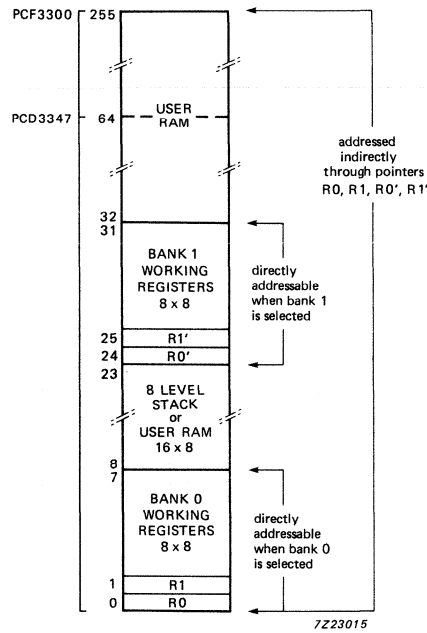


Fig. 4 Data memory map.

DEVELOPMENT DATA

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations. Possible locations from 32 to 64 may be used for storage of program variables or data.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

FUNCTIONAL DESCRIPTION (continued)

Program counter stack (continued)

stack pointer									
1 1 1	----------								R23/22
1 1 0	----------								R21/20
1 0 1	----------								R19/18
1 0 0	----------								R17/16
0 1 1	----------								R15/14
0 1 0	----------								R13/12
0 0 1	----------								R11/10
0 0 0	PSW7	PSW6	PC12	PSW4	PC11	PC10	PC9	PC8	R9
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	R8

Fig. 5 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (H'01') the oscillator and timer/counter are kept running. The microcontroller exits from the IDLE mode by one of two interrupts if they are enabled or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 6).

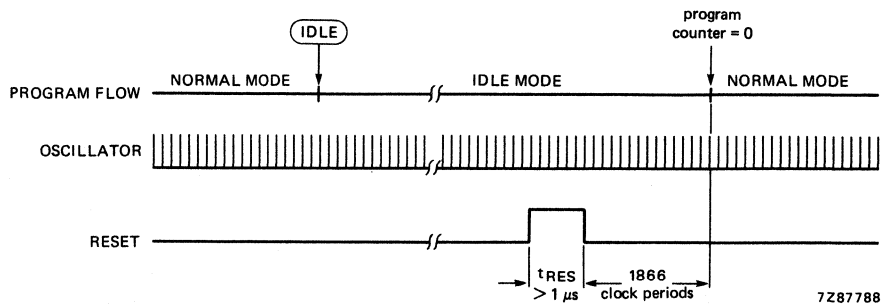


Fig. 6 Exit from IDLE mode via a RESET.

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A LOW-to-HIGH transition on the external interrupt pin (CE/$\overline{T0}$) reactivates the microcontroller. A HIGH level applied to CE/$\overline{T0}$ will reactivate the microcontroller only in the STOP mode. Thus, if CE/$\overline{T0}$ was HIGH before the microcontroller entered the IDLE mode, it must go LOW before the microcontroller can be reactivated (see Fig. 7).

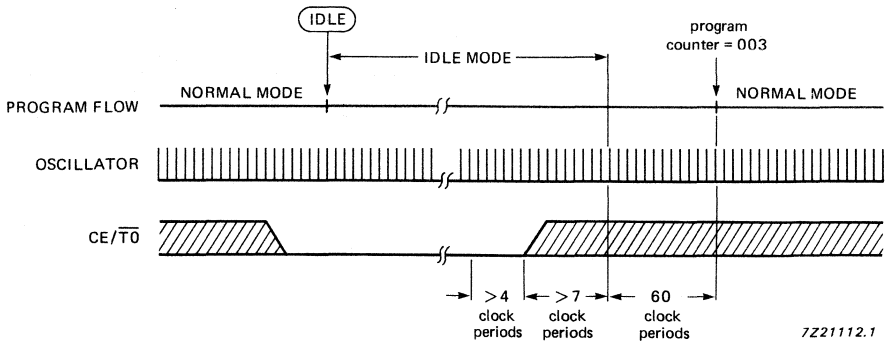


Fig. 7 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when CE/$\overline{T0}$ is LOW for 4 CP (clock periods) followed by a HIGH for 7 CP. After the initial forced CALL H'003' operation (60 CP) the program continues with the external interrupt service routine.

STOP mode

The microcontroller enters the STOP mode by the STOP instruction (H'22'). The oscillator is switched off. The internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 8).

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin HIGH, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a HIGH level applied at the CE/$\overline{T0}$ pin, and not by a LOW-to-HIGH transition as in a normal interrupt mechanism.

When the CE/$\overline{T0}$ level is active during the STOP instruction then no STOP is executed.

A HIGH level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode.

FUNCTIONAL DESCRIPTION (continued)

STOP mode (continued)

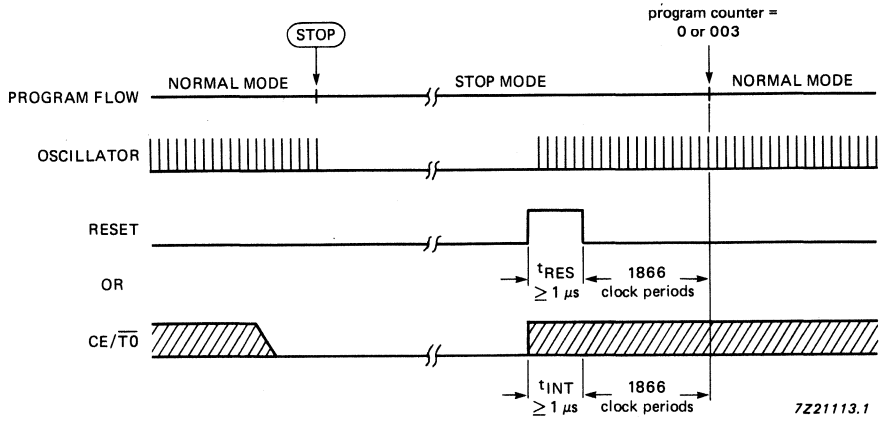


Fig. 8 Entering and exiting the STOP mode.

Tone output (DTMF mode)

Control of the sinewave generator

The on-chip sinewave oscillator is controlled by the 'derivative' registers Dx (x = H'O' to 'FF'). The instruction that controls the derivative registers is shown in Table 1.

Table 1 Derivative register control

mnemonic	opcode	description	function
MOV Dx,A	8D Dx	move accumulator contents to derivative register	(Dx) ← (A)

The instruction is 2 cycles/2 bytes. The second byte selects the derivative register to be addressed (H'O' to 'FF'). Register H'01' is for control of HIGH group frequencies, and register H'02' for control of LOW group frequencies. Thus data transport from accumulator to derivative register D01 is done by the 2-byte opcode 8D,01.

Generation of frequencies

The single and dual tones at the tone output are filtered by an on-chip switched-capacitor filter followed by an on-chip active RC low-pass filter. These ensure that the total harmonic distortion of the DTMF tones fulfil the CEPT CS 203 recommendations. An on-chip reference voltage provides output tone levels that are independent of the supply voltage.

The output frequency can be calculated as follows:

$$f_{out} = \frac{f_{XTAL}}{23\,(x + 2)} \quad \text{Hz}$$

x = 60 to 255 and is the decimal value of the appropriate ROM-code (see Table 2)

Table 2 ROM-codes for DTMF applications

telephone keyboard symbol	contents of low register (hex)	contents of high register (hex)
0	A3	72
1	DD	7F
2	DD	72
3	DD	67
4	C8	7F
5	C8	72
6	C8	67
7	B5	7F
8	B5	72
9	B5	67
A	DD	5D
B	C8	5D
C	B5	5D
D	A3	5D
*	A3	7F
#	A3	67

DTMF generation is stopped by loading H'00' into both derivative registers.

I/O facilities

The PCD3344 family has 14 I/O lines arranged as:

- Port 0 parallel port of 8 lines (P0.0 to P0.7)
- Port 1 parallel port of 4 lines (P1.0 to P1.3)
- CE/$\overline{T0}$ external interrupt and test input. When used as a test input it can be directly tested by conditional branch instructions JT0 and JNT0.
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional. Output data written to a port is latched and remains unchanged until rewritten. Input data is not latched and so must be present until read by an input instruction.

Input lines are fully CMOS compatible, output lines can drive one LS-TTL or CMOS load.

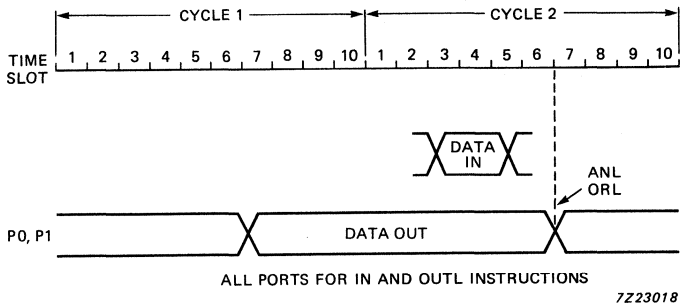


Fig. 9 Timing diagram of all ports on IN and OUTL instructions; for ANL and ORL instructions, the ports change on the time slot 7 of cycle 2.

Fig. 10 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source. Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current source provides sufficient current for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period) to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

In telephone applications this switched pull-up source may not be sufficient. Therefore the PCD3347 offers the possibility to select individually the 12 parallel port pins by the following mask options:

Option 1 –STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2 (2,5 mA). TR2 is active only during 1 clock cycle (0,28 μs at 3,58 MHz).

Option 2 –OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 11).

Option 3 –PUSH-PULL OUTPUT; drive capability of the output will be 2,5 mA (typ.) at V_{DD} = 3 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must be used only as outputs (Fig. 12).

Also, individual mask selection of the RESET state of these port pins can be achieved by appending the following options S and R to options 1, 2 or 3.

Option S-SET; after RESET this pin will be initialized to HIGH

Option R-RESET; after RESET this pin will be initialized to LOW.

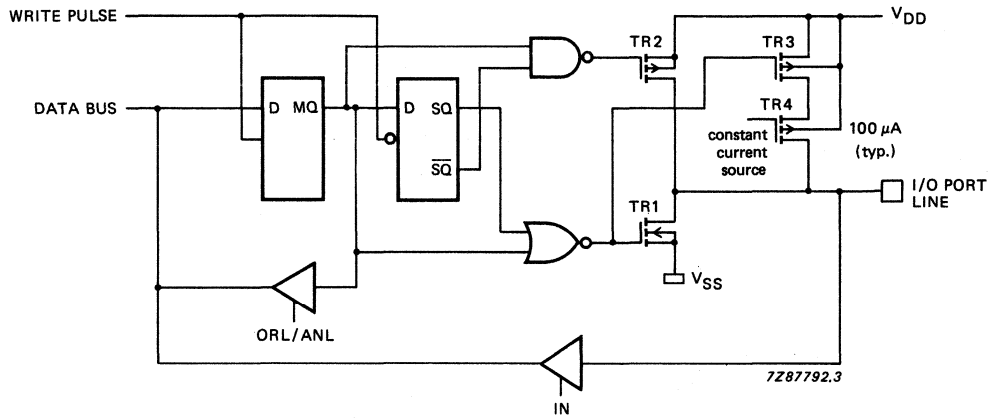


Fig. 10 Standard output with switched pull-up current source.

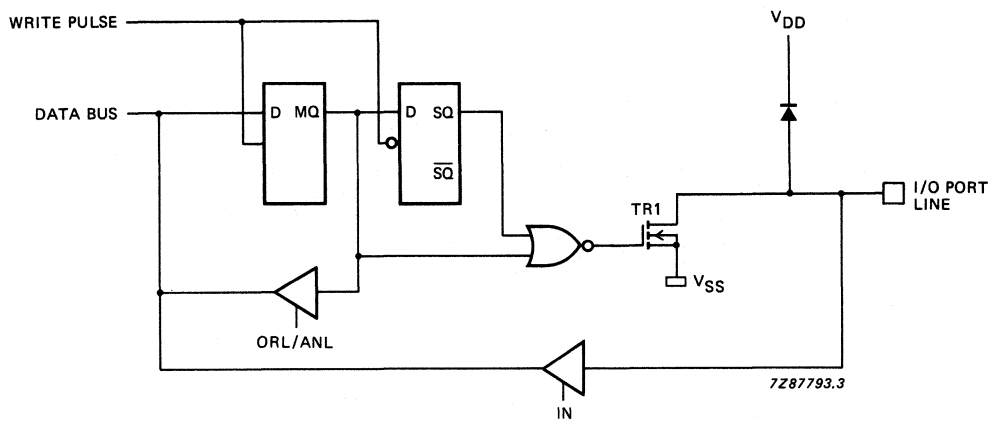


Fig. 11 Open drain output.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Parallel ports (continued)

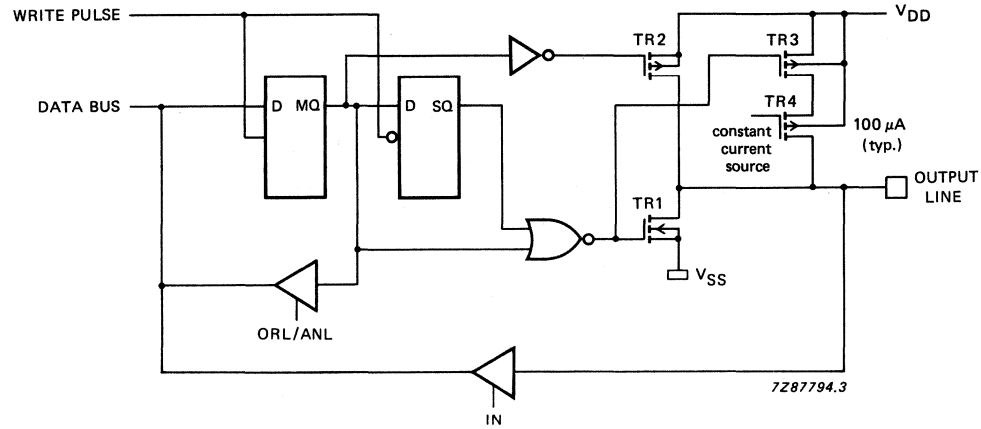


Fig. 12 Push-pull output.

Interrupts (see Fig. 13(a) and Fig. 13(b))

When an interrupt routine is entered, the contents of the program counter and bits 4, 6 and 7 of the PSW are saved in the program counter stack. The contents of the accumulator can only be saved by user software. Interrupt acknowledgement can be carried out by software via I/O ports. All interrupt routines must reside in memory bank 0; the SEL MB1, SEL MB2 and SEL MB3 instructions may not be used in an interrupt routine. An interrupt routine can only be terminated by the RETR (return and restore) instruction. During an interrupt routine, subroutine calls must be terminated by the RET instruction. Using the RETR instruction to terminate a subroutine called in an interrupt routine would terminate the interrupt routine prematurely and result in a wrong return address.

1. **External interrupt**

When the external interrupt is enabled, a HIGH-to-LOW transition on the CE/$\overline{TO}$ input initiates an external interrupt routine which forces a call to program memory location 3. The program counter points to the external interrupt vector address (003 H) between 2,6 and 3,6 machine cycles after the transition occurs. Interrupt latency depends on the instruction that is being executed when the transition occurs. External interrupts are latched in the External Interrupt Flag (EIF) even when they are not enabled. Execution of a DIS I instruction clears previously latched interrupts, the digital filter latch and the external interrupt flag.

2. **Timer/counter interrupt**

When the timer interrupt is enabled, a timer/counter overflow sets the Timer Interrupt Flag (TIF) and forces a CALL to location 7. The timer interrupts are only latched when they are enabled. The timer flag is set every time the timer/counter overflows and is not automatically reset when the timer/counter interrupt routine is called. It can only be cleared by the JTF and JNTF instructions or by a hardware RESET.

3. Simultaneous interrupts

If simultaneous interrupts occur their priority is as follows:

external (highest);
timer/counter (lowest).

An interrupt routine can only be interrupted by a hardware RESET and cannot be interrupted by other interrupts (which will be latched if enabled). When the interrupt routine is terminated by the RETR instruction, at least one instruction of the main program will be executed before another interrupt routine is entered.

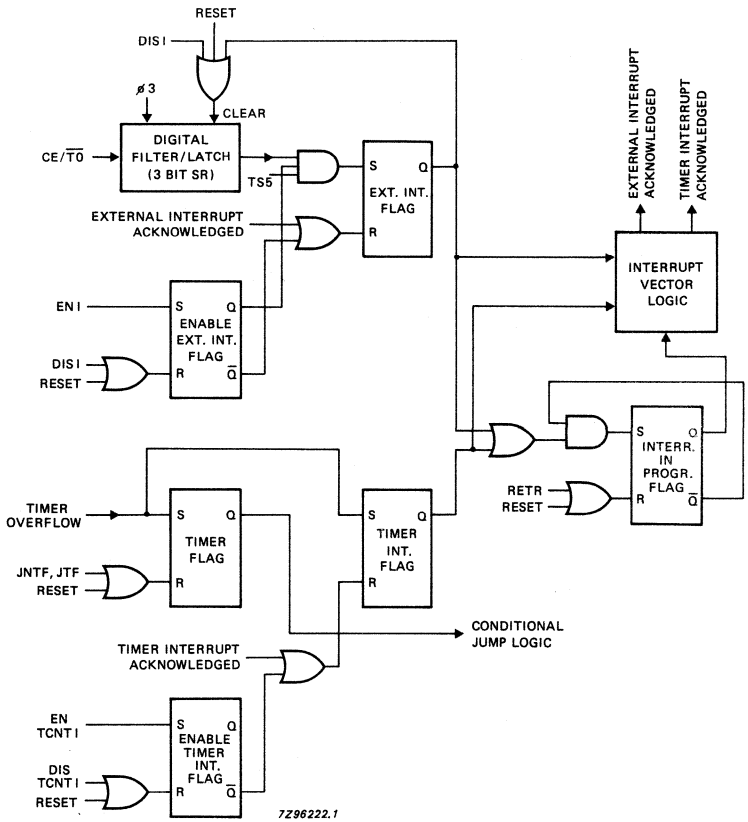


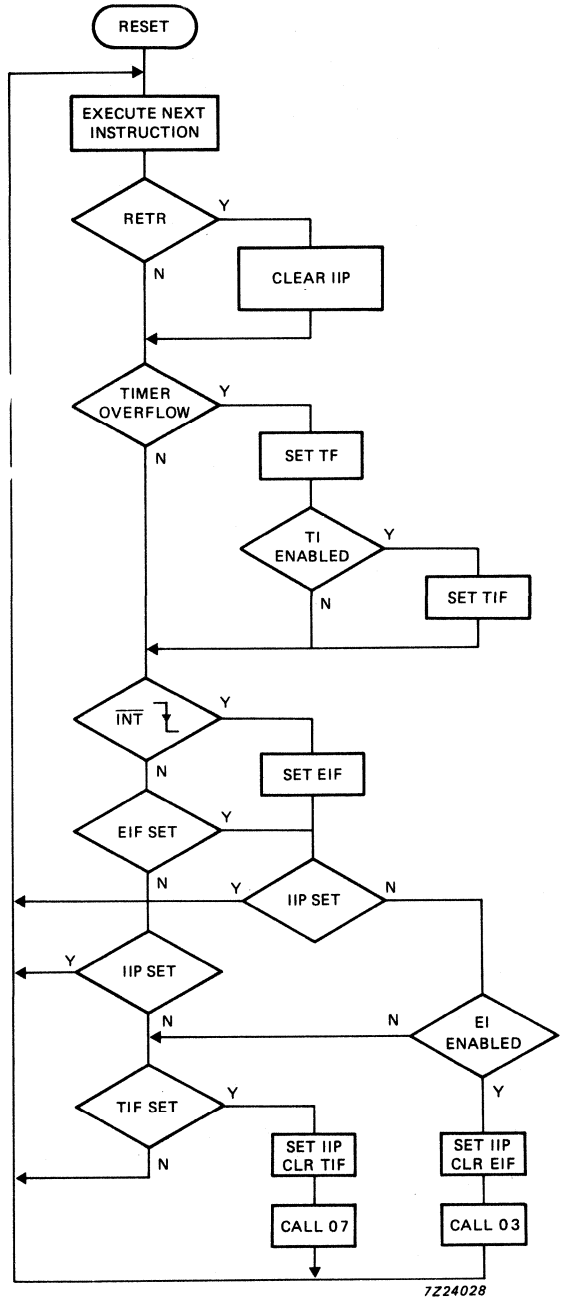
Fig. 13(a) Interrupt logic.

Notes to figure 13(a)

1. CE/$\overline{T0}$ positive edge is always latched in the digital filter/latch.
2. Correct interrupt timing is ensured when CE/$\overline{T0}$ is LOW for $>$ 4 CP followed by a HIGH for $>$ 7 CP.
3. When the interrupt in progress flag is set, further interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.
5. For all flip-flops, RESET overrules SET.

FUNCTIONAL DESCRIPTION (continued)

Interrupts (continued)



EI	External Interrupt
TI	Timer/counter Interrupt
EIF	External Interrupt Flag
TF	Timer Flag
IIP	Interrupt In Progress flag

Fig. 13(b) Interrupt flowchart.

Oscillator (see Fig. 14)

The 3,58 MHz oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-voltage condition is present to prevent discharge of a weak back-up battery.

Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a HIGH level at either the CE/$\overline{T0}$ or RESET pin.

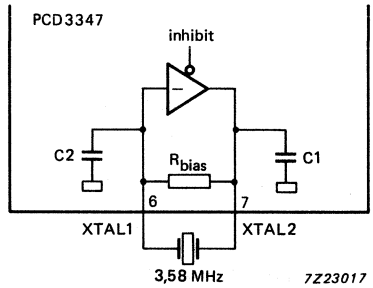


Fig. 14 Oscillator with integrated elements.

The oscillator has an output drive capability from pin 7 (XTAL2). An external clock can be applied to pin 6 (XTAL1). A machine cycle comprises 10 time slots, each time slot being 3 oscillator periods.

In telephony applications the 3,58 MHz crystal provides an 8,4 μs machine cycle. The range of the clock frequency is from 100 kHz up to a maximum which is a function of the supply voltage.

Timer/event counter (see Fig. 15)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 3 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin 8 (T1) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (182,6 kHz for an 8,4 μs machine cycle). When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump if timer flag = 1) or JNTF instruction. Overflow also generates an interrupt to the processor via setting of the Timer Interrupt Flag when the timer/event counter interrupt is enabled.

FUNCTIONAL DESCRIPTION (continued)

Timer/event counter (continued)

Table 3 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

* With prescaler select, PS = 0, the timer counts modulo-32 machine cycles, with PS = 1 it counts modulo-1 cycles (prescaler not used); prescaler cleared with STRT T, prescaler not readable.

** READ does not disturb the counting process.

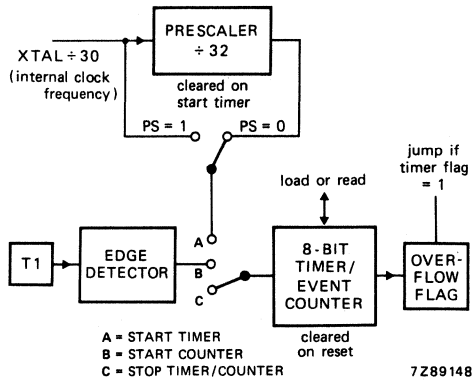


Fig. 15 Timer/event counter.

Program status word (see Fig. 16)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS); 0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS); 0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

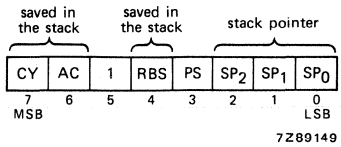


Fig. 16 Program status word.

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program counter (see Fig. 17).

A 12-bit program counter is used to facilitate 8 K bytes of ROM being addressed. The arrangement of the bits is shown in Figure 17. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 12 bits are saved in the stack during CALL and interrupt routines.

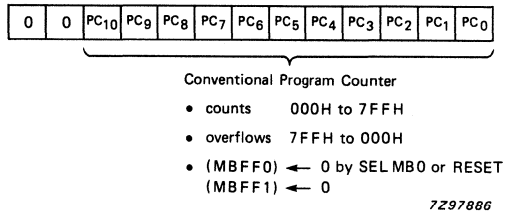


Fig. 17 Program counter.

Central processing unit

The PCD3347 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the CURRENT ROM page.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program.
Table 4 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 4 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JNT0
	0	JT0*
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

* Because of the inverted interrupt input CE/$\overline{T0}$ the conditional jump JT0 is also inverted.

Test input T1 (pin 8)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for $>$ 4 CP, followed by a HIGH for $>$ 4 CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor ($R = \leqslant 100\ k\Omega$).
When T1 is not used pin 8 must be connected to V_{DD} or V_{SS}.

Reset (pin 11)

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory bank 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external and timer)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports according to reset states
- Cancels IDLE and STOP mode

After the voltage is applied to RESET an internal delay of 1866 CP is introduced before the microcontroller commences operation.

Power-on reset

The internal power-on reset circuit monitors the supply voltage V_{DD}. As long as V_{DD} remains below the internal reference level V_{ref} (typically 1,3 V), the oscillator is inhibited and RESET (pin 8) has an undefined level. When V_{DD} rises above V_{ref}, the oscillator is released and RESET is pulled HIGH to V_{DD} by TR1 for a period t_D (typically 50 μs). Note that the start-up time of the oscillator is typically 10 ms because of the narrow bandwidth of the crystal.

Three modes of power-on reset are possible:

1. If V_{DD} has a fast rise time, i.e. V_{DD} reaches its minimum value before the RESET signal finishes (t_D), then no additional circuit is required (see Figs 18 and 19). Note that the first instruction is executed after the oscillator start-up time plus 1866 clock periods.
2. If V_{DD} has a slow rise time then the RESET signal should be stretched by an external CR circuit (see Figs 20 and 21). In the event of a short drop in V_{DD}, the diode path discharges the capacitor rapidly to ensure a reliable power-on reset. The RESET signal should reach at least 70% of the final value of V_{DD} to ensure a correct reset. Given that the RESET voltage and V_{DD} rise exponentially, the above requirement is satisfied when the time constant of the RESET pulse is $>$ 8 times the time constant of V_{DD}. If V_{DD} rises linearly then a RESET time constant $>$ 2 times the rise time of V_{DD} is required.

   When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods (see Fig. 21). If the oscillator starts up prior to the completion of RESET then program execution begins 1866 clock periods after RESET goes LOW.
3. Fig. 22 shows an external reset applied during power-on. The external reset signal must remain HIGH until V_{DD} has reached its minimum operating value corresponding to the selected oscillator frequency. When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods (see Fig. 23). If the oscillator starts up prior to the completion of RESET then program execution begins 1866 clock periods after RESET goes LOW.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

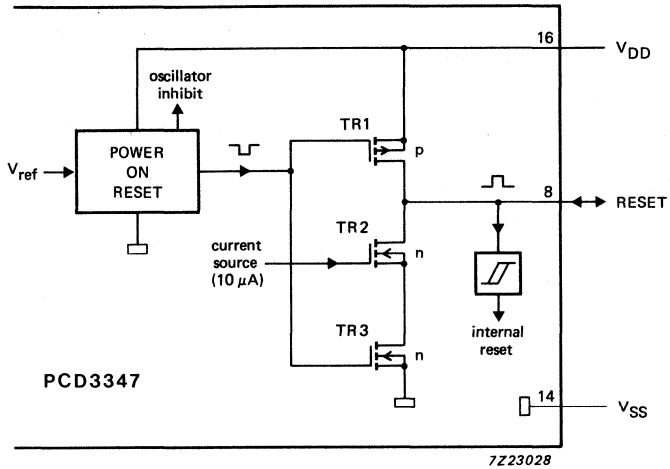


Fig. 18 Power-on reset configuration.

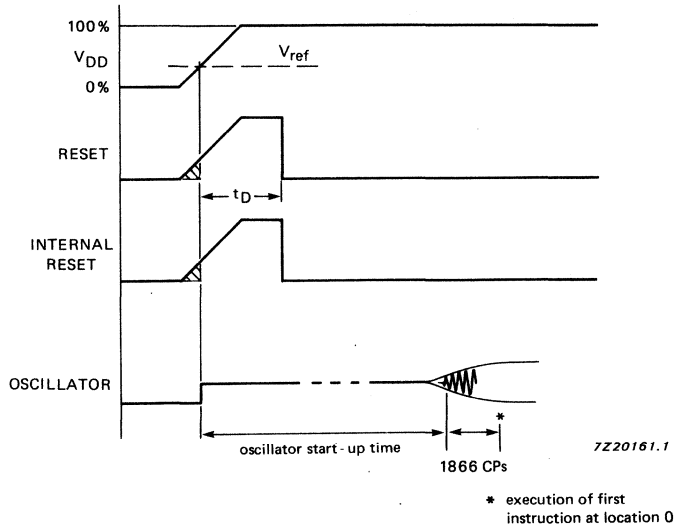


Fig. 19 Timing of power-on reset with fast rise time of V_{DD}.

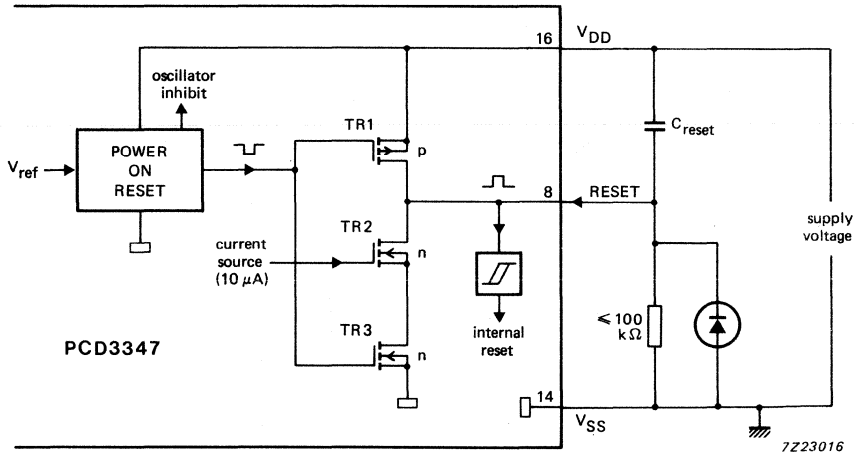


Fig. 20 Stretched power-on reset with external CR circuit.

DEVELOPMENT DATA

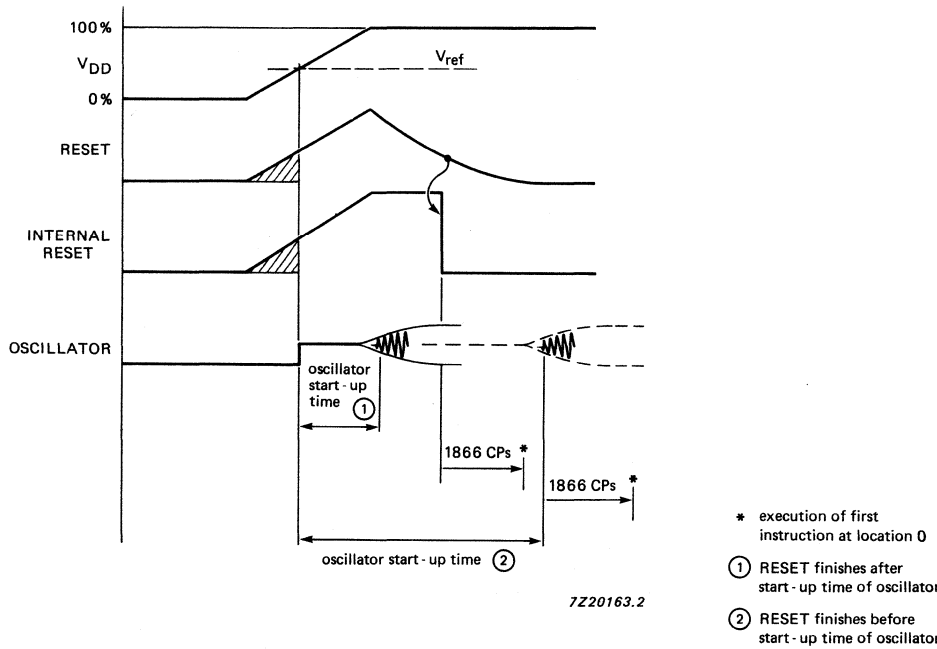


Fig. 21 Timing of power-on reset with a slowly rising V_{DD} and a stretched RESET pulse.

FUNCTIONAL DESCRIPTION (continued)

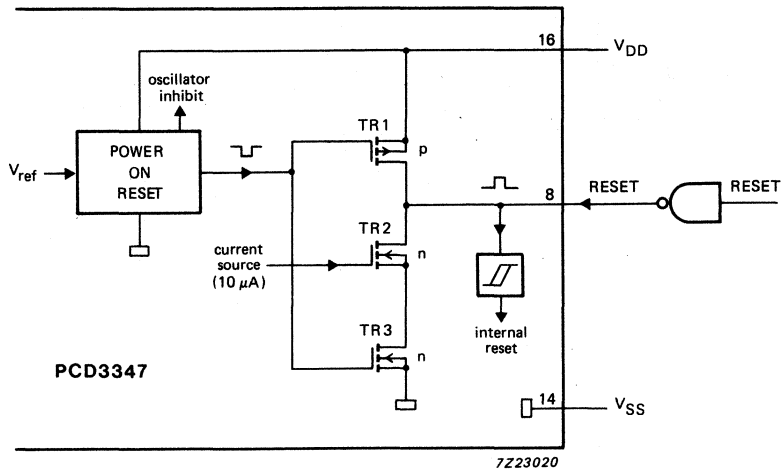


Fig. 22 External power-on reset configuration.

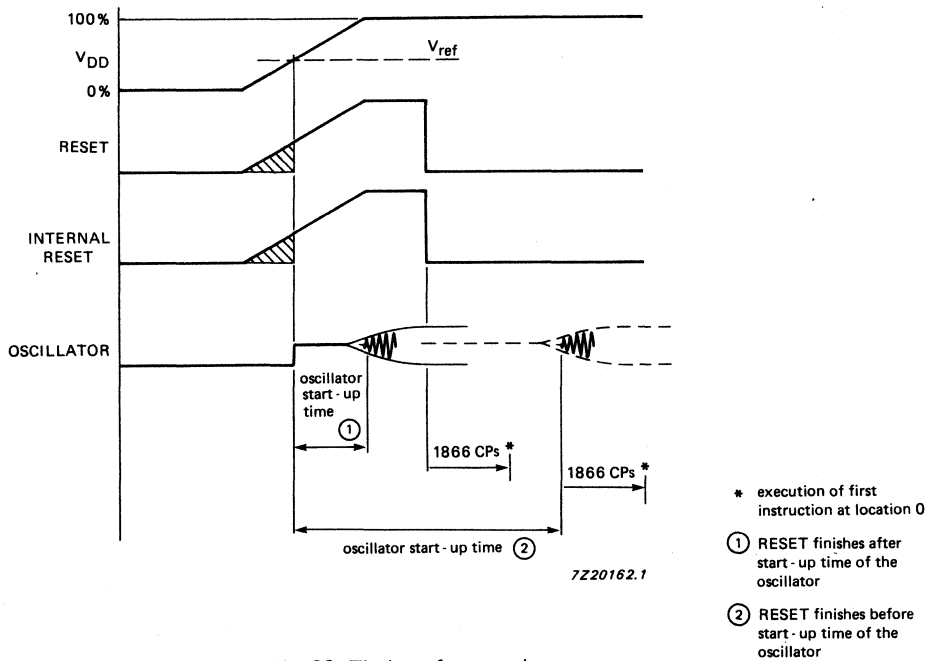


Fig. 23 Timing of external power-on reset.

INSTRUCTION SET

The PCD3347 instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for memory bank selection and derivative control. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 5 details the symbols and definition descriptions that are used in the instruction set of the PCD3347. Table 6 shows the instruction map and Table 7 gives the instruction set.

Table 5 Symbols and definitions used in Tables 6 and 7

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0 to 7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
D	mnemonic for 4-bit digit (nibble)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in page' operation
PC	program counter
Pp	port designation (p = 0 or 1)
PSW	program status word
RB	register bank
Rr	register designation (r = 0 to 7)
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
Dx	derivative register (0 to H'FF')
←	is replaced by
↔	is exchanged with

INSTRUCTION SET (continued)

Table 6 PCD3347 instruction map

first hexadecimal character of opcode ↓

second hexadecimal character of opcode →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, # data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	1	2					
1	INC @Rr 0	1	JB0 addr	ADDC A, # data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0	1	2	3	4	5	6	7
2	XCH A,@Rr 0	1	STOP	MOV A, # data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A,Rr 0	1	2	3	4	5	6	7
3	XCHD A,@Rr 0	1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A 0	1	2					
4	ORL A,@Rr 0	1	MOV A , T	ORL A, # data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0	1	2	3	4	5	6	7
5	ANL A,@Rr 0	1	JB2 addr	ANL A, # data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0	1	2	3	4	5	6	7
6	ADD A,@Rr 0	1	MOV T , A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0	1	2	3	4	5	6	7
7	ADDC A,@Rr 0	1	JB3 addr		CALL page 3			RR A	ADDC A,Rr 0	1	2	3	4	5	6	7
8				RET	JMP page 4				ORL Pp, # data 0	1	2			MOV Dx,A		
9			JB4 addr	RETR	CALL page 4		JNZ addr	CLR C	ANL Pp, # data 0	1	2					
A	MOV @Rr, A 0	1		MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0	1	2	3	4	5	6	7
B	MOV @Rr, # data 0	1	JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr, # data 0	1	2	3	4	5	6	7
C	DEC @Rr 0	1			JMP page 6	SEL RB0	JZ addr	MOV A, PSW	DEC Rr 0	1	2	3	4	5	6	7
D	XRL A,@Rr 0	1	JB6 addr	XRL A, # data	CALL page 6	SEL RB1		MOV PSW, A	XRL A,Rr 0	1	2	3	4	5	6	7
E	DJNZ @Rr,addr 0	1			JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr 0	1	2	3	4	5	6	7
F	MOV A,@Rr 0	1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0	1	2	3	4	5	6	7

Table 7 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

INSTRUCTION SET (continued)

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1})\leftarrow A_n$ $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data	r = 0–7	
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((R0_{0-3}))$ $(A_{0-3})\leftrightarrow((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3)\leftarrow(A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7})\leftarrow(A)$, $(A)\leftarrow((PC))$		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1	
BRANCH	JMP addr	● 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0 address	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1 address			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0 : (PC_{0-7})←addr	
	JT0 addr	36 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JNT0 addr	26 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

INSTRUCTION SET (continued)

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4, 6, 7}$) (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) − 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) − 1 ($PSW_{4, 6, 7}$) + (PC)←((SP))	6

DEVELOPMENT DATA

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	 7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	 7
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	 7
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	 7
DERIVATIVE INPUT/OUTPUT	MOV Dx, A	8D	2/2	move accumulator contents to derivative register	(Dx)←(A) x = 0 to 255	8
	NOP	00	1/1	no operation		

Notes to Table 7

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).
5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 0000P23, P22, P21, P20; PCD3347 Port 2 is not bonded.
8. Instructions for PCF3300 only.

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 16	V_{DD}	−0,8	+8	V
Input voltage	any pin	V_I	−0,8	V_{DD} + 0,8	V
DC current	any input or output	$\pm I_I, \pm I_O$	–	10	mA
Total power dissipation	derate according to thermal resistance	P_{tot}	–	500	mW
Power dissipation	per output	P_O	–	50	mW
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−25	+70	°C
Operating junction temperature		T_j	–	+125	°C
Thermal resistance junction to ambient	SOT146	$R_{th\ j\text{-}a}$	–	120	K/W
	SOT163A	$R_{th\ j\text{-}a}$	–	150	K/W

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 100 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage						
operating		V_{DD}	2,5	–	6	V
STOP mode for RAM data retention		V_{DD}	1,0	–	6	V
Supply current (Fig. 25)						
operating with tone generator on	V_{DD} = 3 V	I_{DD}	–	800	–	μA
operating without tone generator	V_{DD} = 3 V	I_{DD}	–	400	–	μA
IDLE mode (Fig. 26)						
with tone generator on	V_{DD} = 3 V	I_{DD}	–	600	–	μA
without tone generator	V_{DD} = 3 V	I_{DD}	–	200	–	μA
STOP mode (Fig. 27)	note 1; V_{DD} = 1,8 V					
	T_{amb} = 25 °C	I_{DD}	–	1,5	2,0	μA
	T_{amb} = 55 °C	I_{DD}	–	–	5	μA
	T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O						
Switching level		V_{RESET}	–	1,3	–	V
Sink current	$V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs						
Input voltage LOW		V_{IL}	0	–	0,3 V_{DD}	V
Input voltage HIGH		V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Input leakage current	$V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs						
Output voltage LOW	V_I = V_{SS} or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW for all remaining ports	V_{DD} = 3 V; V_O = 0,4 V	I_{OL}	1,5	2,5	–	mA
Pull-up output source current HIGH (Fig. 29)	V_{DD} = 3 V;					
	V_O = 0,7 V_{DD}	$-I_{OH}$	10	–	–	μA
	V_O = V_{SS}	$-I_{OH}$	–	–	300	μA
Push-pull output source current HIGH	V_{DD} = 3 V;					
	V_O = V_{DD} −0,4 V	$-I_{OH}$	0,6	1,5	–	mA

Note 1

Crystal connected between XTAL1 and XTAL2; CE and T1 at V_{SS}.

TONE GENERATOR CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 100 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Tone output (Fig. 24)						
DTMF output voltage levels (r.m.s. values)						
HIGH group		$V_{HG(rms)}$	158	192	205	mV
LOW group		$V_{LG(rms)}$	125	150	160	mV
Frequency deviation		$\Delta f/f$	−0,6	–	+ 0,6	%
DC voltage level		V_{dc}	–	½ V_{DD}	–	V
Output impedance		$\|Z_O\|$	–	0,1	0,5	kΩ
Load resistance		R_L	10	–	–	kΩ
Pre-emphasis of group		ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion	note 2; T_{amb} = 25 °C	THD	–	−25	–	dB

Note 2

Related to the level of the LOW group frequency component (CEPT CS 203)

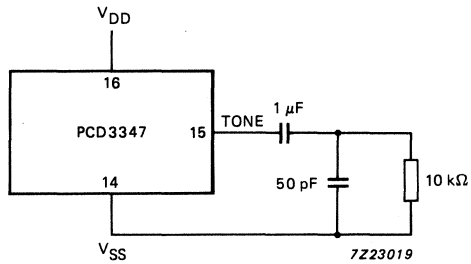


Fig. 24 Tone output test circuit.

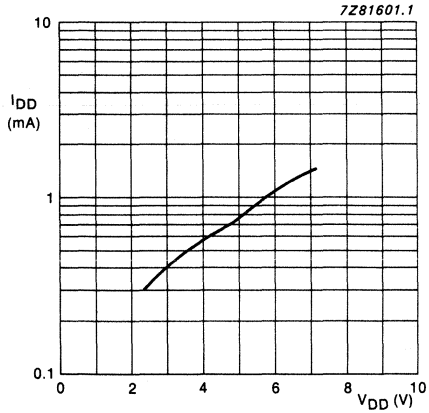


Fig. 25 Typical supply current (I_{DD}) in operating mode as a function of the supply voltage (V_{DD}); T_{amb} = 25 °C; clock frequency = 3,58 MHz; I_{DD} is increased by approximately 0,6 mA when the DTMF function is operating.

DEVELOPMENT DATA

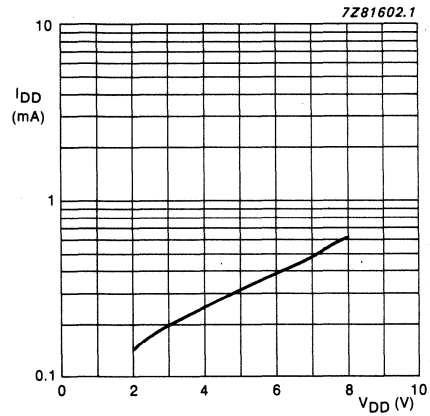
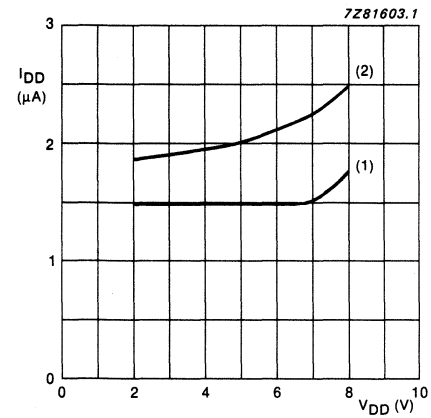
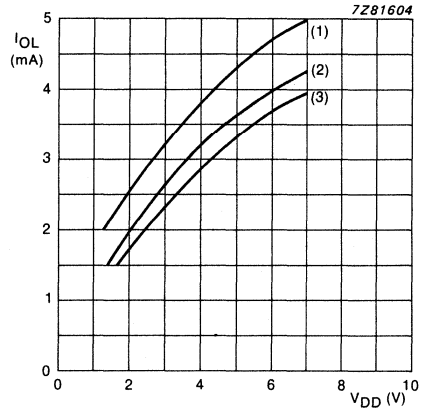


Fig. 26 Typical supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}); T_{amb} = 25 °C; clock frequency = 3,58 MHz.



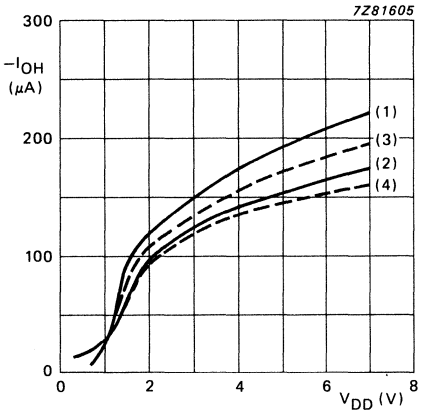
(1) T_{amb} = 25 °C
(2) T_{amb} = 70 °C

Fig. 27 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).



(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = 25\ ^{o}C$
(3) $T_{amb} = 70\ ^{o}C$

Fig. 28 Output sink current LOW (I_{OL}), as a function of supply voltage (V_{DD}); $V_O = 0{,}4$ V.



(1) $T_{amb} = 25\ ^{o}C$; $V_O = V_{SS}$
(2) $T_{amb} = 25\ ^{o}C$; $V_O = 0{,}7\ V_{DD}$
(3) $T_{amb} = 70\ ^{o}C$; $V_O = V_{SS}$
(4) $T_{amb} = 70\ ^{o}C$; $V_O = 0{,}7\ V_{DD}$

Fig. 29 Output source current HIGH ($-I_{OH}$) as a function of supply voltage (V_{DD}).

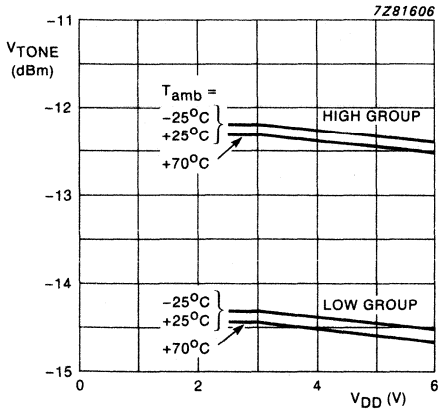


Fig. 30 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

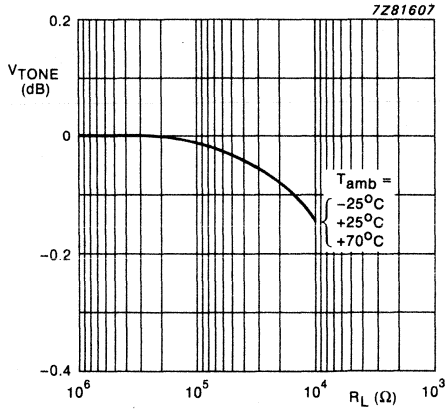


Fig. 31 Dual tone output voltage level as a function of output load resistance.

DEVELOPMENT DATA

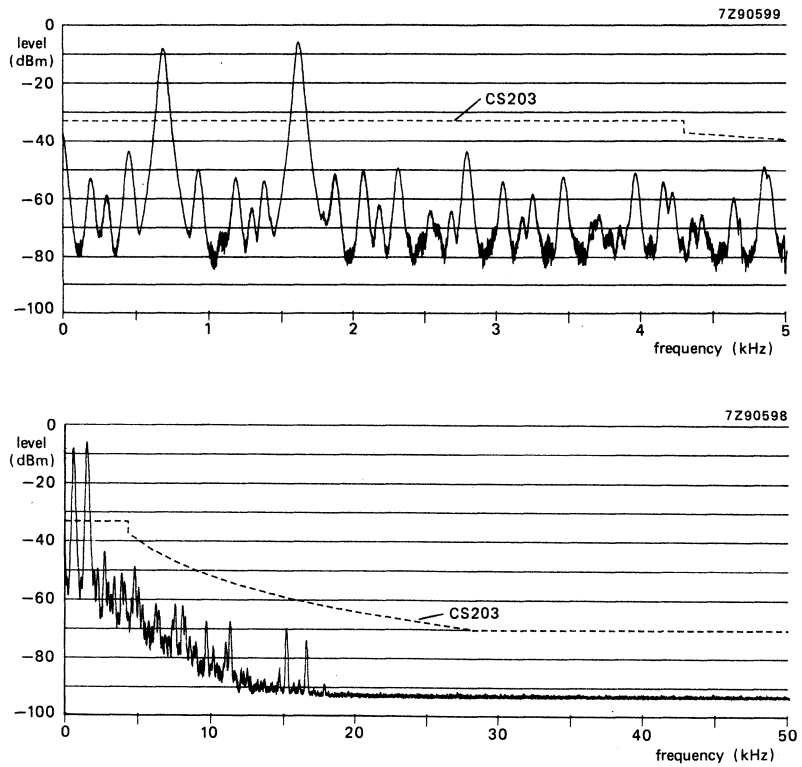


Fig. 32 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

A block diagram of an electronic featurephone built around the PCD3347 is shown in Figure 31. It comprises the following dedicated telephony ICs:

- TEA1060/1061/1067/1068 transmission circuit for telephony
- PCF8576 or PCF8577 2 LCD drivers in LCD module MB7020160
- PCF8571 1 K RAMs with Serial I/O; the number of RAMs depends on the required amount of stored telephone numbers
- PCD3360 programmable multi-tone ringer

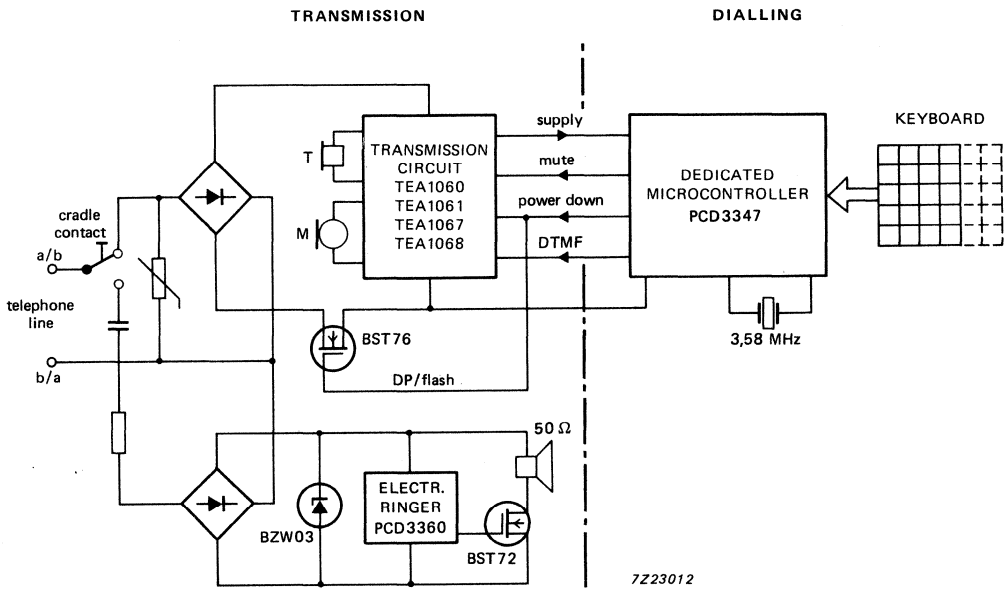


Fig. 33 Block diagram of electronic featurephone with common line interface.

Philips Components

Data sheet	
status	Product specification
date of issue	October 1990

PCD3348

CMOS microcontroller for telephone sets

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 8 K ROM bytes
- 256 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{TO}$)
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O which can be used in bus systems with more than one master (serial I/O data via an existing port line and clock via a dedicated line); tailored for I²C-bus communications
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles
- Clock frequency 450 kHz to 10 MHz
- Single supply voltage from 1.8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals (e.g. PCD3312C DTMF generator)
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C.

GENERAL DESCRIPTION

The PCD3348 is a single-chip 8-bit microcontroller fabricated in CMOS. It has special on-chip features for applications in telephone sets. The device is mask programmable, designed to provide telephone dialling facilities such as redial, repertory dial, emergency call, keyboard scan and control for liquid crystal display, pulse dial and/or DTMF dial via dedicated peripheral.

For detailed information see the PCD33XX family specification.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3348P	28	DIL	plastic	SOT117
PCD3348T	28	mini-pack	plastic	SO28; SOT136A

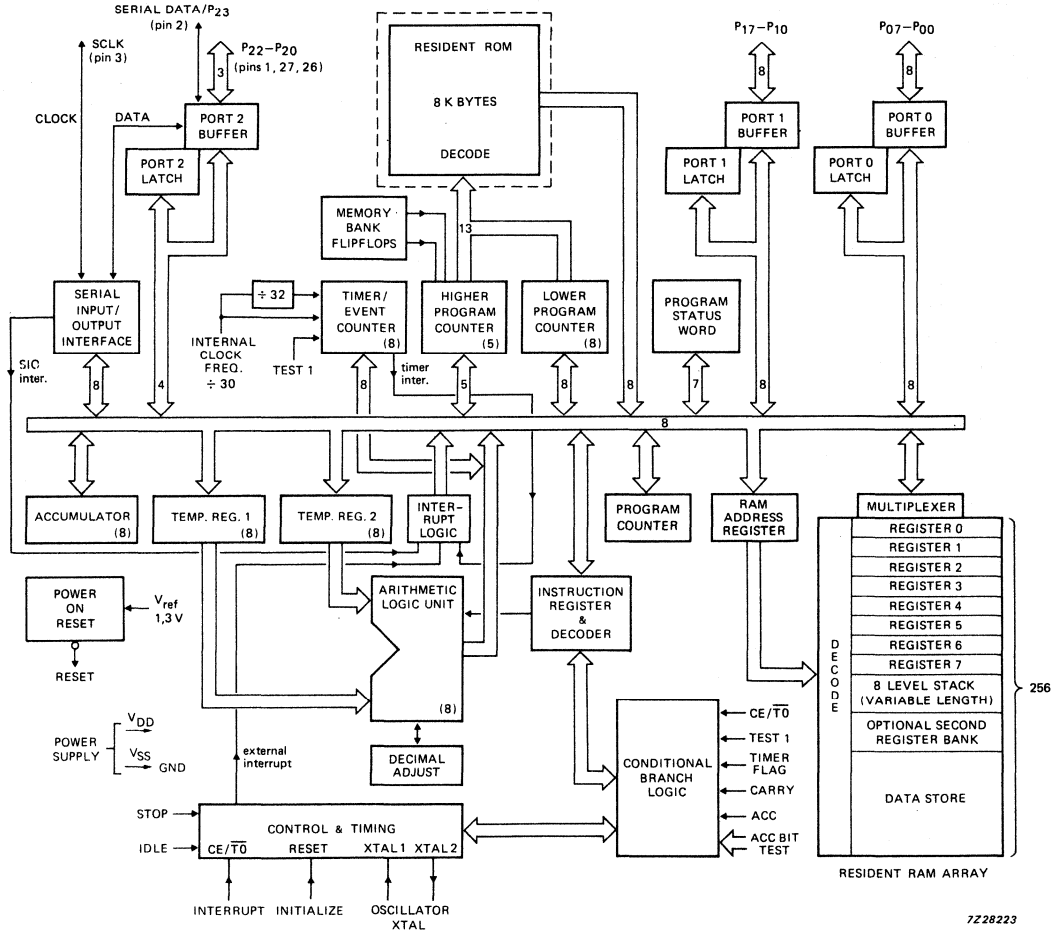
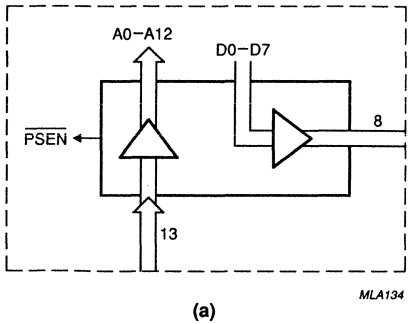


Fig.1 Block diagram.



(a)

Fig.1a Replacement of dotted part in Fig.1, for the PCD3301B 'Piggy-back' version.

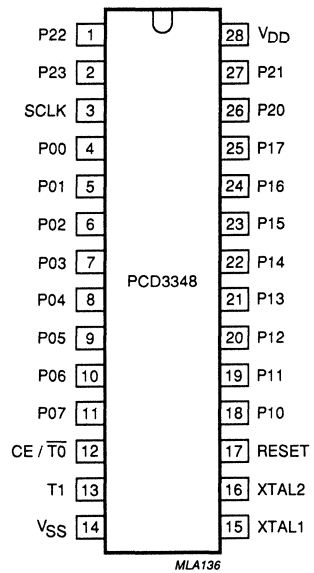


Fig.2 Pinning diagram: PCD3348 and bottom pinning PCD3301B.

PINNING

SYMBOL	PIN	DESCRIPTION
SCLK	3	**Clock:** bidirectional clock for serial I/O.
P00-P07	4-11	**Port 0:** 8-bit quasi-bidirectional I/O port.
CE/$\overline{TO}$	12	**Interrupt/Test 0:** external interrupt input (sensitive to positive-going edge) test input pin; when used as a test input directly tested by conditional branch instructions JTO and JNTO.
T1	13	**Test 1:** test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
V_{SS}	14	**Ground:** circuit earth potential.
XTAL1	15	**Crystal input:** connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
XTAL2	16	Connection to the other side of the timing component.
RESET	17	**Reset input:** used to initialize the processor (active HIGH), or output of power-on reset circuit.
P10-P17	18-25	**Port 1;** 8-bit quasi-bidirectional I/O port.
P20-P23	26, 27, 1, 2	**Port 2:** 4-bit quasi-bidirectional I/O port. P23 is the serial data input/output in serial I/O mode.
V_{DD}	28	**Power supply;** 1.8 V to 6 V.

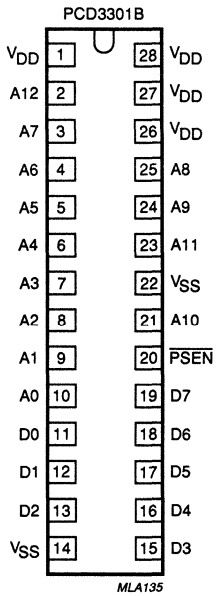


Fig.3 Pinning diagram: PCD3301B 'Piggy Back' version top pinning; to access a 2732 or 2764 EPROM.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SS}	14, 22	**Ground**
V_{DD}	1, 26-28	**Power supply**
A0-A12	10-3, 25, 24, 21, 23, 2	**Address outputs**
D0-D7	11-13, 15-19	**Data**
$\overline{PSEN}$	20	**Program Store Enable**

Notes

1. Access time for ROM/EPROMS to be below $7 \times 1/f_{XTAL}$.

FUNCTIONAL DESCRIPTION

'Piggy-Back' version PCD3301B

The PCD3301B is a special package that has standard pinning to the bottom which facilitates insertion as a mask-programmed device. An EPROM can be mounted on top in an additional socket. The total package height is greater than the standard DIL package. The RAM has 256 bytes and can also address 8 Kbytes of program memory.

Program memory PCD3348

The program memory consists of 8192 bytes (8-bit words), in a read-only memory (ROM). Each location is directly addressable by the Program Counter. The memory is mask-programmed at the factory. Figure 4 shows the program memory map.

Four program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET).
- Location 3; contains the first byte of an external interrupt service subroutine.
- Location 5; contains the first byte of a serial I/O interrupt service subroutine.
- Locations 7; contains the first byte of a timer/event counter interrupt service subroutine.

Program memory is arranged in banks of 2 Kbytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using the unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

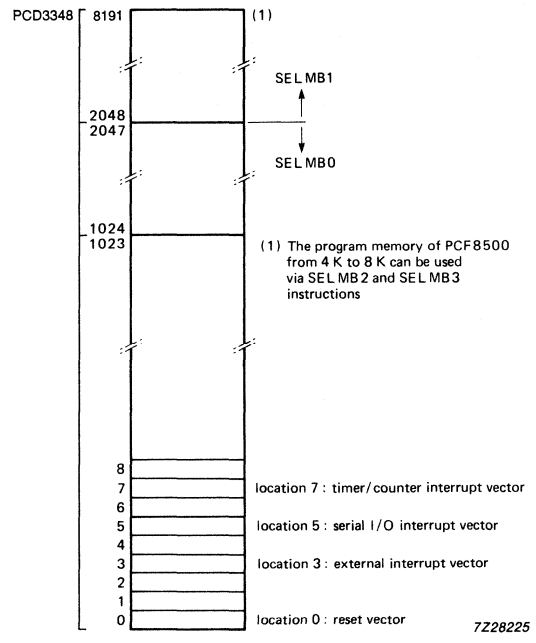


Fig.4 Program memory map.

Data memory PCD3348

Data memory consists of 256 bytes (8-bit words), random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable.

Memory also includes an 8-level Program Counter stack addressed by a 8-level Program Counter stack addressed by a 3-bit Stack Pointer. Figure 5 shows the data memory map.

WORKING REGISTERS

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

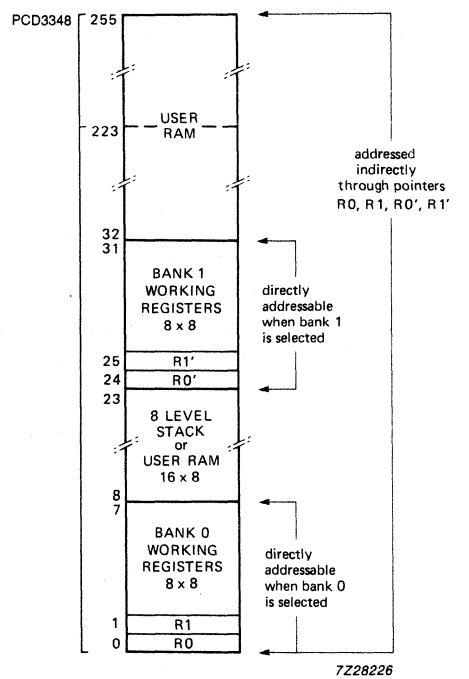


Fig.5 Data memory map.

PROGRAM COUNTER STACK

Locations 8 to 23 may be designated as an 8-level Program Counter stack (2 locations per level), or as general purpose RAM. The Program Counter stack (Fig.6) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the Program Counter prior to servicing the subroutine.

A 3-bit Stack Pointer determines which of the eight register pairs of the Program Counter stack will be loaded with the next generated return address. The Stack Pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the Program Counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The Stack Pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the Stack Pointer decrements by one and the contents of the register pair on top of the stack are transferred to the Program Counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations. Possible locations from 32 to 223 may be used for storage of program variables or data.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the Stack Pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the Program Counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the Program Counter return address is saved; with a subroutine CALL, the saved Program Counter value is one less than the computer counter return address.

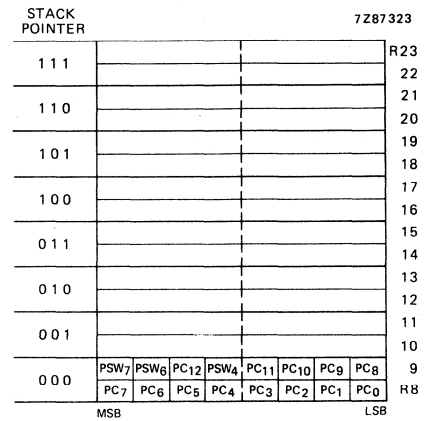


Fig.6 Program Counter stack.

IDLE and STOP modes

IDLE MODE

When the microcontroller enters the IDLE mode via the IDLE instruction (01H) the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode by one of three interrupts if they are enabled or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig.7).

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A LOW-to-HIGH transition on the external interrupt pin (CE/$\overline{TO}$) reactivates the microcontroller. A HIGH level applied to CE/$\overline{TO}$ will reactive the microcontroller only in the STOP mode. Thus, if CE/$\overline{TO}$ was HIGH before the microcontroller entered the IDLE mode, it must go LOW before the microcontroller can be reactivated (see Fig.8).

Wake-up from the IDLE mode is ensured when CE/$\overline{TO}$ is LOW for 4 clock periods followed by a HIGH for 7 clock periods. After the initial forced CALL 003H operation (60 clock periods) the program continues with the external interrupt service routine.

STOP MODE

The microcontroller enters the STOP mode by the STOP instruction (22H). The oscillator is switched off. The internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input by an external RESET signal. When one of these two signals is applied an internal delay of 1866 clock periods is provided to ensure that all internal clocks are operating correctly before restart (see Fig.9).

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence executed. If the microcontroller exits the STOP mode by pulling the external interrupt pin HIGH, an interrupt pin sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a HIGH level applied at the CE/$\overline{TO}$ pin, and not by a LOW-to-HIGH transition as in a normal interrupt mechanism. When the CE/$\overline{TO}$ level is active during the STOP instruction then no STOP is executed.A HIGH level on the external interrupt input of at least 1 µs will cause the microcontroller to exit the STOP mode.

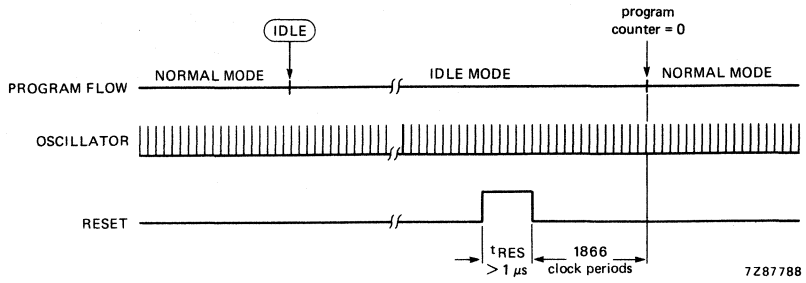


Fig.7 Exit from IDLE mode via RESET.

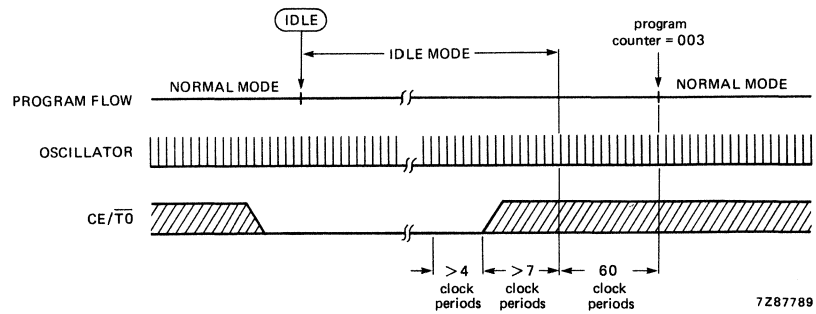


Fig.8 Exit from IDLE mode via an interrupt.

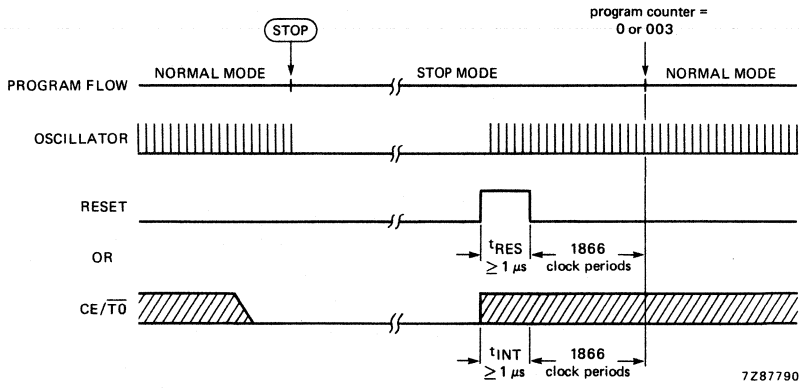


Fig.9 Entering and leaving the STOP mode.

I/O facilities

The PCD3348 family has 23 I/O lines arranged as:

Port 0	Parallel port of 8 lines (P00 to P07)
Port 1	Parallel port of 8 lines (P10 to P17)
Port 2	Parallel port of 4 lines (P20 to P23)
SCLK	Serial I/O consisting of a data line shared with a parallel port line (P23) and a separate clock line SCLK
CE/$\overline{TO}$	External interrupt and test input. When used as a test input can be directly tested by conditional branch instructions JTO and JNTO
T1	Test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

PARALLEL PORTS

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional. Output data written to a port is latched and remains unchanged until rewritten. Input data is not latched and so must be present until read by an input instruction. Input lines are fully CMOS compatible, output lines can drive one LS-TTL or CMOS load.

Fig.11 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source. Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current provides sufficient source current for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output. When a logic 1 is written to the line for the first time MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

In telephone applications this switched pull-up source may not be sufficient. Therefore the PCD3348 offers the possibility to select individually 19 of the 20 parallel port pins (not P23), by the following mask options:

Option 1 STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 µA (typical) and P-channel booster transistor TR2 (1.5 mA). TR2 is only active during 1 clock cycle (0.28 µs at 3.58 MHz).

Option 2 OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig.12).

Option 3 PUSH-PULL OUTPUT; drive capability of the output will be 1.5 mA (typical) at V_{DD} = 3 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must only be used as outputs (Fig.13).

Also, individual mask selection of the RESET state of these port pins can be achieved by appending the following options S and R to options 1, 2 or 3.

Option S SET; after RESET this pin will be initialized to HIGH.

Option R RESET; after RESET this pin will be initialized to LOW.

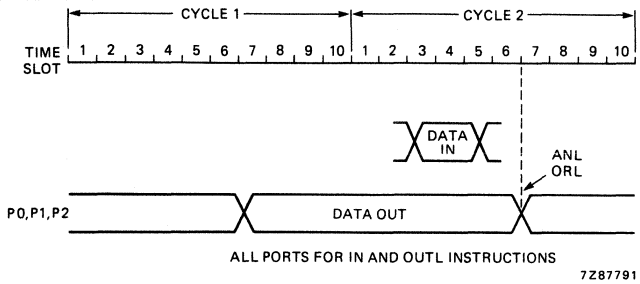


Fig.10 Timing diagram of all ports on IN and OUTL instructions; for ANL and ORL instructions, the ports change on the time slot 7 of cycle 2.

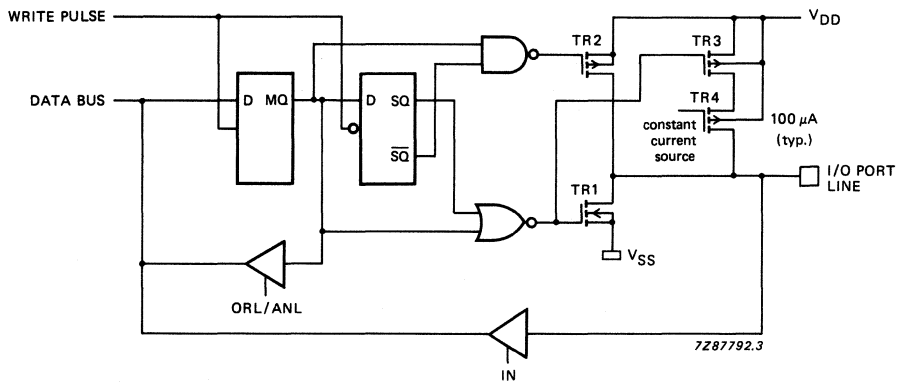


Fig.11 Standard output with switched pull-up current source.

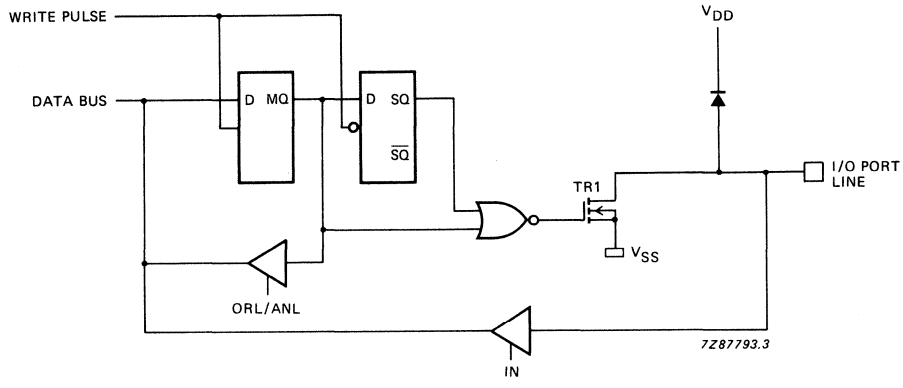


Fig.12 Open drain output.

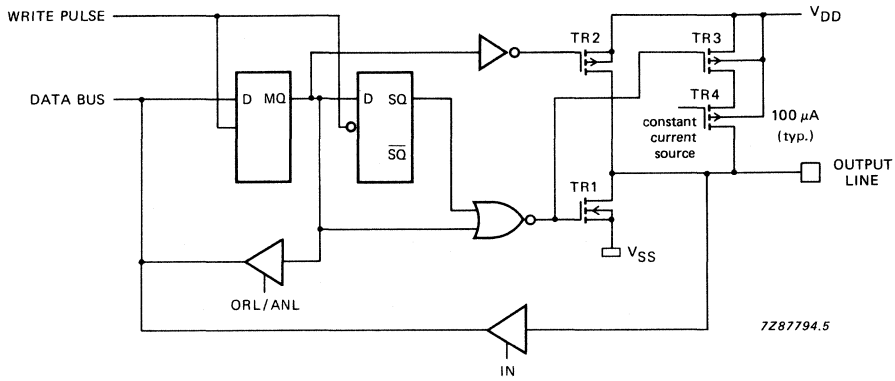


Fig.13 Push-pull output.

SERIAL I/O (SIO)

The PCD3348 has an on-chip serial I/O interface. This SIO interface is a versatile feature in an intelligent telephone set, as shown in application diagram Fig.32. In this application the SIO is used communicate with different peripherals, such as:

- DTMF generator (PCD3312C)
- LCD drivers (PCF8577)
- External RAM (PCD8571)
- Clock calendar (PCB8573)

No extra hardware is required for decoding, addressing and data processing.

Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCD3343 only when a complete byte is received. It then reads the data byte in one instruction. Likewise, during transmission the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data. The microcontroller in only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

The design of the PCD3348 serial I/O system allows any number of devices from the clips family to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address.
Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCD3348 is switched off. This means that the serial I/O logic will remain in the state it was at the occurrence of the STOP instruction. To avoid 'bus block' problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction. This must be carried out only when the PCD3348 has finished a serial data transfer.

SERIAL I/O INTERFACE (tailored for I^2C-bus communications)
Fig.14 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 3 (SCLK) while the data lines share pin 2 (serial data) with the I/O line P23 of Port 2. When the serial I/O is enabled, P23 is disabled as a parallel port line; (P23 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register.

Data Shift Register (S0)

Register S0 converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while interface bits can only be read.

MST and **TRX**
These bits determine the operating mode of the serial I/O interface as shown in Table 1.

Table 1 Operating modes of the serial I/O interface.

MST	TRX	OPERATING MODE
0	0	Slave receiver
1	0	Master receiver
0	1	Slave transmitter
1	1	Master transmitter

BB (Bus Busy)

This flag indicates the status of the bus.

PIN (Pending Interrupt Not)

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO (Enable Serial Output)
The ESO flag enables/disables the serial I/O interface: ESO = '1' enables, ESO = ;0; disables. ESO can only be written by software.

BC0, **BC1** and **BC2**

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL (Arbitration Lost)

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, looses a bus arbitration procedure.

AAS (Addressed As Slave)

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

ADO (Address Zero)

This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB (Last Received Bit)

This contains either the last data bit received, or a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

Serial clock control word (S2)

Bits 0 to 4 of the Clock Control Register S2 are used to set the frequency of the serial clock signal. When a 3.58 MHz crystal is used, the frequency of the serial clock can be varied between 92 kHz and 580 Hz (see Table 2). An asymmetrical clock with a HIGH-to-LOW ratio of 3 : 1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O. S2 is a write only register.

Address Register

The Address Register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The Address Register can be written to using the MOV S0, A and MOV S0, #data instructions, but only when ESO = '0'.

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When the logic is enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt is still indicated by PIN in S1, allowing the interrupt to be serviced. However, vectored interrupt will not occur.

Table 2 S10 clock pulse frequency control when using a 3.58 MHz crystal.

HEXADECIMAL S20-S24 CODE	DIVISOR	f_{SCLK} (kHz) (approx.)
0 (note 1)	-	-
1	39	92
2	45	80
3	51	70
4	63	57
5	75	48
6	87	41
7	99	36
8	123	29
9	147	24
A	171	21
B	195	18
C	243	15
D	291	12
E	339	11
F	387	9.2
10	483	7.4
11	579	6.2
12	675	5.3
13	771	4.6
14	963	3.7
15	1155	3.1
16	1347	2.7
17	1539	2.3
18	1923	1.9
19	2307	1.6
1A	2691	1.3
1B	3075	1.2
1C	3843	0.93
1D	4611	0.78
1E	5379	0.67
1F	6147	0.58

Note

1. This value is not allowed.

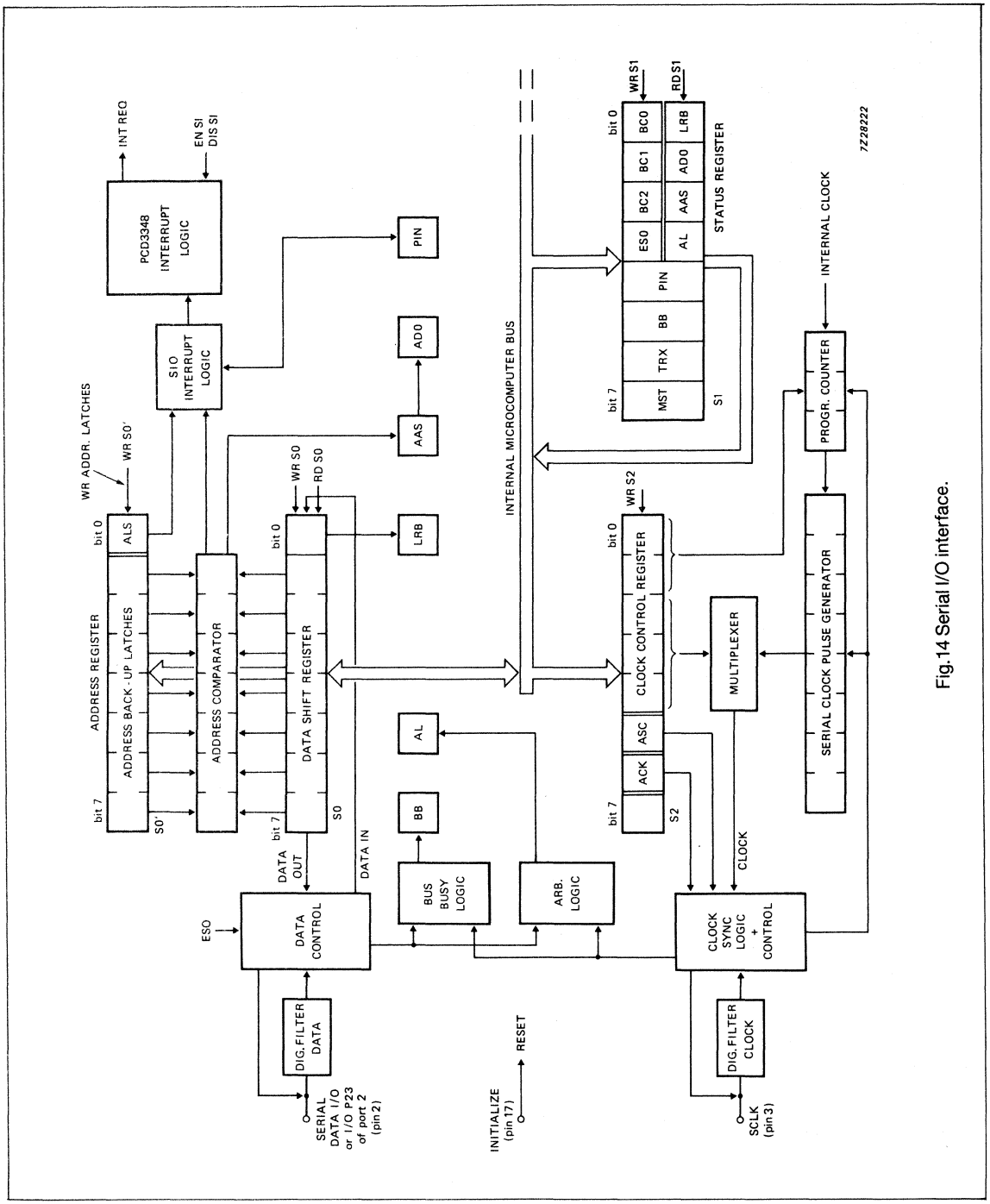


Fig.14 Serial I/O interface.

Interrupts (see Fig.15)

When the external interrupt is enabled, a LOW-to-HIGH transition on the CE/$\overline{TO}$ input initiates an external interrupt subroutine which causes a CALL to program memory location 3 following completion of the current instruction. The interrupt must remain enabled until the interrupt instruction is completed, otherwise the next instruction of the main program will be executed. Serial I/O interrupt, when enabled, causes a CALL to location 5, and a timer/event counter overflow forces a CALL to location 7 when the timer interrupt is enabled.

When an interrupt subroutine starts, the contents of the Program Counter bits 4, 6 and 7 of the PSW have been saved in the Program Counter stack. Accumulator contents have to be saved by software. Interrupt acknowledgement can be carried out by software via port pins. All interrupt subroutines must reside in memory bank 0.

Since the interrupt system is single level, once an interrupt is detected, all further interrupt requests are latched, but ignored, pending a RETR instruction to re-enable the interrupt input logic. After executing RETR, the program continues in the main part; this is independent of the occurrence of a second interrupt during the running of the first routine. If 2 or 3 interrupts occur simultaneously, their priority is:

1. External
2. Serial I/O
3. Timer/event counter

An external interrupt can be generated by using the timer/counter in the event counter mode. The counter is first preset to (FFH), then the EN TCNTI instruction is executed. A LOW-to-HIGH transition of the T1 input will then initiate an interrupt subroutine and cause a CALL to location 7.

On execution of a DIS 1 instruction, the PCD3348 always clears the digital filter/latch and the External Interrupt Flag. The Timer Flag (TF) is reset only when the JTF or JNTF instruction is executed or after RESET. The Timer Interrupt Flag is set when timer overflow occurs, only if the timer interrupt is enabled.

The microcontroller will exit the IDLE mode when any one of the following three interrupts is enabled:

- external
- serial I/O
- timer/event counter.

There is no internal pull-up or pull-down device connected to the external interrupt input (pin 12). If required pin 12 must be externally connected to a resistor ($R \leq 100\ k\Omega$). When the external interrupt is not used pin 12 must be connected to V_{SS}.

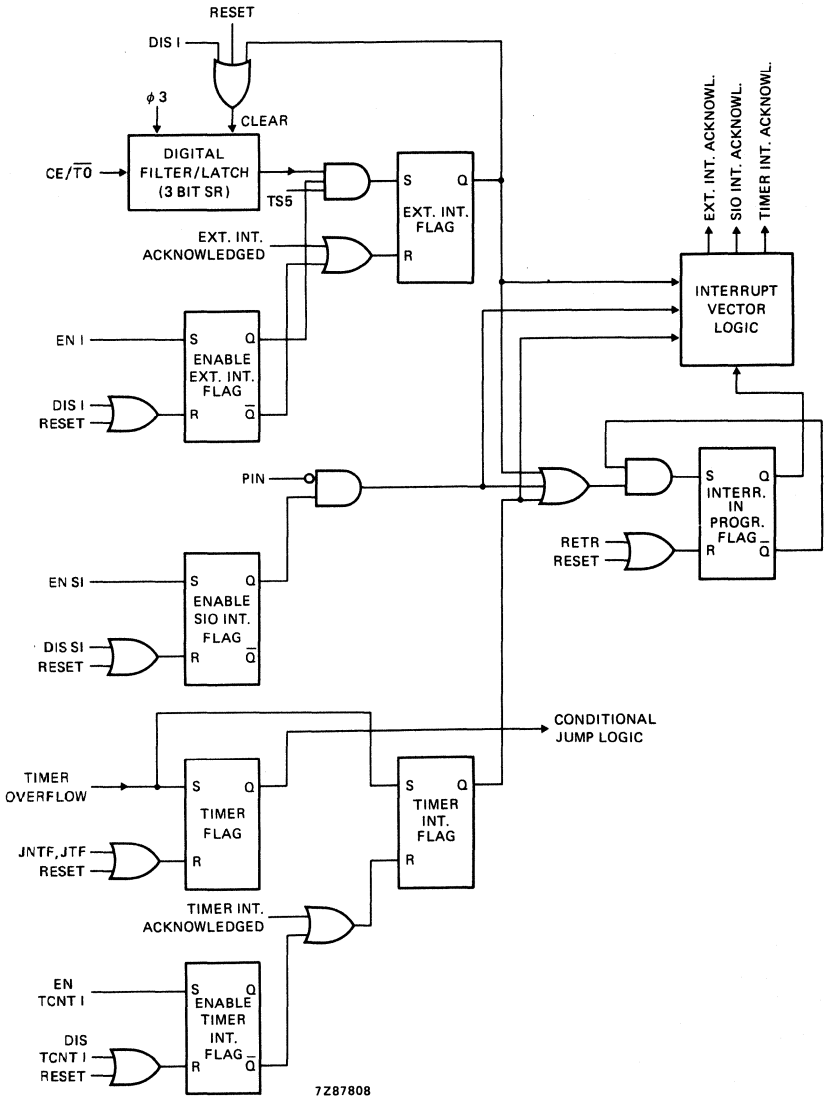


Fig.15 Interrupt logic.

Notes to Fig.15

1. CE/$\overline{TO}$ positive edge is always latched in the digital filter/latch.
2. Correct interrupt timing is ensured when CE/$\overline{TO}$ is LOW for < 4 CP followed by a HIGH for > 7 CP.
3. When the interrupt in progress flag is set, further interrupts are latched but ignored, until RETR is executed.
4. A DIS 1 instruction always clears a pending external interrupt.

Oscillator

The 3.58 MHz oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-voltage condition is present to prevent discharge of a weak back-up battery. Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a HIGH level at either the CE/$\overline{TO}$ or RESET pin. The oscillator has the output drive capability for the DTMF generator (PCD3311C/3312C) via pin 16 (XTAL2). An external clock can be applied to pin 15 (XTAL1). A machine cycle consists of 10 time slots, each time slot being 3 oscillator periods.

In telephony applications the 3.58 MHz crystal provides a 8.4 µs machine cycle. The range of the clock frequency is from 450 kHz up to a maximum which is a function of the supply voltage (see Fig.23).

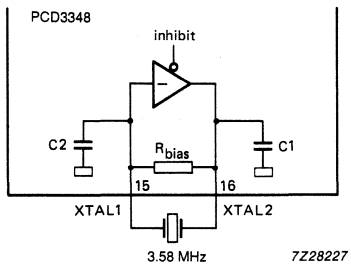


Fig.16 Oscillator with integrated elements.

Timer/event counter

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 3 gives the instructions that control the counter and prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin 13 (T1) are counted. The maximum rate at which the counter may be incremented is once very machine cycle (182.6 kHz for a 8 µs machine cycle). When the counter overflows, the Timer Flag is set. The flag can be tested and reset using the JTF (jump if Timer Flag = 1) or JNTF instruction.

Overflow also generates an interrupt to the processor via setting of the Timer Interrupt Flag when the timer/event counter interrupt is enabled.

Table 3 Timer/event counter control.

FUNCTION	TIMER MODE MODULO-1, MODULO-32 (1)	COUNTER MODE
CLEAR	MOV T, A (A) = 0 or RESET	MOV T, A (A) = 0 or RESET
PRESET	MOV T, A	MOV T, A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ (2)	MOV A, T	MOV A, T

Notes to Table 3

1. With prescaler select, PS = 0, the timer counts modulo-32 machines cycles, with PS = 1 it counts modulo-1 cycles (prescaler not used); prescaler cleared with STRT T, prescaler not readable.
2. READ does not disturb the counting process.

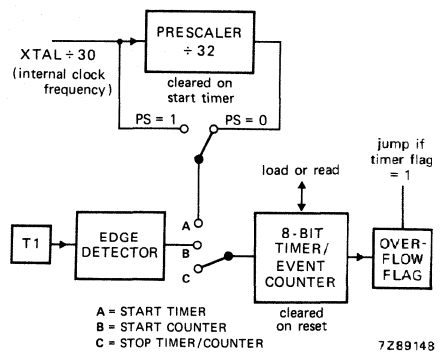


Fig.17 Timer/event counter.

Program Status Word

The Program Status Word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.

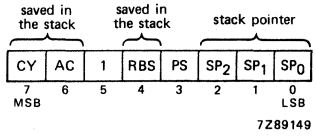


Fig.18 Program Status Word.

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the Program Counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program Counter

A 13-bit Program Counter is used to facilitate 8 K of ROM being addressed. The arrangement of the bits is shown in Fig.19. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 13 bits are saved in the stack during CALL and interrupt routines.

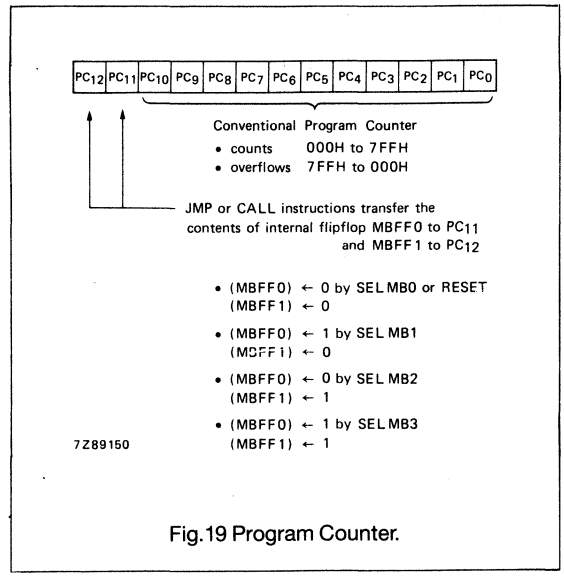


Fig.19 Program Counter.

Table 4 Program Status Word bits.

BIT	DESCRIPTION
0 to 2	Stack Pointer bits (SP_0), SP_1, SP_2)
3	prescaler select (PS); 0 = modulo-32; 1 = modulo-1 (no prescaling)
4	working register bank select (RBS); 0 = register bank 0; 1 = register bank 1
5	not used
6	auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
7	carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

Central Processing Unit

The PCD3348 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOV A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 5 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Test input T1 (pin 13)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for > 4 CP, followed by a HIGH for > 4 CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

Reset

A positive-going signal on the RESET input/output:

- Sets the Program Counter to zero
- Selects location 0 of memory bank 0 and register bank 0
- Sets the Stack Pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the Timer Flag
- Sets all ports according to reset states
- Sets the serial I/O to slave receiver mode and disable the serial I/O
- Cancels IDLE and STOP mode

After the voltage is applied to RESET an internal delay of 1866 CP is introduced before the micro-controller commences operation.

Table 5 Conditional branches.

TEST	JUMP CONDITION	JUMP INSTRUCTION
Accumulator	all bits zero any bit non-zero	JZ JZN
Accumulator bit test	1	JB0 to JB7
Carry flag	1 0	JC JNC
Timer overflow flag	1 0	JTF JNTF
Test input T0	1 0	JNTO JTO (note 1)
Test input T1	1 0	JT1 JNT1
Register	non-zero	DJNZ

Note

1. Because of the inverted interrupt input CE/$\overline{TO}$ the conditional jump JTO is also inverted.

Power-on-reset and low-voltage detection

In telephony applications, correct operation of the PCD3348 during moments of slowly changing supply voltages and low-voltage conditions is essential. This achieved by the addition of an internal power-on-reset and low-voltage detection circuit. To allow an external RESET signal being fed into the PCD3348, the reset pin (pin 17) has been configured as an input/output.

While a reset condition exist in the detection circuit, pin 17 is pulled HIGH by TR1 controlled by the reset circuit. When the reset condition is not present a pull-down current source (TR2) will be activated. TR2 forces pin 17 LOW thus removing the RESET signal from the microcontroller. Since the level at pin 17 is recognized by the microcontroller, the reset time constant can be stretched by connecting an external capacitor between V_{DD} and pin 17 (see Fig.22). The signal at pin 17 can also be used as an output to reset other devices in the system.

The internal reset circuit monitors the PCD3348 supply voltage. If the voltage drops below the switching level (typ. 1.3 V), a reset is removed (pin 17 goes LOW), after a fixed delay (t_d), when the supply voltage rises above the switching level again. The delay ensures a complete reset even when the supply voltage quickly rises above switching level after initial switch-on. During a low-voltage condition the oscillator is inhibited to prevent complete discharge of a weak battery. The timing of the power-on-reset and low-voltage detection circuit is shown in Fig.21.

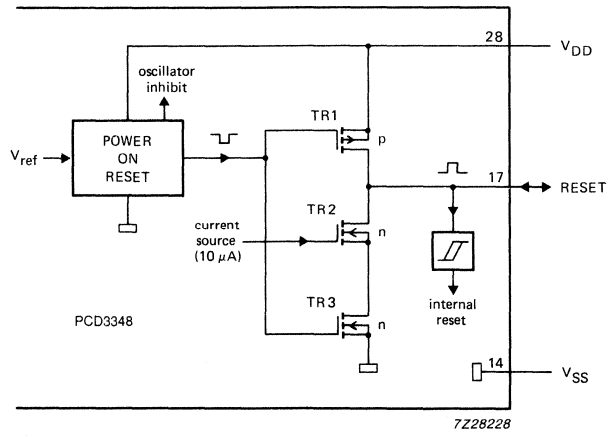
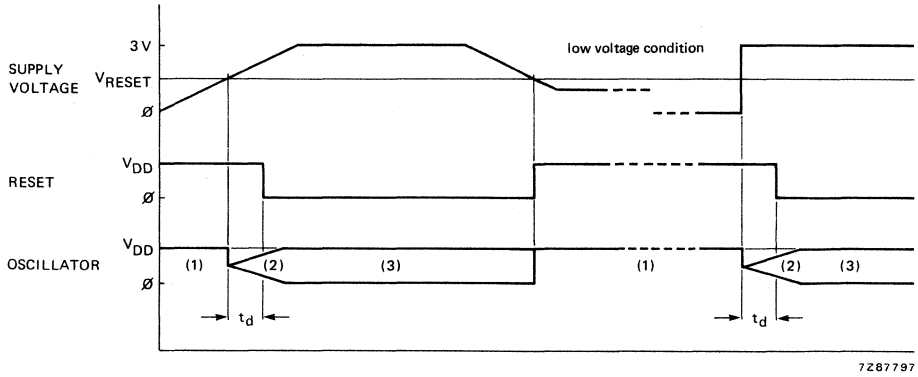


Fig.20 Power-on-reset configuration.



Notes to Fig.21.

(1) Oscillator inhibited
(2) Oscillator starting
(3) Oscillator running, but may be stopped with a STOP condition

Fig.21 Timing of power-on-reset and low-voltage detection.

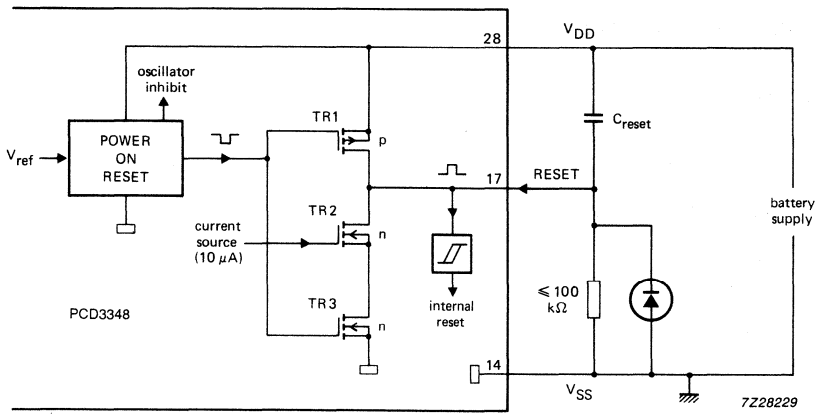


Fig.22 Stretched power-on-reset with external capacitor.

INSTRUCTION SET

The PCD3348 instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for serial I/O operation and memory bank selection. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 8 gives the instruction set of the PCD3348. Table 7 shows the instruction map and Table 6 details the symbols and definition descriptions that are used.

Table 6 Symbols and definition used in Table 8.

SYMBOL	DEFINITION DESCRIPTION
A	accumulator
ADDR	program memory address
Bb	bit designation (b = 0 to 7)
C	carry bit (bit CY)
CNT	event counter
D	mnemonic for 4-bit digit (nibble)
data	8-bit number or expression
I	interrupt
MBn	memory bank (n = 0 to 3)
MBFFn	memory bank flip-flop (n = 0 or 1)
P	mnemonic for 'in-page' operation
PC	Program Counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
RBS	register bank select
Rr	register designation (r = 0 to 7)
Sn	serial I/O register (n = 0, 1 or 2)
SP	Stack Pointer
T	timer
TF	Timer Flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addresses by X
←	is replaced by
↔	is exchanged with

Table 7 PCD3348 Instruction map.

first hexadecimal character of opcode ↓ | second hexadecimal character of opcode →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, #data	JMP page 0	EN I	JNTF addr	DEC A		IN A,Pp			MOV A,Sn			
									0	1	2		0	1		
1	INC @ Rr		JB0 addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr							
	0	1							0	1	2	3	4	5	6	7
2	XCH A, @Rr		STOP	MOV A, #data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A,Rr							
	0	1							0	1	2	3	4	5	6	7
3	XCHD A, @Rr		JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A				MOV Sn,A			
	0	1							0	1	2		0	1	2	
4	ORL A, @Rr		MOV A, T	ORL A, #data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr							
	0	1							0	1	2	3	4	5	6	7
5	ANL A, @Rr		JB2 addr	ANL A, #data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr							
	0	1							0	1	2	3	4	5	6	7
6	ADD A, @Rr		MOV T, A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr							
	0	1							0	1	2	3	4	5	6	7
7	ADDC A, @Rr		JB3 addr		CALL page 3			RR A	ADDC A,Rr							
	0	1							0	1	2	3	4	5	6	7
8				RET	JMP page 4	EN SI			ORL Pp,#data				MOV A,Dx	MOV Dx,A	ANL Dx,A	ORL Dx,A
									0	1	2					
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data				MOV Sn,#data			
									0	1	2		0	1	2	
A	MOV @ Rr,A			MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A							
	0	1							0	1	2	3	4	5	6	7
B	MOV @Rr, #data		JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data							
	0	1							0	1	2	3	4	5	6	7
C	DEC @Rr				JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr							
	0	1							0	1	2	3	4	5	6	7
D	XRL A, @Rr		JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr							
	0	1							0	1	2	3	4	5	6	7
E	DJNZ @ Rr,addr				JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr,addr							
	0	1							0	1	2	3	4	5	6	7
F	MOV A, @Rr		JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr							
	0	1							0	1	2	3	4	5	6	7

MBA281

Table 8 Instruction set.

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION		NOTES
ACCUMULATOR						
ADD A, Rr	6<8 + r>	1/1	Add register contents to A	(A) ← (A) + (Rr)	r = 0 to 7	1
ADD A, @Rr	6r	1/1	Add RAM data, addressed by Rr, to A	(A) ← (A) + ((Rr))	r = 0, 1	1
ADD A, #data	03 data	2/2	Add immediate data to A	(A) ← (A) + data		1
ADDC A, Rr	7<8 + r>	1/1	Add carry and register contents to A	(A) ← (A) + (Rr) + (C)	r = 0 to 7	1
ADDC A, @Rr	7r	1/1	Add carry and RAM data, addressed by Rr, to A	(A) ← (A) + ((Rr)) + (C)	r = 0, 1	1
ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A) ← (A) + data + (C)		1
ANL A, Rr	5<8 + r>	1/1	'AND' Rr with A	(A) ← (A) AND (Rr)	r = 0 to 7	
ANL A, @Rr	5r	1/1	'AND' RAM data, addressed by Rr, with A	(A) ← (A) AND ((Rr))	r = 0, 1	
ANL A, #data	53 data	2/2	'AND' immediate data with A	(A) ← (A) AND data		
ORL A, Rr	4<8 + r>	1/1	'OR' Rr with A	(A) ← (A) OR (Rr)	r = 0 to 7	
ORL A, @Rr	4r	1/1	'OR' RAM data, addressed by Rr, with A	(A) ← (A) OR ((Rr))	r = 0, 1	
ORL A, #data	43 data	2/2	'OR' immediate data with A	(A) ← (A) OR data		
XRL A, Rr	D<8 + r>	1/1	'XOR' Rr with A	(A) ← (A) XOR (Rr)	r = 0 to 7	
XRL A, @Rr	Dr	1/1	'XOR' RAM data, addressed by Rr, with A	(A) ← (A) XOR ((Rr))	r = 0, 1	
XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A) ← (A) XOR data		
INC A	17	1/1	Increment A by 1	(A) ← (A) + 1		
DEC A	07	1/1	Decrement A by 1	(A) ← (A) – 1		
CLR A	27	1/1	Clear A to zero	(A) ← 0		
CPL A	37	1/1	One's complement A	(A) ← NOT(A)		
RL A	E7	1/1	Rotate A left	$(A_{n+1}) \leftarrow (A_n)$ $(A_0) \leftarrow (A_7)$	n = 0 to 6	
RLC A	F7	1/1	Rotate A left through carry	$(A_{n+1}) \leftarrow A_n$ $(A_0) \leftarrow (C), (C) \leftarrow (A_7)$	n = 0 to 6	2
RR A	77	1/1	Rotate A right	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (A_0)$	n = 0 to 6	
RRC A	67	1/1	Rotate A right through carry	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (C), (C) \leftarrow (A_0)$	n = 0 to 6	2
DA A	57	1/1	Decimal adjust A	(A) ← (A) + 06H if AC = 1 or $(A_{0-3}) > 9$; (A) ← (A) + 60H if $(A_{4-7}) > 9$		2
SWAP A	47	1/1	Swap nibbles of A	$(A_{4-7}) \leftrightarrow (A_{0-3})$		2
DATA MOVES						
MOV A, Rr	F<8 + r>	1/1	Move register contents to A	(A) ← (Rr)	r = 0 to 7	
MOV A, @Rr	Fr	1/1	Move RAM data, addressed by Rr, to A	(A) ← ((Rr))	r = 0, 1	
MOV A, #data	23 data	2/2	Move immediate data to A	(A) ← data		
MOV Rr, A	A<8 + r>	1/1	Move accumulator contents to register	(Rr) ← (A)	r = 0 to 7	
MOV @Rr, A	Ar	1/1	Move accumulator contents to RAM location addressed by Rr	((Rr)) ← (A)	r = 0, 1	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION		NOTES
MOV Rr, #data	B<8 + r> data	2/2	Move immediate data to Rr	(Rr) ← data	r = 0 to 7	
MOV @Rr, #data	Br data	2/2	Move immediate data to RAM location addressed by Rr	((R0)) ← data	r = 0, 1	
XCH A, Rr	2<8 + r>	1/1	Exchange accumulator contents with Rr	(A) ↔ (Rr)	r = 0 to 7	
XCH A, @Rr	2r	1/1	Exchange accumulator contents with RAM data addressed by Rr	(A) ↔ ((Rr))	r = 0, 1	
XCHD A, @Rr	3r	1/1	Exchange lower nibbles of A and RAM data addressed by Rr	(A_{0-3}) ↔ ((Rr_{0-3}))	r = 0, 1	
MOV A, PSW	C7	1/1	Move PSW contents to accumulator	(A) ← (PSW)		
MOV PSW, A	D7	1/1	Move accumulator bit 3 to PSW_3 (PS)	(PS) ← (A_3)		3
MOVP A, @A	A3	1/2	Move indirectly addressed data in current page to A	(PC_{0-7}) ← (A), (A) ← ((PC))		
CARRY FLAG						
CLR C	97	1/1	Clear carry bit	(C) ← 0		2
CPL C	A7	1/1	Complement carry bit	(C) ← NOT(C)		2
REGISTER						
INC Rr	1<8 + r>	1/1	Increment register by 1	(Rr) ← (Rr) + 1	r = 0 to 7	
INC @Rr	1r	1/1	Increment RAM data, addressed by Rr, by 1	((Rr)) ← ((Rr)) + 1	r = 0, 1	
DEC Rr	C<8 + r>	1/1	Decrement register by 1	(Rr) ← (Rr) – 1	r = 0 to 7	
DEC @Rr	Cr	1/1	Decrement RAM data, addressed by Rr, by 1	((Rr)) ← ((Rr)) – 1	r = 0, 1	
BRANCH						
JMP addr	<2n>4 addr	2/2	Unconditional jump within a 2 K bank	(PC_{8-10}) ← n (PC_{0-7}) ← addr (PC_{11-12}) ← (MBFF 0-1)	n = 0 to 7	
JMPP @A	B3	1/2	Indirect jump within a page	(PC_{0-7}) ← ((A))		
DJNZ Rr, addr	E<8 + r> addr	2/2	Decrement Rr by 1 and jump if not zero to addr	(Rr) ← (Rr) – 1; if (Rr) not zero, then (PC_{0-7}) ← addr	r = 0 to 7	
DJNZ @Rr, addr	Er	2/2	Decrement RAM data, addressed by Rr, by 1 and jump if not zero to addr	((Rr)) ← ((Rr)) – 1; if ((Rr)) not zero, then (PC_{0-7}) ← addr	r = 0, 1	
JBb addr	<2b + 1>2 addr	2/2	Jump to addr if Accumulator bit b = 1	If (A_b) = 1, then (PC_{0-7}) ← addr	b = 0 to 7	
JC addr	F6 addr	2/2	Jump to addr if C = 1	If (C) = 1, then (PC_{0-7}) ← addr		
JNC addr	E6 addr	2/2	Jump to addr if C = 0	If (C) = 0, then (PC_{0-7}) ← addr		
JZ addr	C6 addr	2/2	Jump to addr if A = 0	If (A) = 0, then (PC_{0-7}) ← addr		
JNZ addr	96 addr	2/2	Jump to addr if A is NOT zero	If (A) ≠ 0, then (PC_{0-7}) ← addr		
JT0 addr	36 addr	2/2	Jump to addr if T0 = 1	If T0 = 1, then (PC_{0-7}) ← addr		
JNT0 addr	26 addr	2/2	Jump to addr if T0 = 0	If T0 = 0: (PC_{0-7}) ← addr		

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
JT1 addr	56 addr	2/2	Jump to addr if T1 = 1	If T1 = 1: (PC_{0-7}) ← addr	
JNT1 addr	46 addr	2/2	Jump to addr if T1 = 0	If T1 = 0: (PC_{0-7}) ← addr	
JTF addr	16 addr	2/2	Jump to addr if Timer Flag = 1	If TF = 1: (PC_{0-7}) ← addr	4
JNTF addr	06 addr	2/2	Jump to addr if Timer Flag = 0	If TF = 0: (PC_{0-7}) ← addr	4
TIMER/EVENT COUNTER					
MOV A, T	42	1/1	Move timer/event counter contents to accumulator	(A) ← (T)	
MOV T, A	62	1/1	Move accumulator contents to timer/event counter	(T) ← (A)	
STRT CNT	45	1/1	Start event counter		
STRT T	55	1/1	Start timer		
STOP TCNT	65	1/1	Stop timer/event counter		
EN TCNTI	25	1/1	Enable timer/event counter interrupt		
DIS TCNTI	35	1/1	Disable timer/event counter interrupt		
CONTROL					
EN I	05	1/1	Enable external (chip enable) interrupt		
DIS I	15	1/1	Disable external (chip enable) interrupt		
SEL RB0	C5	1/1	Select register bank 0	(RBS) ← 0	5
SEL RB1	D5	1/1	Select register bank 1	(RBS) ← 1	5
SEL MB0	E5	1/1	Select program memory bank 0	(MBFF0) ← 0, (MBFF1) ← 0	10
SEL MB1	F5	1/1	Select program memory bank 1	(MBFF0) ← 1, (MBFF1) ← 0	10
SEL MB2	A5	1/1	Select program memory bank 2	(MBFF0) ← 0, (MBFF1) ← 1	10
SEL MB3	B5	1/1	Select program memory bank 3	(MBFF0) ← 1, (MBFF1) ← 1	10
STOP	22	1/1	Enter Stop mode		
IDLE	01	1/1	Enter Idle mode		
SUBROUTINE					
CALL addr	<2n + 1>4 addr	2/2	Jump to subroutine	((SP)) ← (PC), n = 0 to 7 ($PSW_{4, 6, 7}$) (SP) ← (SP) + 1 (PC_{8-10}) ← n (PC_{0-7}) ← addr (PC_{11-12}) ← (MBFF0-1)	6
RET	83	1/2	Return from subroutine	(SP) ← (SP) - 1 (PC) ← ((SP))	6
RETR	93	1/2	Return from interrupt and restore bits 4, 6, 7 of PSW	(SP) ← (SP) - 1 ($PSW_{4, 6, 7}$) + (PC) ← ((SP))	6

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION		NOTES
PARALLEL INPUT/OUTPUT						
IN A, Pp	08	1/2	Input port p data to accumulator	(A) ← (P0)		
	09			(A) ← (P1)		
	0A			(A) ← (P2)		7
OUTL Pp, A	38	1/2	Output accumulator data to port p	(P0) ← (A)		
	39			(P1) ← (A)		
	3A			(P2) ← (A)		
ANL Pp, #data	98 data	2/2	AND port p with immediate data	(P0) ← (P0) AND data		
	99 data			(P1) ← (P1) AND data		
	9A data			(P2) ← (P2) AND data		
ORL Pp, #data	88 data	2/2	OR port p data with immediate data	(P0) ← (P0) OR data		
	89 data			(P1) ← (P1) OR data		
	8A data			(P2) ← (P2) OR data		
SERIAL INPUT/OUTPUT						
MOV A, S_n	0C	1/2	Move serial I/O register contents to accumulator	(A) ← (S0)	n = 0, 1	8
	0D			(A) ← (S1)		
MOV S_n, A	3C	1/2	Move accumulator contents to serial I/O register	(S0) ← (A)	n = 0, 1, 2	9
	3D			(S1) ← (A)		
	3E			(S2) ← (A)		
MOV S_n, #data	9C data	2/2	Move immediate data to serial I/O register	(S0) ← data	n = 0, 1, 2	
	9D data			(S1) ← data		
	9E data			(S2) ← data		
EN SI	85	1/1	Enable serial I/O interrupt			
DIS SI	95	1/1	Disable serial I/O interrupt			
NOP	00	1/1	No operation	(PC_{0-10}) ← (PC_{0-10}) + 1		

Notes

1. PSW CY, AC affected.
2. PSW CY affected.
3. PSW PS affected.
4. Execution of a JTF or JNTF instruction resets the Timer Flag (TF).
5. PSW RBS affected.
6. PSW SP_0, SP_1, SP_2 affected.
7. (A) = 1111, P23, P22, P21, P20
8. (S1) has a different meaning for read and write operations. See section 4.11.4.
9. (S2) is a write only register. Reading S2 will give value FFH.
10. SEL MB instructions may not be used within interrupt routines.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+ 8	V
V_I	all input voltages	0.8	V_{DD} + 0.8	V
$\pm I_I$, $\pm I_O$	DC current into any input or output	-	10	mA
P_{tot}	total power dissipation	-	500	mW
P_O	power dissipation per output except P23, SCLK	-	50	mW
P_O	power dissipation per output P23, SCLK	-	180	mW
T_{stg}	storage temperature range	-65	+ 150	°C
T_{amb}	operating ambient temperature range	-25	+ 70	°C
Tj	operating junction temperature	-	+ 125	°C

THERMAL RESISTANCE

SYMBOL	PACKAGE	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}a}$	SOT117	junction to ambient	120	K/W
$R_{th\ j\text{-}a}$	SOT136A	junction to ambient	150	K/W

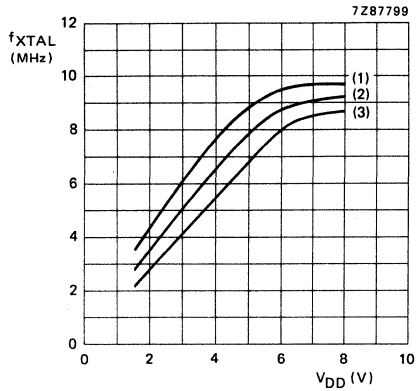
DC CHARACTERISTICS

V_{DD} = 2.75 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3.58 MHz with R_S = 50; unless otherwise specified. See Figures 23 to 26.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage operating		1.8	-	6	V
V_{DD}	STOP mode for RAM retention		1.0	-	6	V
I_{DD}	supply current operating	V_{DD} = 3 V	-	600	-	µA
I_{DD}	IDLE mode	V_{DD} = 3 V	-	300	-	µA
I_{DD}	STOP mode (see note 1)	V_{DD} = 1.8 V; T_{amb} = 25 °C	-	1.2	2.5	µA
I_{DD}	STOP mode (see note 1)	V_{DD} = 1.8 V; T_{amb} = 55 °C	-	-	5	µA
I_{DD}	STOP mode (see note 1)	V_{DD} = 1.8 V; T_{amb} = 70 °C	-	-	10	µA
RESET I/O						
V_{RESET}	switching level		-	1.3	-	V
I_{OL}	sink current	$V_{DD} > V_{RESET}$	-	7	-	µA
Inputs						
V_{IL}	input voltage LOW		0	-	0.3 V_{DD}	V
V_{IH}	input voltage HIGH		0.7 V_{DD}	-	V_{DD}	V
$\pm I_L$	input leakage current	$V_{SS} < V_I < V_{DD}$	-	-	1	µA
Outputs						
V_{OL}	output voltage LOW	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert$ < 1 µA	-	-	0.05	V
I_{OL}	output sink current LOW except P23/SDA,SCLK	V_{DD} = 3 V; V_O = 0.4 V	0.75	1.5	-	mA
I_{OL}	output sink current LOW P23/SDA, SCLK		1.5	-	-	mA
$-I_{OH}$	pull-up output source current HIGH	V_{DD} = 3 V; V_O = 0.9 V_{DD};	25	-	-	µA
$-I_{OH}$	pull-up output source current HIGH	V_{DD} = 3 V; V_O = V_{SS};	-	-	200	µA
$-I_{OH}$	push-pull output source current HIGH	V_{DD} = 3 V; V_O = V_{DD} −0.4 V	0.75	1.5	-	mA

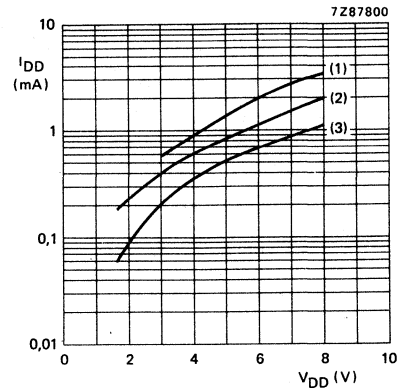
Note to the DC characteristics

1. Crystal connected between XTAL1 and XTAL2; SCL and SDA pulled to V_{DD} via 5.6 Ω resistor; CE and T1 as V_{SS}.



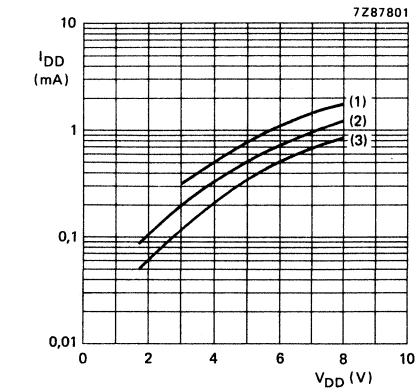
(1) T_{amb} = –25 °C
(2) T_{amb} = + 25 °C
(3) T_{amb} = + 70 °C

Fig.23 Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (V_{DD}).



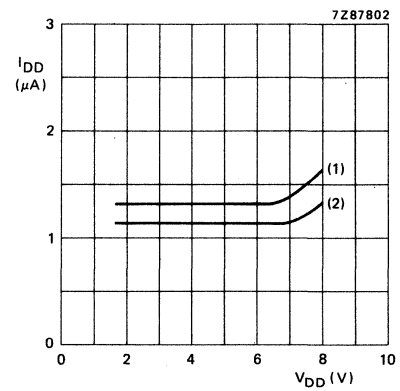
(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

Fig.24 Typical supply current (I_{DD}) in operating mode as a function of the supply voltage (V_{DD}); T_{amb} = + 25 °C.



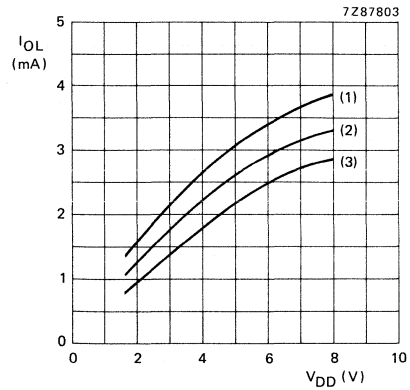
(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

Fig.25 Typical supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}); T_{amb} = + 25 °C.



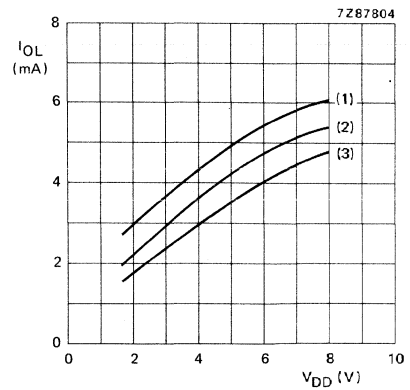
(1) T_{amb} = + 70 °C
(2) T_{amb} = + 25 °C

Fig.26 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).



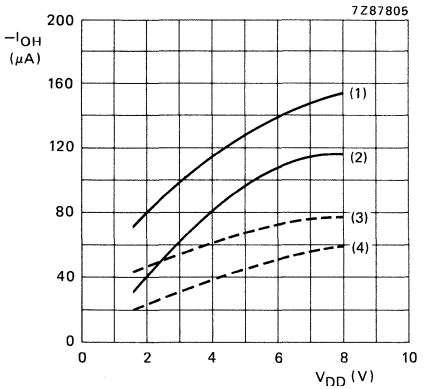
(1) T_{amb} = −25 °C
(2) T_{amb} = + 25 °C
(3) T_{amb} = + 70 °C

Fig.27 Output sink current LOW (I_{OL}), except outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); V_O = 0.4 V.



(1) T_{amb} = −25 °C
(2) T_{amb} = + 25 °C
(3) T_{amb} = + 70 °C

Fig.28 Output current LOW (I_{OL}), outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); V_O = 0.4 V.



(1) T_{amb} = + 25 °C; $V_O = V_{SS}$
(2) T_{amb} = + 25 °C; V_O = 0.9 V_{DD}
(3) T_{amb} = + 70 °C; $V_O = V_{SS}$
(4) T_{amb} = + 70 °C; V_O = 0.9 V_{DD}

Fig.29 Output source current HIGH ($-I_{OH}$) as a function of supply voltage (V_{DD})

AC CHARACTERISTICS

Maximum rise and fall times between 10 and 90% levels;
C_L = 50 pF; T_{amb} = + 70 °C.

SYMBOL	PARAMETER	SUPPLY VOLTAGE (VDD)			UNIT
		1.8	3.0	6.0	
t_f	fall time	200	100	70	ns
t_r	rise time	200	100	80	ns

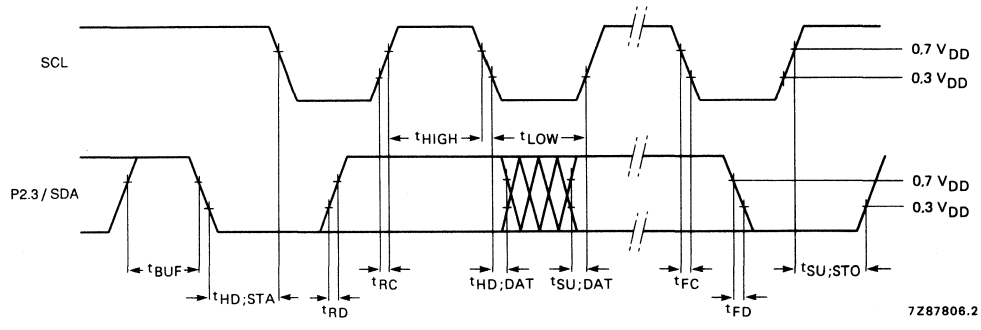


Fig.30 PCD3348 timing requirements for the P23 and SCLK input signals.

Table 9 Input timing shown in Fig.30.

SYMBOL	TIMING
t_{BUF}	≥ $14t_{XTAL}$
$t_{HD;STA}$	≥ $14t_{XTAL}$
t_{HIGH}	≥ $17t_{XTAL}$
t_{LOW}	≥ $17t_{XTAL}$
$t_{SY;STO}$	≥ $14t_{XTAL}$
$t_{HD;DAT}$	< 0
$t_{SU;DAT}$	≥ 250 ns
t_{RD}	≤ 1 µs
t_{RC}	≤ 1 µs
t_{FD}	≤ 1 µs
t_{FC}	≤ 0.3 µs

Notes to Table 9

1. t_{XTAL} = one period of the XTAL input frequency (f_{XTAL}).
   For f_{XTAL} = 3.58 MHz; t_{XTAL} = 280 ns.
2. These figures apply to all modes.

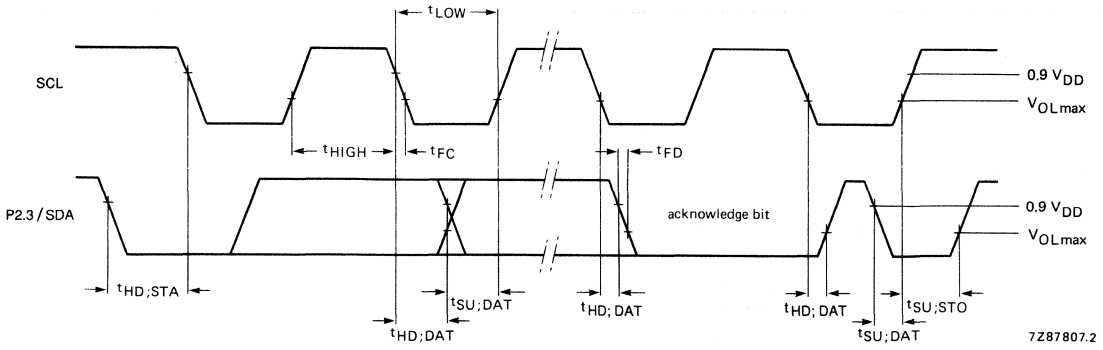


Fig.31 PCD3348 timing requirements for the P23 and SCLK output signals.

Table 10 Output timing shown in Fig.31.

SYMBOL	TIMING	
	NORMAL MODE (ASC in S2 = 0)	**LOW-SPEED MODE (ASC in S2 = 1)**
$t_{HD;STA}$	$1/2(DF + 9)t_{XTAL}$	$3/4(DF + 9)t_{XTAL}$
t_{HIGH}	$1/2(DF)t_{XTAL}$	$3/4\ (DF)t_{XTAL}$
t_{LOW}	$1/2(DF)t_{XTAL}$	$1/4(DF)t_{XTAL}$
$t_{SU;STO}$	$1/2(DF \circledR 3)t_{XTAL}$	$1/4(DF \circledR 3)t_{XTAL}$
$t_{HD;DAT}$ (slave transmitter) any DF	 $\geq 9t_{XTAL}$ $\leq 12t_{XTAL}$	 $\geq 9t_{XTAL}$ $\leq 12t_{XTAL}$
$t_{HD;DAT}$ for DF ≤ 51 for DF ≤ 99	$\geq 9t_{XTAL}$ $\leq 12t_{XTAL}$ - -	- - $\geq 9t_{XTAL}$ $\leq 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter) for DF > 51 for DF > 99 for DF ≤ 51 for DF ≤ 99	 $\geq 15t_{XTAL}$ $\leq 24t_{XTAL}$ - $\geq 9t_{XTAL}$ -	 - - $\geq 15t_{XTAL}$ $\leq 24t_{XTAL}$ $\geq 9t_{XTAL}$
t_{AC}	$\geq 9t_{XTAL}$ $\leq 12t_{XTAL}$	$\geq 9t_{XTAL}$ $\leq 12t_{XTAL}$
t_{FD}, t_{FC}	≤ 100 ns at C_b = 400 pF	≤ 100 ns at C_b = 400 pF

Notes to Table 10

1. t_{XTAL} = one period of the XTAL input frequency (f_{XTAL}).
   For f_{XTAL} = 3.58 MHz; t_{XTAL} = 280 ns.
2. DF = divisor (see Table 2 Serial I/O section).
3. C_b = the maximum bus capacitance for each line.

APPLICATION INFORMATION

A block diagram of an electronic featurephone built around the PCD3348 is shown in Fig.32. It comprises the following dedicated telephony ICs:

TEA1060/1061	transmission circuit for telephony
PCD3312C	DTMF generator with Serial I/O
PCE2111 or	2 LCD drivers in LCD module
PCF8577	MB7020160
PCD8571	1 K RAM's with Serial I/O; the number of RAM's depend on the required amount of stored telephone numbers
PCD3360	programmable multi-tone ringer

A detailed application diagram of the PCD3348 with PCD3312C (DTMF), two PCD8571 (RAM) and two PCE2211 (LCD display drivers) is shown in Fig.33.

Row 5 of the keyboard contains the following special keys:

- P program and autodial
- FL flash or register recall
- R redial or extended redial
- AP access pause

Row 6 contains the different diode options.

Columns 5 and 6 contain the button keys M0 to M9; single name keys for repertory telephone numbers.

Additional information is available on request for the following:

- Serial I/O
- I^2C-bus specification
- Interrupt logic
- Instruction set descriptions
- Software routines for an intelligent telephone set.

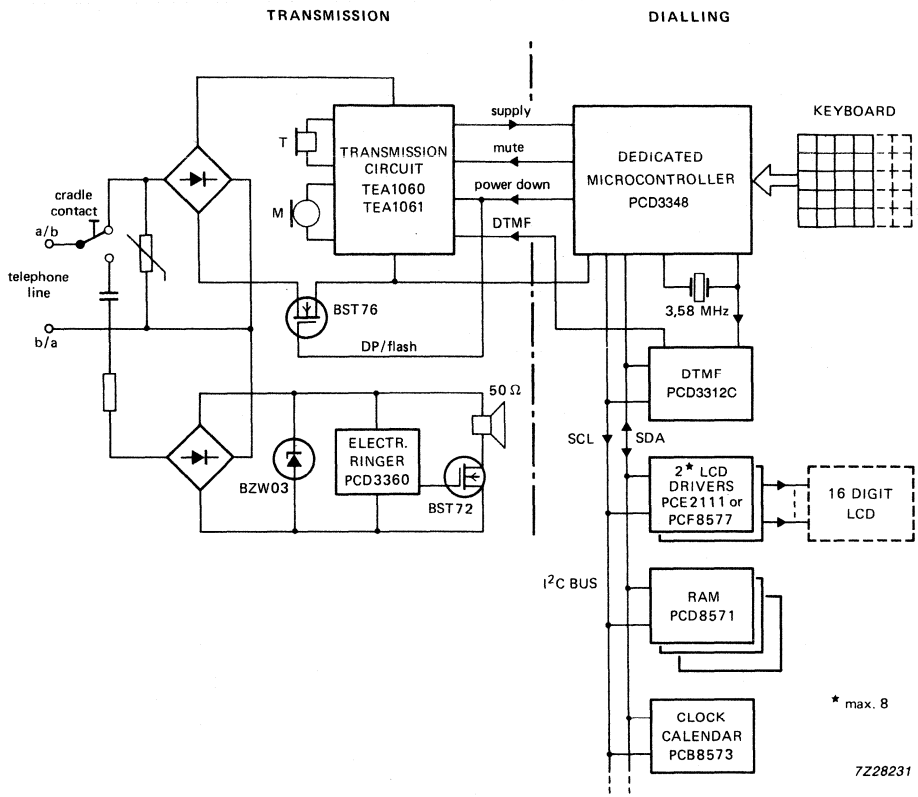


Fig.32 Block diagram of electronic featurephone with common line interface.

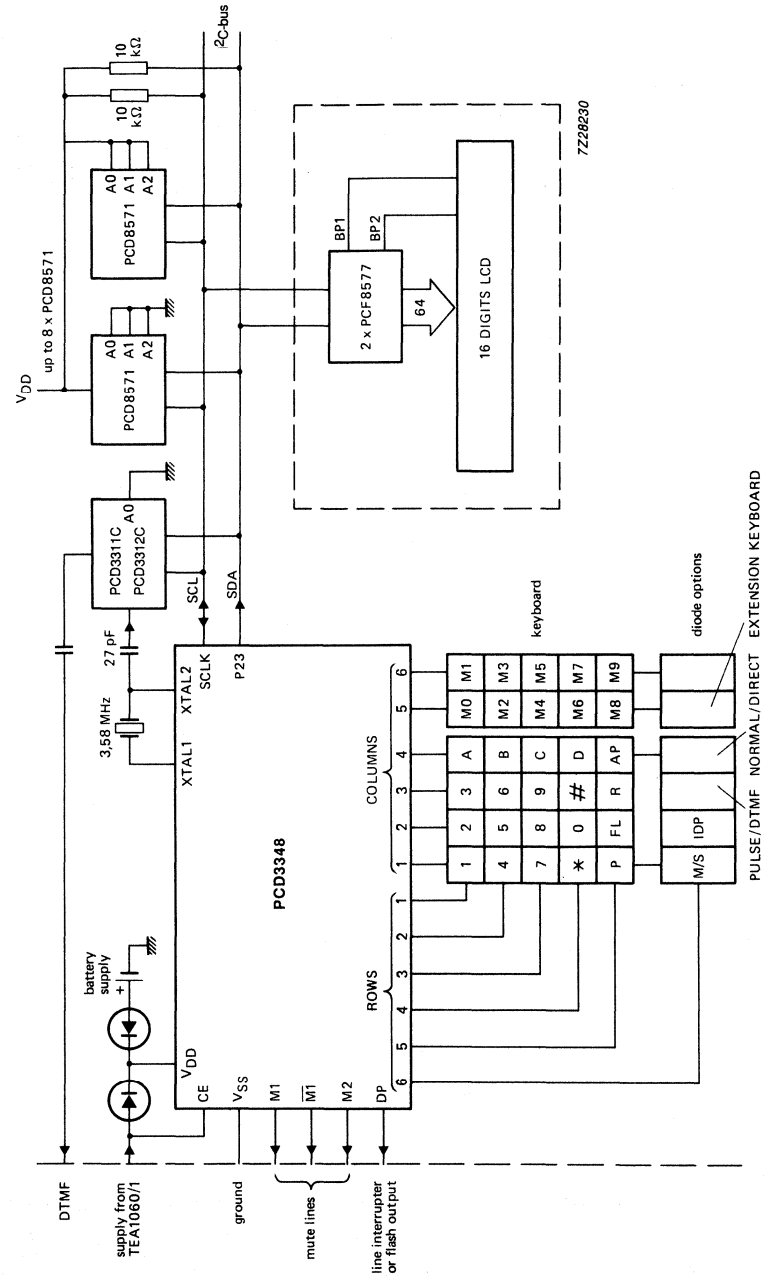


Fig.33 Application diagram of PCD3348 for electronic featurephone with associated keyboard.

CMOS MICROCONTROLLER WITH ON-CHIP DTMF GENERATOR

GENERAL DESCRIPTION

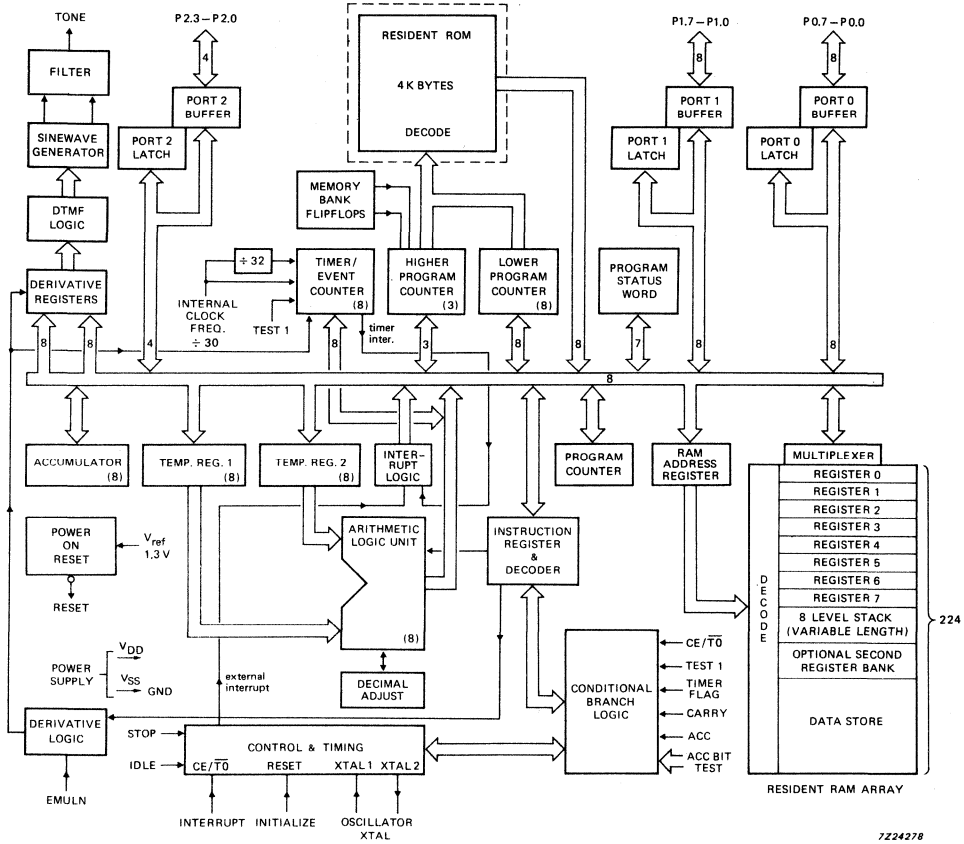
The PCD3349 is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD33XX family. It has an on-chip dual tone multi-frequency (DTMF) generator and other features for application in telephone sets. For further detailed information, see PCD33XX family specifications.

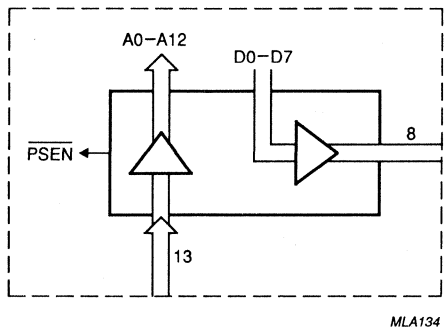
Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 4096 ROM bytes
- 224 RAM bytes
- On-chip DTMF tone generator
- On-chip voltage reference for supply and temperature-independent tone output
- On-chip filtering for low output distortion (CEPT CS203 compatible)
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles
- Clock frequency 3.58 MHz
- Single supply voltage from 2.5 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3349P: 28-lead DIL; plastic (SOT117).
PCD3349T: 28-lead mini-pack; plastic (SO28; SOT136A).





(a)

Fig. 1. PCD3349 block diagram: the function in the dotted outline is replaced as shown in (a) for the PCD3344B 'piggy-back' version.

DEVELOPMENT DATA

PINNING (for normal operation)

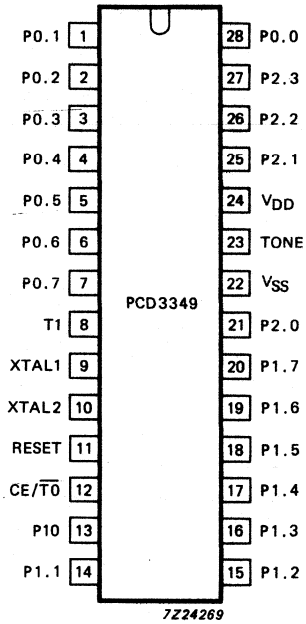


Fig. 2 Pinning diagram.

PIN DESIGNATION

28, 1-7	P0.0-P0.7	Port 0: 8-bit quasi-bidirectional I/O port.
8	T1	Test 1: test input, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter using the STRT CNT instruction.
9	XTAL1	Crystal input: connection to the timing component (crystal) which determines the frequency of the internal oscillator; is also the input for an external clock source.
10	XTAL2	Connection to other side of timing component.
11	RESET	Reset input (active HIGH): used to initialize the processor or output of the power-on-reset circuit.
12	CE/$\overline{T0}$	Interrupt/Test 0: external interrupt input (sensitive to positive-going edge)/test input pin. When used as a test input is directly tested by conditional branch instructions JT0 and JNT0.
13-20	P1.0-P1.7	Port 1: 8-bit quasi-bidirectional I/O port.
21, 25-27	P2.0-P2.3	Port 2: 4-bit quasi-bidirectional I/O port.
22	V_{SS}	Ground: circuit earth potentional.
23	TONE	Tone output: single or dual tone frequency output with on-chip filtering for low output distortion (CEPT CS203 compatible). This generator is controlled via the internal processor bus.
24	V_{DD}	Power supply: 2.5 to 6 V.

FUNCTIONAL DESCRIPTION

Program memory PCD3349

The program memory comprises 4096 bytes (8-bit words) in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 3 shows the program memory map.

Three program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine,
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

The program memory is divided into location 'pages', each of 256 bytes. This division applies only for conditional branches. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory PCD3349

Data memory consists of 224 bytes (8-bit words) of random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 4 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently-addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 5) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with next generated return address.

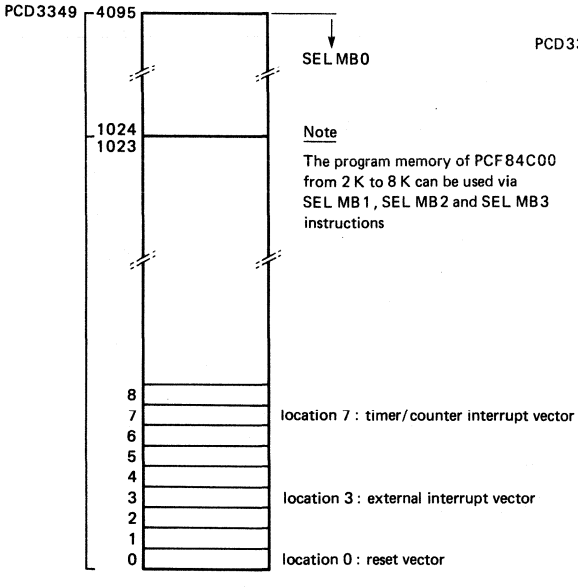


Fig. 3 Program memory map.

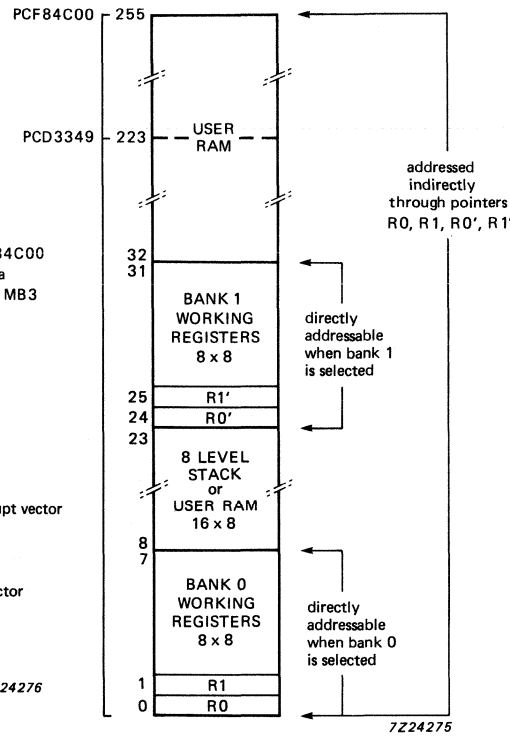


Fig. 4 Data memory map.

DEVELOPMENT DATA

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations. Possible locations from 32 to 223 may be used for storage of program variables or data.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

FUNCTIONAL DESCRIPTION (continued)

Program counter stack (continued)

stack pointer									
1 1 1	----------								R23/22
1 1 0	----------								R21/20
1 0 1	----------								R19/18
1 0 0	----------								R17/16
0 1 1	----------								R15/14
0 1 0	----------								R13/12
0 0 1	----------								R11/10
0 0 0	PSW7	PSW6	PC12	PSW4	PC11	PC10	PC9	PC8	R9
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	R8

Fig. 5 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (H'01') the oscillator and timer/counter are kept running. The microcontroller exits from the IDLE mode by one of two interrupts if they are enabled or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 6).

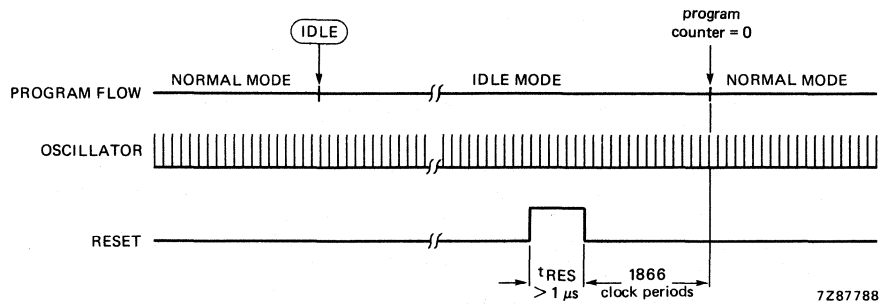


Fig. 6 Exit from IDLE mode via a RESET.

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A LOW-to-HIGH transition on the external interrupt pin (CE/$\overline{T0}$) reactivates the microcontroller. A HIGH level applied to CE/$\overline{T0}$ will reactivate the microcontroller only in the STOP mode. Thus, if CE/$\overline{T0}$ was HIGH before the microcontroller entered the IDLE mode, it must go LOW before the microcontroller can be reactivated (see Fig. 7).

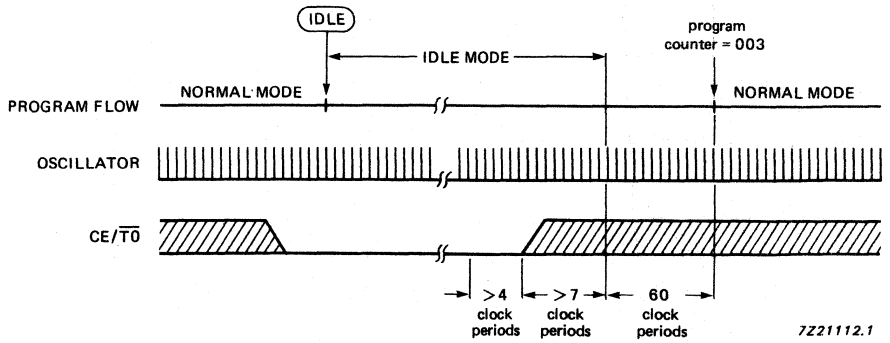


Fig. 7 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when CE/$\overline{T0}$ is LOW for 4 CP (clock periods) followed by a HIGH for 7 CP. After the initial forced CALL H'003' operation (60 CP) the program continues with the external interrupt service routine.

STOP mode

The microcontroller enters the STOP mode by the STOP instruction (H'22'). The oscillator is switched off. The internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 8).

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin HIGH, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a HIGH level applied at the CE/$\overline{T0}$ pin, and not by a LOW-to-HIGH transition as in a normal interrupt mechanism.

When the CE/$\overline{T0}$ level is active during the STOP instruction then no STOP is executed.

A HIGH level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

STOP mode (continued)

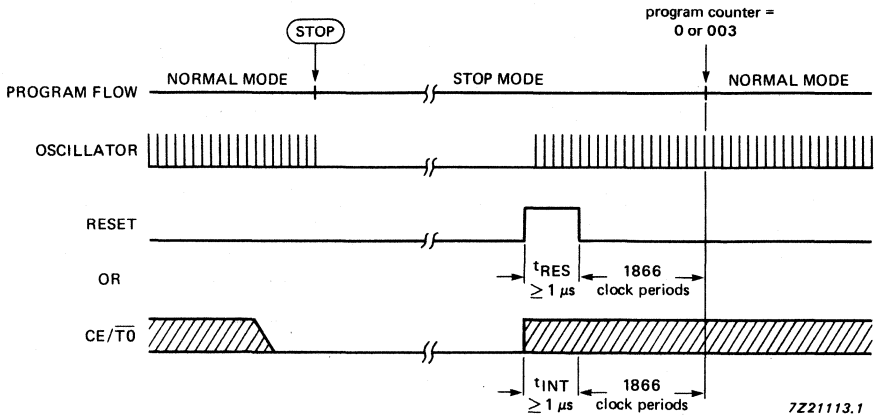


Fig. 8 Entering and exiting the STOP mode.

Tone output (DTMF mode)

Control of the sinewave generator

The on-chip sinewave oscillator is controlled by the 'derivative' registers Dx (x = H'0' to 'FF'). The instruction that controls the derivative registers is shown in Table 1.

Table 1 Derivative register control

mnemonic	opcode	description	function
MOV Dx,A	8D Dx	move accumulator contents to derivative register	(Dx) ← (A)

The instruction is 2 cycles/2 bytes. The second byte selects the derivative register to be addressed (H'0' to 'FF'). Register H'01' is for control of HIGH group frequencies, and register H'02' for control of LOW group frequencies. Thus data transport from accumulator to derivative register D01 is done by the 2-byte opcode 8D,01.

Generation of frequencies

The single and dual tones at the tone output are filtered by an on-chip switched-capacitor filter followed by an on-chip active RC low-pass filter. These ensure that the total harmonic distortion of the DTMF tones fulfil the CEPT CS 203 recommendations. An on-chip reference voltage provides output tone levels that are independent of the supply voltage.

The output frequency can be calculated as follows:

$$f_{out} = \frac{f_{XTAL}}{23\,(x + 2)}\ \text{Hz}$$

x = 60 to 255 and is the decimal value of the appropriate ROM-code (see Table 2)

Table 2 ROM-codes for DTMF applications

telephone keyboard symbol	contents of low register (hex)	contents of high register (hex)
0	A3	72
1	DD	7F
2	DD	72
3	DD	67
4	C8	7F
5	C8	72
6	C8	67
7	B5	7F
8	B5	72
9	B5	67
A	DD	5D
B	C8	5D
C	B5	5D
D	A3	5D
*	A3	7F
#	A3	67

DTMF generation is stopped by loading H'00' into both derivative registers.

I/O facilities

The PCD3349 family has 22 I/O lines arranged as:

- Port 0 parallel port of 8 lines (P0.0 to P0.7)
- Port 1 parallel port of 8 lines (P1.0 to P1.7)
- Port 2 parallel port of 4 lines (P2.0 to P2.3)
- CE/$\overline{T0}$ external interrupt and test input. When used as a test input it can be directly tested by conditional branch instructions JT0 and JNT0
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional. Output data written to a port is latched and remains unchanged until rewritten. Input data is not latched and so must be present until read by an input instruction.

Input lines are fully CMOS compatible, output lines can drive one LS-TTL or CMOS load.

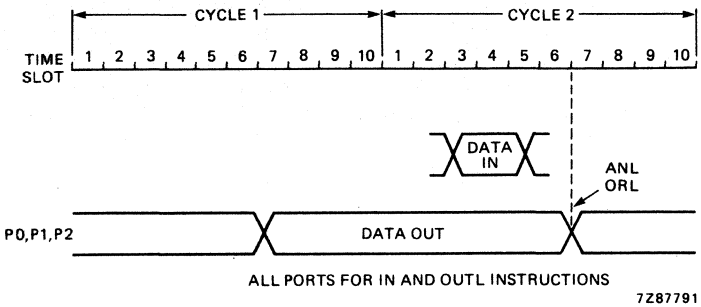


Fig. 9 Timing diagram of all ports on IN and OUTL instructions; for ANL and ORL instructions, the ports change on the time slot 7 of cycle 2.

Fig. 10 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source. Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current source provides sufficient current for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period) to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

In telephone applications this switched pull-up source may not be sufficient. Therefore the PCD3349 offers the possibility to select individually the 20 parallel port pins by the following mask options:

Option 1 –STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2 (1.5 mA). TR2 is active only during 1 clock cycle (0.28 μs at 3.58 MHz).

Option 2 –OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 11).

Option 3 –PUSH-PULL OUTPUT; drive capability of the output will be 1.5 mA (typ.) at V_{DD} = 3 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must be used only as outputs (Fig. 12).

Also, individual mask selection of the RESET state of these port pins can be achieved by appending the following options S and R to options 1, 2 or 3.

Option S-SET; after RESET this pin will be initialized to HIGH.

Option R-RESET; after RESET this pin will be initialized to LOW.

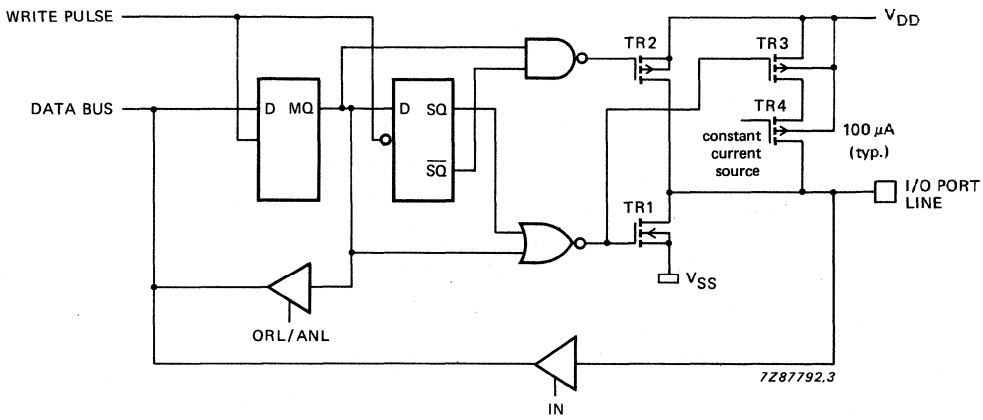


Fig. 10 Standard output with switched pull-up current source.

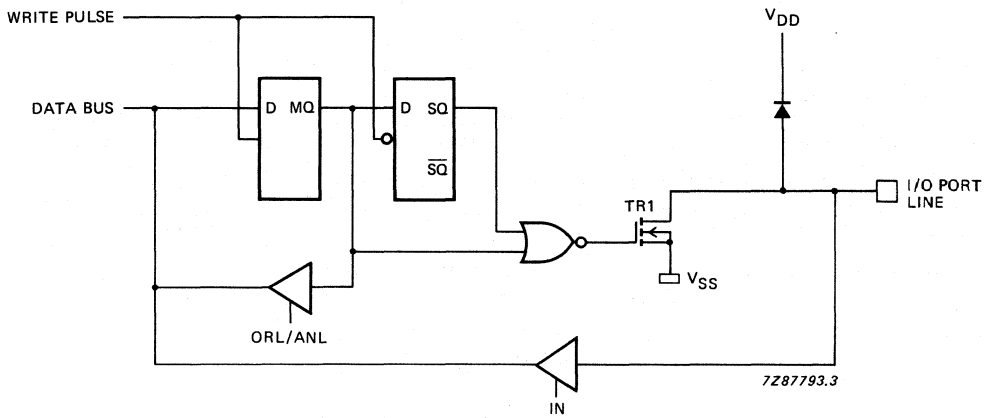


Fig. 11 Open drain output.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Parallel ports (continued)

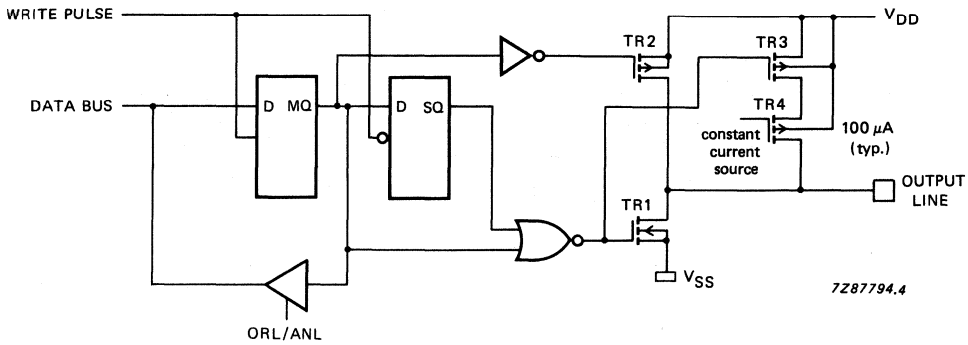


Fig. 12 Push-pull output.

Interrupts (see Fig. 13(a) and Fig. 13(b))

When an interrupt routine is entered, the contents of the program counter and bits 4, 6 and 7 of the PSW are saved in the program counter stack. The contents of the accumulator can only be saved by user software. Interrupt acknowledgement can be carried out by software via I/O ports. All interrupt routines must reside in memory bank 0; the SEL MB1, SEL MB2 and SEL MB3 instructions may not be used in an interrupt routine. An interrupt routine can only be terminated by the RETR (return and restore) instruction. During an interrupt routine, subroutine calls must be terminated by the RET instruction. Using the RETR instruction to terminate a subroutine called in an interrupt routine would terminate the interrupt routine prematurely and result in a wrong return address.

1. **External interrupt**

When the external interrupt is enabled, a LOW-to-HIGH transition on the CE/$\overline{TO}$ input initiates an external interrupt routine which forces a call to program memory location 3. The program counter points to the external interrupt vector address (003 H) between 2.6 and 3.6 machine cycles after the transition occurs. Interrupt latency depends on the instruction that is being executed when the transition occurs. External interrupts are latched in the External Interrupt Flag (EIF) even when they are not enabled. Execution of a DIS I instruction clears previously latched interrupts, the digital filter latch and the external interrupt flag.

2. **Timer/counter interrupt**

When the timer interrupt is enabled, a timer/counter overflow sets the Timer Interrupt Flag (TIF) and forces a CALL to location 7. The timer interrupts are only latched when they are enabled. The timer flag is set every time the timer/counter overflows and is not automatically reset when the timer/counter interrupt routine is called. It can only be cleared by the JTF and JNTF instructions or by a hardware RESET.

3. Simultaneous interrupts

If simultaneous interrupts occur their priority is as follows:

external (highest);
timer/counter (lowest).

An interrupt routine can only be interrupted by a hardware RESET and cannot be interrupted by other interrupts (which will be latched if enabled). When the interrupt routine is terminated by the RETR instruction, at least one instruction of the main program will be executed before another interrupt routine is entered.

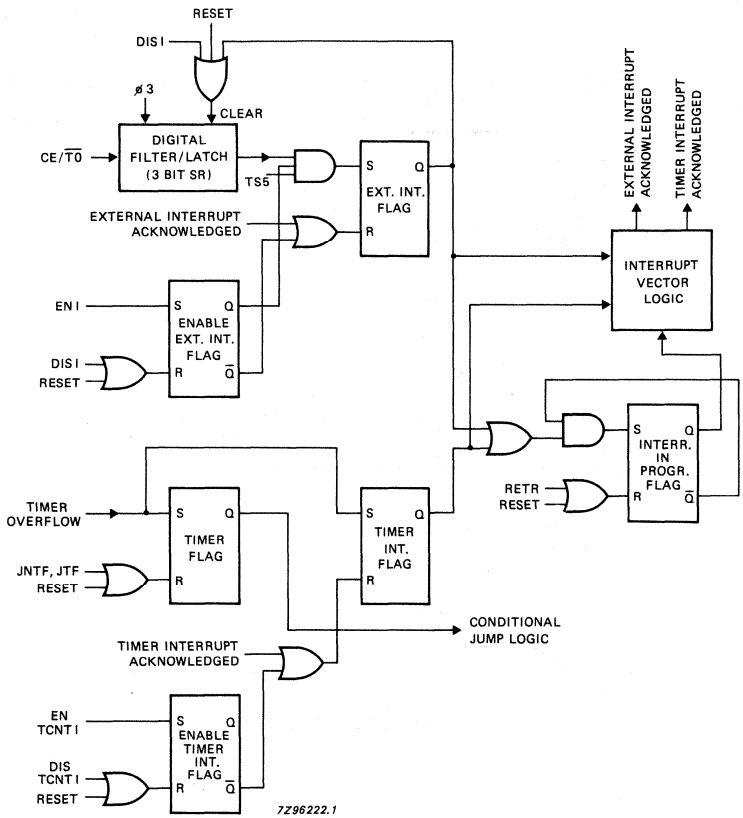


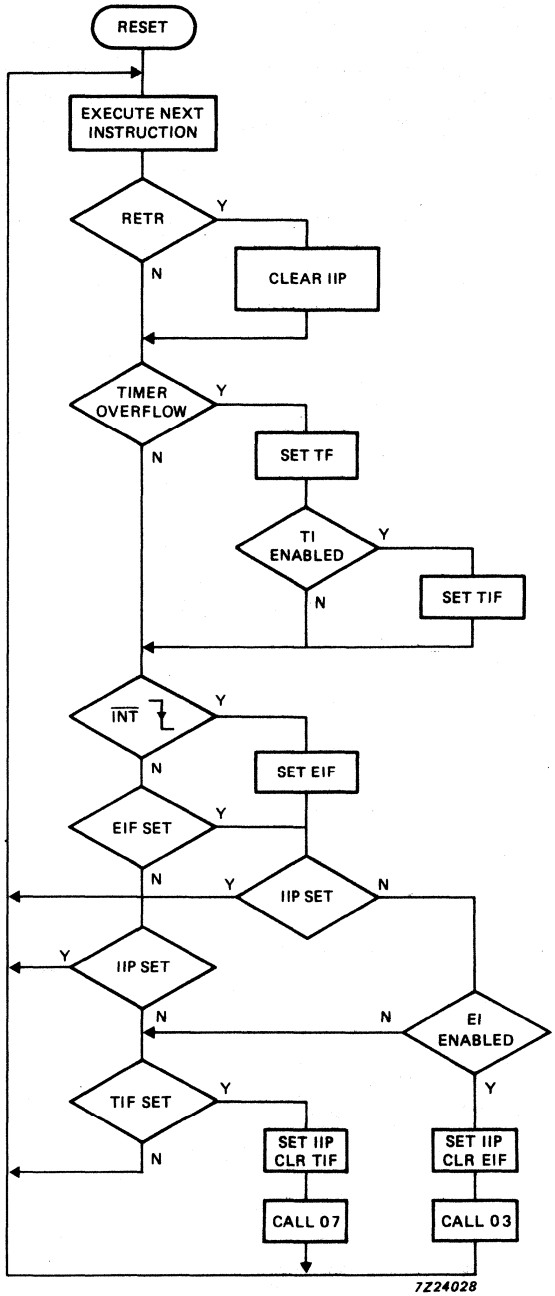
Fig. 13(a) Interrupt logic.

Notes to figure 13(a)

1. CE/$\overline{T0}$ positive edge is always latched in the digital filter/latch.
2. Correct interrupt timing is ensured when CE/$\overline{T0}$ is LOW for $>$ 4 CP followed by a HIGH for $>$ 7 CP.
3. When the interrupt in progress flag is set, further interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.
5. For all flip-flops, RESET overrules SET.

FUNCTIONAL DESCRIPTION (continued)

Interrupts (continued)



EI	External Interrupt
TI	Timer/counter Interrupt
EIF	External Interrupt Flag
TF	Timer Flag
IIP	Interrupt In Progress flag

Fig. 13(b) Interrupt flowchart.

Oscillator (see Fig. 14)

The 3.58 MHz oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-voltage condition is present to prevent discharge of a weak back-up battery.

Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a HIGH level at either the CE/$\overline{T0}$ or RESET pin.

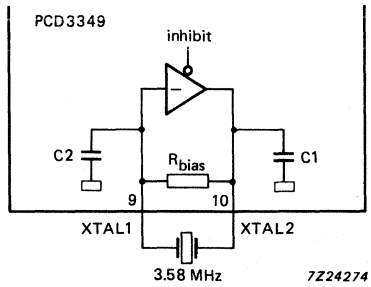


Fig. 14 Oscillator with integrated elements.

The oscillator has an output drive capability from pin 10 (XTAL2). An external clock can be applied to pin 9 (XTAL1). A machine cycle comprises 10 time slots, each time slot being 3 oscillator periods.

In telephony applications the 3.58 MHz crystal provides an 8.4 μs machine cycle. The range of the clock frequency is from 100 kHz up to a maximum which is a function of the supply voltage.

Timer/event counter (see Fig. 15)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 3 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin 8 (T1) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (182.6 kHz for an 8.4 μs machine cycle). When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump if timer flag = 1) or JNTF instruction. Overflow also generates an interrupt to the processor via setting of the Timer Interrupt Flag when the timer/event counter interrupt is enabled.

FUNCTIONAL DESCRIPTION (continued)

Timer/event counter (continued)

Table 3 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

* With prescaler select, PS = 0, the timer counts modulo-32 machine cycles, with PS = 1 it counts modulo-1 cycles (prescaler not used); prescaler cleared with STRT T, prescaler not readable.

** READ does not disturb the counting process.

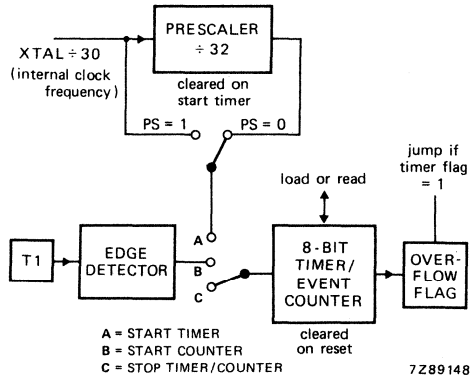


Fig. 15 Timer/event counter.

Program status word (see Fig. 16)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS); 0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS); 0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

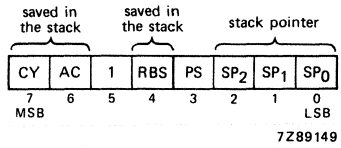


Fig. 16 Program status word.

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program counter (see Fig. 17).

A 12-bit program counter is used to facilitate 8 K bytes of ROM being addressed. The arrangement of the bits is shown in figure 17. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 12 bits are saved in the stack during CALL and interrupt routines.

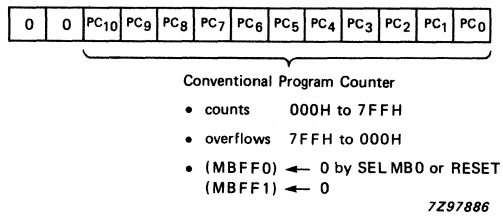


Fig. 17 Program counter.

Central processing unit

The PCD3349 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the CURRENT ROM page.

FUNCTIONAL DESCRIPTION (continued)

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program.
Table 4 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 4 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JNT0
	0	JT0*
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

* Because of the inverted interrupt input CE/$\overline{T0}$ the conditional jump JT0 is also inverted.

Test input T1 (pin 8)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for $>$ 4 CP, followed by a HIGH for $>$ 4 CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor ($R = \leqslant 100\ k\Omega$).
When T1 is not used pin 8 must be connected to V_{DD} or V_{SS}.

Reset (pin 11)

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory bank 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external and timer)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports according to reset states
- Cancels IDLE and STOP mode

After the voltage is applied to RESET an internal delay of 1866 CP is introduced before the microcontroller commences operation.

Power-on reset

The internal power-on reset circuit monitors the supply voltage V_{DD}. As long as V_{DD} remains below the internal reference level V_{ref} (typically 1.3 V), the oscillator is inhibited and RESET (pin 11) has an undefined level. When V_{DD} rises above V_{ref}, the oscillator is released and RESET is pulled HIGH to V_{DD} by TR1 for a period t_D (typically 50 μs). Note that the start-up time of the oscillator is typically 10 ms because of the narrow bandwidth of the crystal.

Three modes of power-on reset are possible:

1. If V_{DD} has a fast rise time, i.e. V_{DD} reaches its minimum value before the RESET signal finishes (t_D), then no additional circuit is required (see Figs 18 and 19). Note that the first instruction is executed after the oscillator start-up time plus 1866 clock periods.
2. If V_{DD} has a slow rise time then the RESET signal should be stretched by an external CR circuit (see Figs 20 and 21). In the event of a short drop in V_{DD}, the diode path discharges the capacitor rapidly to ensure a reliable power-on reset. The RESET signal should reach at least 70% of the final value of V_{DD} to ensure a correct reset. Given that the RESET voltage and V_{DD} rise exponentially, the above requirement is satisfied when the time constant of the RESET pulse is $>$ 8 times the time constant of V_{DD}. If V_{DD} rises linearly then a RESET time constant $>$ 2 times the rise time of V_{DD} is required.

   When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods (see Fig. 21). If the oscillator starts up prior to the completion of RESET then program execution begins 1866 clock periods after RESET goes LOW.
3. Fig. 22 shows an external reset applied during power-on. The external reset signal must remain HIGH until V_{DD} has reached its minimum operating value corresponding to the selected oscillator frequency. When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods (see Fig. 23). If the oscillator starts up prior to the completion of RESET then program execution begins 1866 clock periods after RESET goes LOW.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

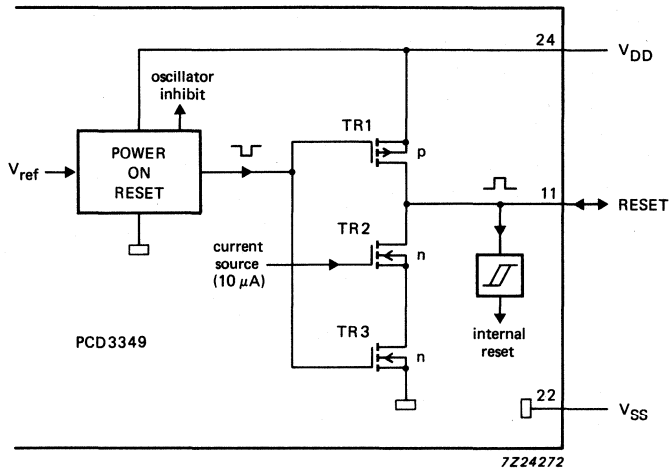


Fig. 18 Power-on reset configuration.

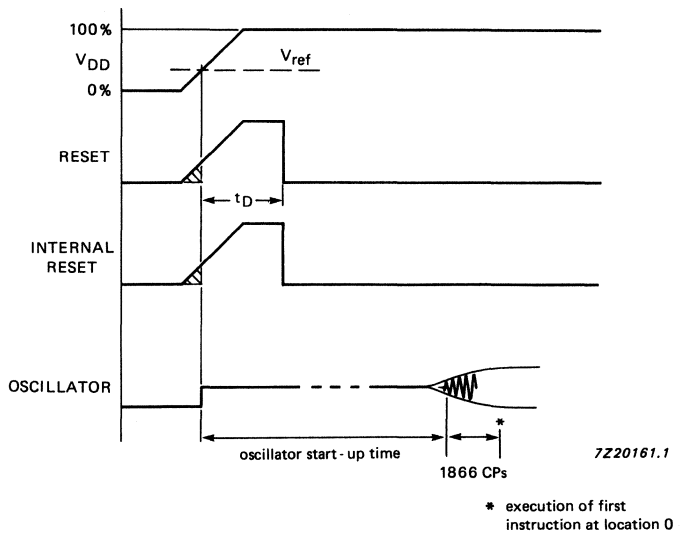


Fig. 19 Timing of power-on reset with fast rise time of V_{DD}.

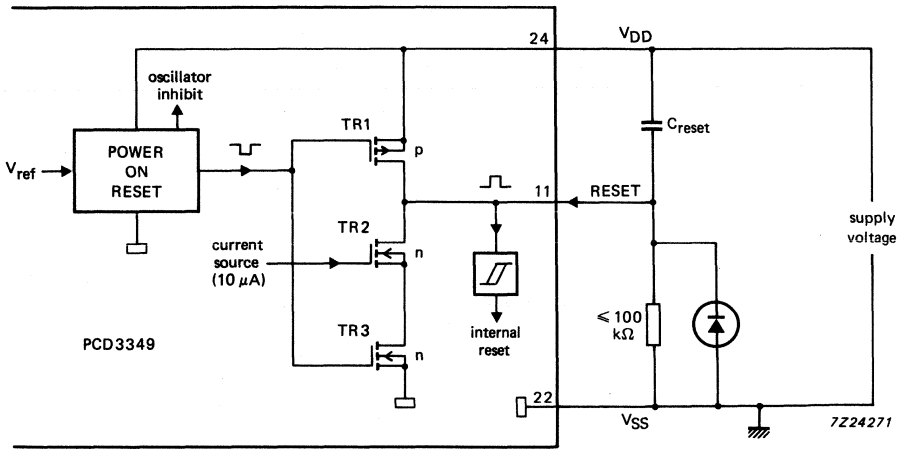


Fig. 20 Stretched power-on reset with external CR circuit.

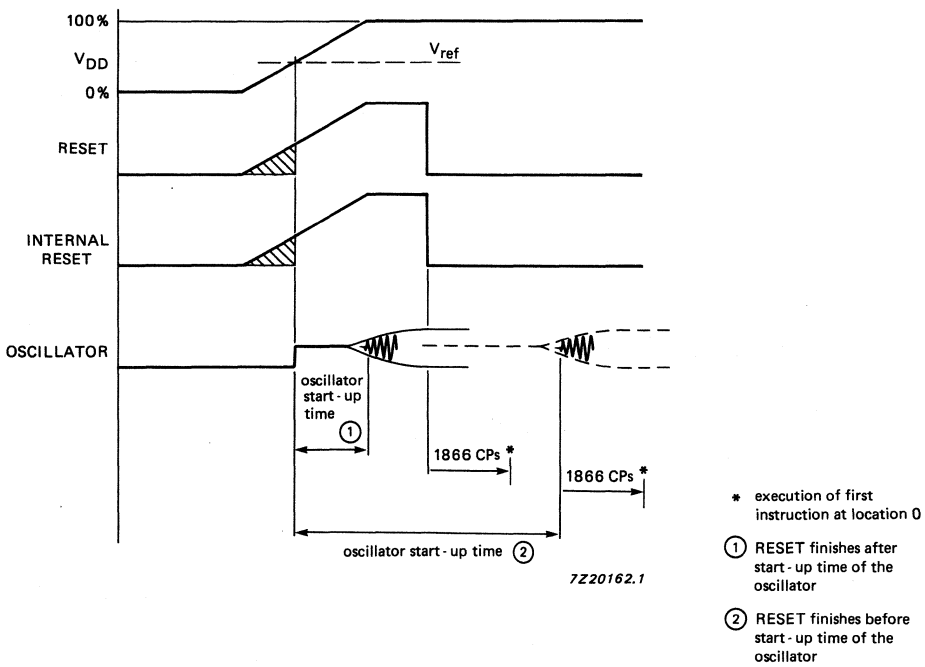


Fig. 21 Timing of power-on reset with a slowly rising V_{DD} and a stretched RESET pulse.

FUNCTIONAL DESCRIPTION (continued)

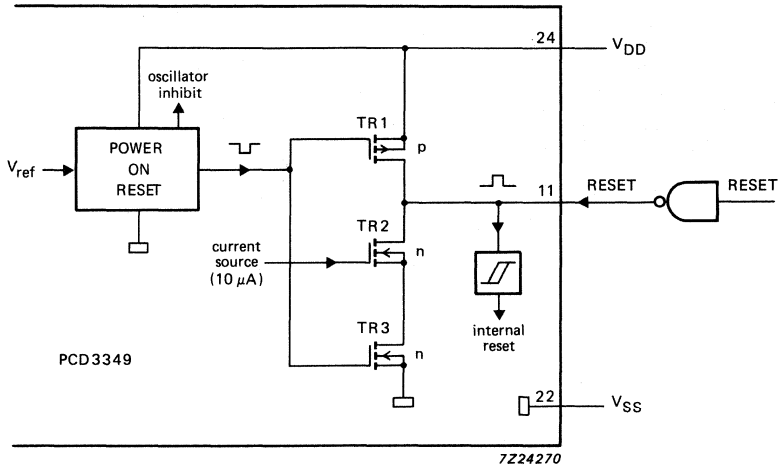


Fig. 22 External power-on reset configuration.

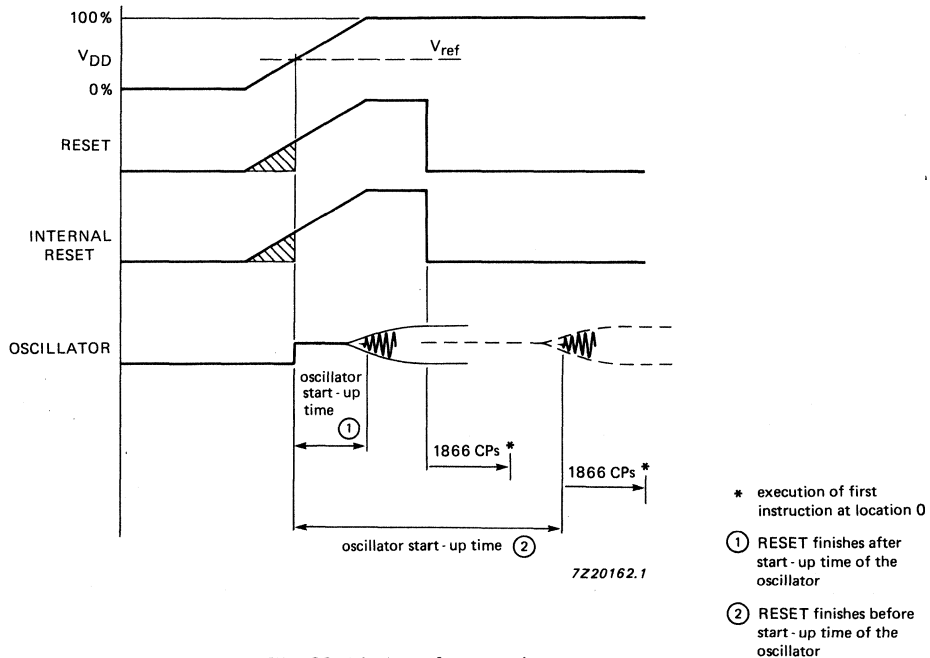


Fig. 23 Timing of external power-on reset.

INSTRUCTION SET

The PCD3349 instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for memory bank selection and derivative control. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 5 details the symbols and definition descriptions that are used in the instruction set of the PCD3349. Table 6 shows the instruction map and Table 7 gives the instruction set.

Table 5 Symbols and definitions used in Tables 6 and 7

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0 to 7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
D	mnemonic for 4-bit digit (nibble)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0 to 7)
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
Dx	derivative register (0 to H'FF')
←	is replaced by
↔	is exchanged with

DEVELOPMENT DATA

INSTRUCTION SET (continued)

Table 6 PCD3349 instruction map

first hexadecimal character of opcode ↓

second hexadecimal character of opcode →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, # data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp							
1	INC @Rr		JB0 addr	ADDC A, # data	CALL page 0	DIS I	JTF addr	INC A	INC Rr							
2	XCH A,@Rr		STOP	MOV A, # data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A,Rr							
3	XCHD A,@Rr		JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A							
4	ORL A,@Rr		MOV A, T	ORL A, # data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr							
5	ANL A,@Rr		JB2 addr	ANL A, # data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr							
6	ADD A,@Rr		MOV T, A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr							
7	ADDC A,@Rr		JB3 addr		CALL page 3			RR A	ADDC A,Rr							
8				RET	JMP page 4				ORL Pp, # data					MOV Dx,A		
9			JB4 addr	RETR	CALL page 4		JNZ addr	CLR C	ANL Pp, # data							
A	MOV @Rr, A			MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A							
B	MOV @Rr, # data		JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr, # data							
C	DEC @Rr				JMP page 6	SEL RB0	JZ addr	MOV A, PSW	DEC Rr							
D	XRL A,@Rr		JB6 addr	XRL A, # data	CALL page 6	SEL RB1		MOV PSW, A	XRL A,Rr							
E	DJNZ @Rr,addr				JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr							
F	MOV A,@Rr		JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr							

	0	1	2	3	4	5	6	7
0								
1	INC Rr							
2	XCH A,Rr							
3								
4	ORL A,Rr							
5	ANL A,Rr							
6	ADD A,Rr							
7	ADDC A,Rr							
8								
9								
A	MOV Rr,A							
B	MOV Rr, # data							
C	DEC Rr							
D	XRL A,Rr							
E	DJNZ Rr, addr							
F	MOV A,Rr							

Table 7 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

INSTRUCTION SET (continued)

Table 7 (continued)

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1})\leftarrow A_n$ $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data	r = 0–7	
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((R0_{0-3}))$ $(A_{0-3})\leftrightarrow((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3)\leftarrow(A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7})\leftarrow(A)$, $(A)\leftarrow((PC))$		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1	
BRANCH	JMP addr	● 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0 address	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1 address			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0 : (PC_{0-7})←addr	
	JT0 addr	36 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JNT0 addr	26 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

INSTRUCTION SET (continued)

Table 7 (continued)

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4, 6, 7}$) (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) – 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) – 1 ($PSW_{4, 6, 7}$) + (PC)←((SP))	6

DEVELOPMENT DATA

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
DERIVATIVE INPUT/OUTPUT	MOV Dx, A	8D	2/2	move accumulator contents to derivative register	(Dx)←(A) x = 0 to 255	8
	NOP	00	1/1	no operation		

Notes to Table 7

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).
5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 0000 P2.3, P2.2, P2.1, P2.0
8. Instructions for PCF84C00 only.

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 24)		V_{DD}	−0.8	+ 8	V
Input voltage (any pin)		V_I	−0.8	V_{DD} + 0.8	V
DC current (any input or output)		$\pm I_I, \pm I_O$	–	10	mA
Total power dissipation	note 1	P_{tot}	–	500	mW
Power dissipation (per output)		P_O	–	50	mW
Storage temperature range		T_{stg}	−65	+ 150	°C
Operating ambient temperature range		T_{amb}	−25	+ 70	°C
Operating junction temperature		T_j	–	+ 125	°C

Note to the ratings

1. Derate according to thermal resistance.

THERMAL RESISTANCE

From junction to ambient

SOT117	$R_{th\ j\text{-}a}$	=	120	K/W
SOT136A	$R_{th\ j\text{-}a}$	=	150	K/W

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3.58 MHz with R_S = 100 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage						
operating		V_{DD}	2.5	–	6	V
STOP mode for RAM data retention		V_{DD}	1.0	–	6	V
Supply current (Fig. 25)						
operating with tone generator on	V_{DD} = 3 V	I_{DD}	–	1.2	–	mA
operating without tone generator	V_{DD} = 3 V	I_{DD}	–	600	–	μA
IDLE mode (Fig. 26)						
with tone generator on	V_{DD} = 3 V	I_{DD}	–	900	–	μA
without tone generator	V_{DD} = 3 V	I_{DD}	–	300	–	μA
STOP mode (Fig. 27)	note 1; V_{DD} = 1.8 V					
	T_{amb} = 25 °C	I_{DD}	–	1.2	2.5	μA
	T_{amb} = 55 °C	I_{DD}	–	–	5	μA
	T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O						
Switching level		V_{RESET}	–	1.3	–	V
Sink current	$V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs						
Input voltage LOW		V_{IL}	0	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Input leakage current	$V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs						
Output voltage LOW	V_I = V_{SS} or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0.05	V
Output sink current LOW						
P1.2, P1.3, P1.4, P2.0, P2.1, P2.2, P2.3 (Fig. 28)	V_{DD} = 3 V; V_O = 0.4 V	I_{OL}	0.7	1.5	–	mA
for remaining ports (Fig. 29)	V_O = 0.4 V	I_{OL}	1.5	–	–	mA
Pull-up output source current HIGH (Fig. 30)	V_{DD} = 3 V;					
	V_O = 0.9 V_{DD}	$-I_{OH}$	10	–	–	μA
	V_O = V_{SS}	$-I_{OH}$	–	–	300	μA
Push-pull output source current HIGH	V_{DD} = 3 V;					
	V_O = V_{DD} −0.4 V	$-I_{OH}$	0.6	1.5	–	mA

TONE GENERATOR CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3.58 MHz with R_S = 100 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Tone output (Fig. 24)						
DTMF output voltage levels (RMS values)						
HIGH group		$V_{HG(rms)}$	158	192	205	mV
LOW group		$V_{LG(rms)}$	125	150	160	mV
Frequency deviation		$\Delta f/f$	−0.6	–	+ 0.6	%
DC voltage level		V_{dc}	–	½ V_{DD}	–	V
Output impedance		$\|Z_O\|$	–	0.1	0.5	kΩ
Pre-emphasis of group		ΔV_G	1.85	2.1	2.35	dB
Total harmonic distortion	note 2; T_{amb} = 25 °C	THD	–	−25	–	dB

Notes to the characteristics

1. Crystal connected between XTAL1 and XTAL2; CE and T1 at V_{SS}.
2. Related to the level of the LOW group frequency component (CEPT CS 203).

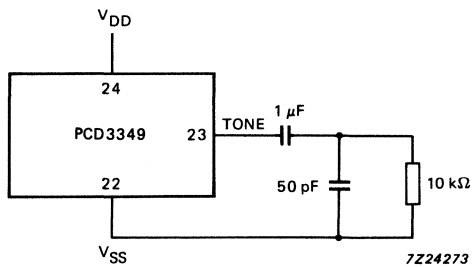


Fig. 24 Tone output test circuit.

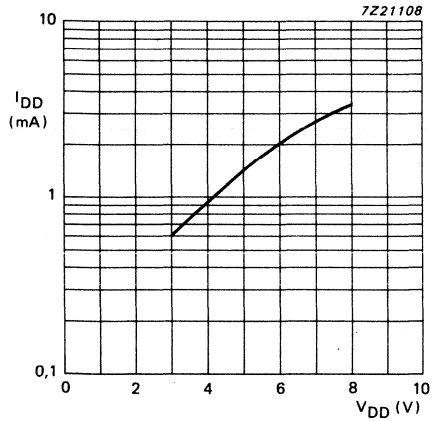


Fig. 25 Typical supply current (I_{DD}) in operating mode as a function of the supply voltage (V_{DD}); T_{amb} = 25 °C; clock frequency = 3.58 MHz; I_{DD} is increased by approximately 0.6 mA when the DTMF function is operating.

DEVELOPMENT DATA

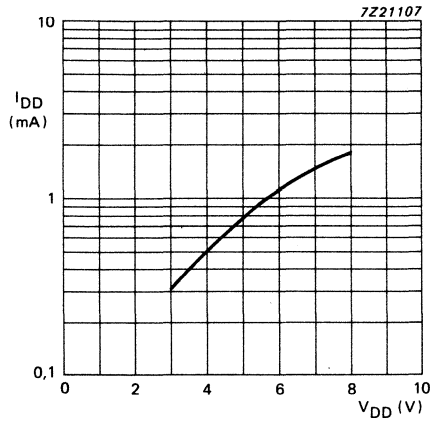
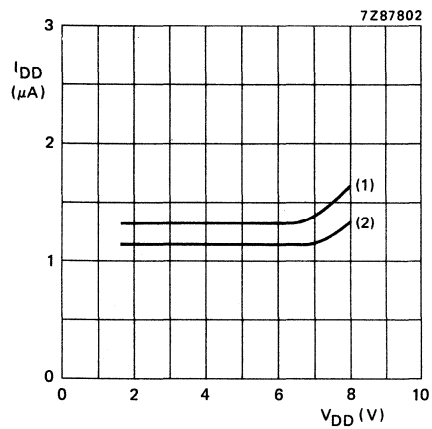
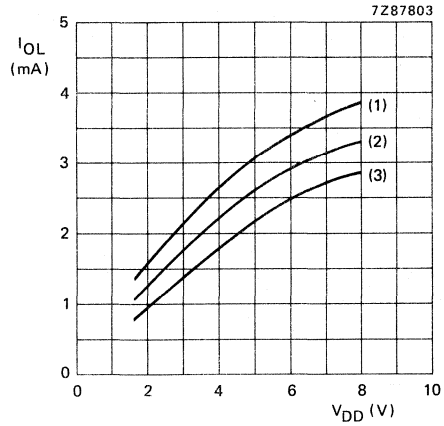


Fig. 26 Typical supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}); T_{amb} = 25 °C; clock frequency = 3.58 MHz.



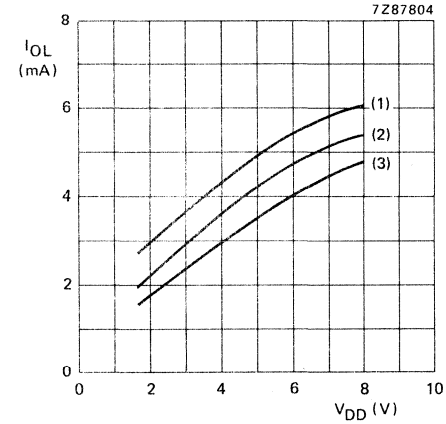
(1) T_{amb} = 25 °C
(2) T_{amb} = 70 °C

Fig. 27 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).



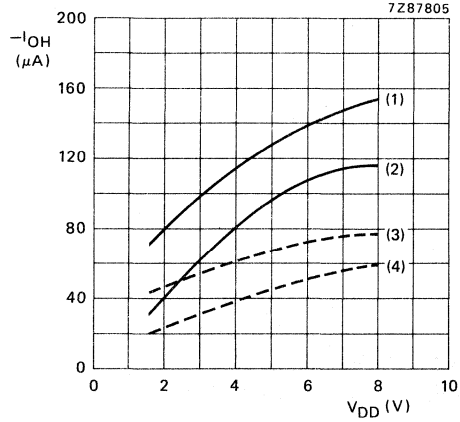
(1) T_{amb} = −25 °C
(2) T_{amb} = + 25 °C
(3) T_{amb} = + 70 °C

Fig. 28 Output sink current LOW (I_{OL}), for P1.2, P1.3, P1.4, P2.0, P2.1, P2.2, P2.3 as a function of supply voltage (V_{DD}); V_O = 0.4 V.



(1) T_{amb} = −25 °C
(2) T_{amb} = + 25 °C
(3) T_{amb} = + 70 °C

Fig. 29 Output sink current LOW (I_{OL}), for remaining ports as a function of supply voltage (V_{DD}); V_O = 0.4 V.



(1) T_{amb} = 25 °C; V_O = V_{SS}
(2) T_{amb} = 25 °C; V_O = 0.9 V_{DD}
(3) T_{amb} = 70 °C; V_O = V_{SS}
(4) T_{amb} = 70 °C; V_O = 0.9 V_{DD}

Fig. 30 Output source current HIGH ($-I_{OH}$) as a function of supply voltage (V_{DD}).

APPLICATION INFORMATION

A block diagram of an electronic featurephone built around the PCD3349 is shown in Figure 31. It comprises the following dedicated telephony ICs:

- TEA1060/1061/1067/1068 transmission circuit for telephony
- PCF8576 or PCF8577 2 LCD drivers in LCD module MB7020160
- PCF8571 1 K RAMs with Serial I/O; the number of RAMs depends on the required amount of stored telephone numbers
- PCD3360 programmable multi-tone ringer

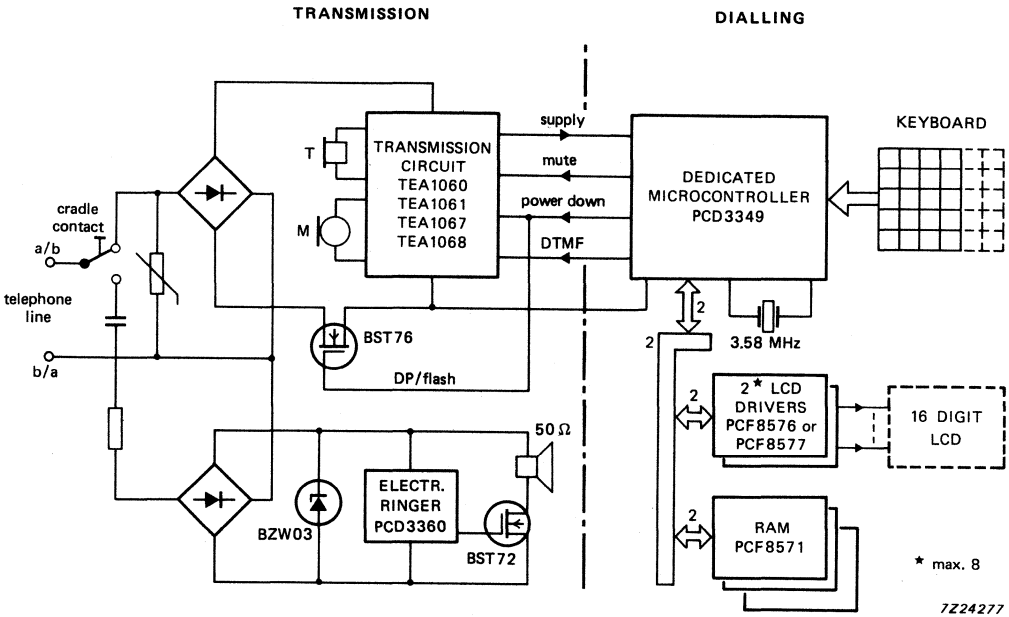


Fig. 31 Block diagram of electronic featurephone with common line interface.

PROGRAMMABLE MULTI-TONE TELEPHONE RINGER

GENERAL DESCRIPTION

The PCD3360 is a CMOS integrated circuit, designed to replace the electro-mechanical bell in telephone sets. It meets most postal requirements, particularly with tone sequence possibilities and input frequency selectivity. Output signals for a loudspeaker or for a piezo-electric (PXE) transducer are provided. No audio transformer is required since the loudspeaker is driven in class D.

Features

- Output signals for electro-dynamic transducer (loudspeaker) or for piezo-electric transducer (PXE)
- 7 basic frequencies (tones) and a pause
- 4 selectable tone sequences
- 4 selectable repetition rates
- 3 selectable impedance settings
- 3-step automatic swell
- Delta-modulated output signal that approximates a sinewave
- Input frequency discriminator with selectable upper and lower frequency limits
- Output for optical signal

Note

Tone sequences (up to 16 tones long), impedance settings and automatic swell levels are mask programmable for customized versions.

QUICK REFERENCE DATA

Available frequencies (tones)		533/600/667/800/ 1000/1067 and 1333	Hz
Number of intervals per tone sequence		15 or 16	
Lower limits of frequency discriminator		13,33 or 20	Hz
Upper limits of frequency discriminator		30 or 60	Hz
Impedance settings (with 50 Ω loudspeaker)	approx.	7 or 10,5 or 17,5	kΩ
Switch-on delay at 25 Hz	max.	60	ms

PACKAGE OUTLINES

PCD3360P: 16-lead DIL; plastic (SOT38).
PCD3360T: 16-lead mini-pack; plastic (SO16L; SOT162A).

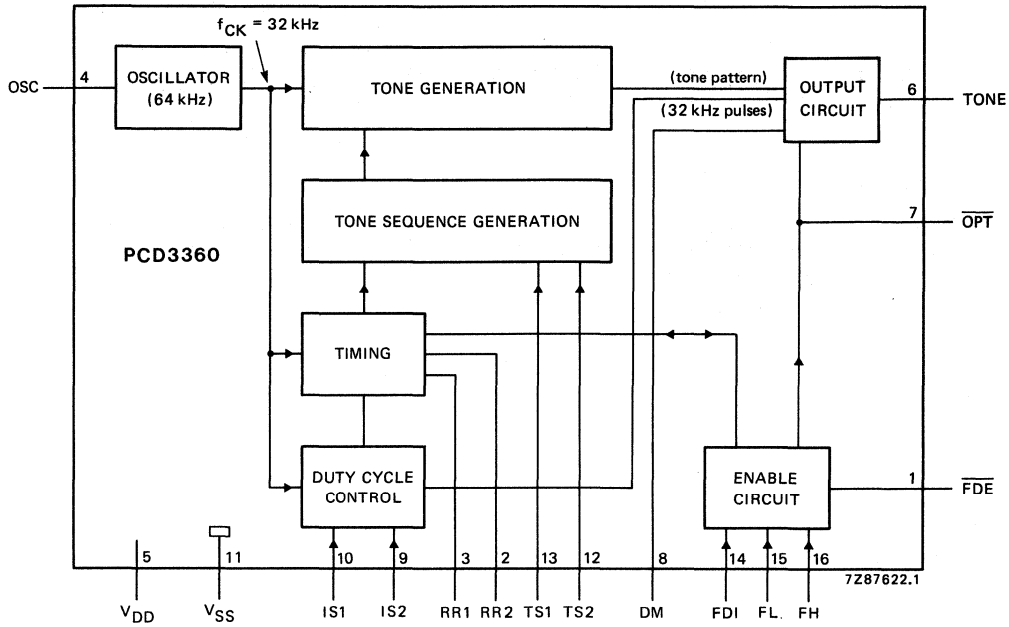


Fig. 1 Block diagram.

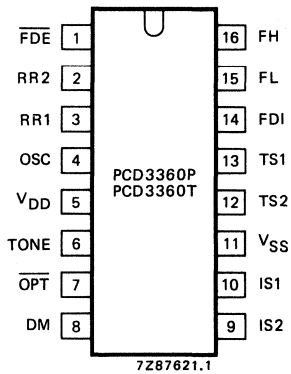


Fig. 2 Pinning diagram for PCD3360P and PCD3360T.

PINNING

1	$\overline{FDE}$	frequency discriminator enable
2	RR2	repetition rate selection
3	RR1	repetition rate selection
4	OSC	oscillator
5	V_{DD}	positive supply
6	TONE	tone output
7	$\overline{OPT}$	optical signal output
8	DM	drive mode selection
9	IS2	impedance setting and automatic swell
10	IS1	impedance setting and automatic swell
11	V_{SS}	negative supply
12	TS2	tone sequence selection
13	TS1	tone sequence selection
14	FDI	frequency discriminator input
15	FL	lower frequency limit selection
16	FH	upper frequency limit selection

FUNCTIONAL DESCRIPTION (see Fig. 1)

Supply pins (V_{DD} and V_{SS})

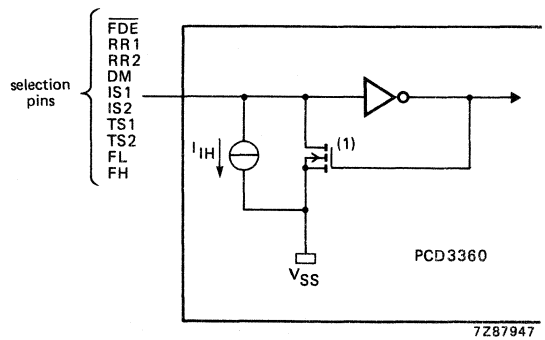
If the supply voltage (V_{DD}) drops below the standby voltage (V_{SB}), the oscillator and most other functions are switched off and the supply current is reduced to the standby current (I_{SB}). The automatic swell register retains its information until V_{DD} drops further to a value V_{AS} at which reset occurs.

Oscillator (OSC)

The 64 kHz oscillator is operated via an external resistor and capacitor connected to pin OSC. The oscillator signal is divided by two to provide the 32 kHz internal system clock.

Selection pins ($\overline{FDE}$, RR2, RR1, DM, IS2, IS1, TS2, TS1, FL and FH)

These pins are pulled down internally by a pull-down current I_{IH} when they are connected to V_{DD}, and by a pull-down resistance R_{IL} when they are connected to V_{SS} (see Fig. 3). Thus when the pins are open-circuit they are defined LOW. Therefore only a single-contact switch is required to connect the pins to V_{DD}; yet the supply current is only marginally increased as I_{IH} is very small.



(1) Transistor resistance = R_{IL} when switched on.

Fig. 3 Input circuit of selection pins.

Frequency discriminator circuit (pins $\overline{FDE}$ and FDI)

The frequency discriminator circuit prevents the ringer being activated by dial pulses, speech or other unqualified signals.

The circuit is enabled or disabled by input $\overline{FDE}$.

When $\overline{FDE}$ is HIGH, FDI acts as a logic enable input.
The circuit will produce tone sequences provided FDI is HIGH and V_{DD} exceeds V_{SB}.
When $\overline{FDE}$ is LOW, FDI acts as the frequency discriminator input.
The circuit will produce tone sequences provided V_{DD} exceeds V_{SB} and the signal at FDI fulfils the conditions set by FL and FH.

When the frequency discriminator is enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the circuit will start to produce tone sequences after two rising or two falling edges have occurred at FDI. The time between these edges must be within the limits set by FL and FH.

FUNCTIONAL DESCRIPTION (continued)

The circuit will continue to produce tone sequences provided the time between subsequent falling edges or between subsequent rising edges remains within the limits set by FL and FH, otherwise it will stop. Because two edges are required for detection, either positive or negative, the switch-on delay will vary between 1 and 1,5 cycles of the incoming ringing frequency.

FDI has a Schmitt-trigger action; the levels are set by an external resistor R2 (see Fig. 8) and an internal sink current that is switched from 20 μA (typ.) for FDI = LOW to $< 0{,}1$ μA for FDI = HIGH. Excess current entering FDI via R2 is absorbed by internal diodes clamped to V_{DD} and V_{SS}.

Selection of frequency discriminator limits (FL and FH)

With the frequency discriminator enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the lower and upper limits of the input frequency are set by inputs FL and FH as shown by Table 1 and Table 2 respectively.

Table 1 Selection of lower frequency discriminator limits (f_{osc} = 64 kHz)

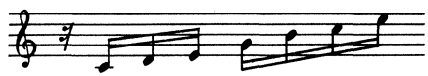
FL input state	lower discriminator limit (Hz)
LOW	20
HIGH	13,33

Table 2 Selection of upper frequency discriminator limits (f_{osc} = 64 kHz)

FH input state	upper discriminator limit (Hz)
LOW	60
HIGH	30

Selection of tone sequences (TS1 and TS2)

A tone sequence is composed of 15 or 16 equal time intervals. Each time interval may be filled with one of seven available tones or with a pause; these are shown together with their corresponding internal ROM tone code in Fig. 4.



tone key	–	c	d	e	g	b	c	e
frequency (Hz)	0	533	600	667	800	1000	1067	1333
frequency ratio		8	9	10	12	15	16	20
tone code	0	1	2	3	4	5	6	7

7Z87948

Fig. 4 Available tones and their corresponding internal ROM tone code.

Four tone sequences are programmed in the internal ROM (see Fig. 5). Inputs TS1 and TS2 determine which tone sequence is selected and output at pin TONE. The sequences are mask programmable with any length up to 16 time intervals.

The tone sequences are repeated continuously provided the enable conditions at inputs $\overline{FDE}$ and FDI are valid and $V_{DD} > V_{SB}$; the first sequence always starts with the first tone shown in Fig. 5.

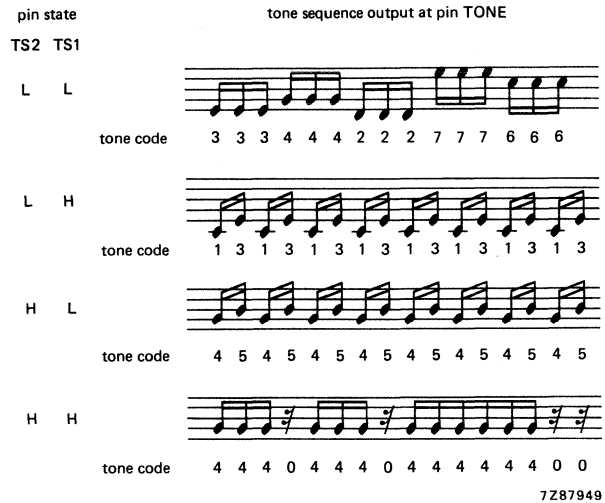


Fig. 5 Tone sequences mask-programmed in the PCD3360.

Selection of repetition rates (RR1 and RR2)

The duration of a time interval within a tone sequence is determined by the state of inputs RR1 and RR2 as shown in Table 3. The resultant variation of repetition rate acts as a distinguishing feature between adjacent telephones.

Table 3 Duration of time intervals (f_{osc} = 64 kHz)

input state		time interval
RR1	RR2	ms
L	L	15
L	H	30
H	L	45
H	H	60

The repetition rate variation can be extended by mask programming (for customer defined versions) the same tone combination for all 4 tone sequences, but with a different number of time intervals per tone. Thus the repetition rate can be selected from 16 values by inputs RR1, RR2, TS1 and TS2.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Drive mode selection (DM)

The output signal at pin TONE can be selected for application with electro-dynamic or piezo-electric transducers. An example of both signals, for a tone frequency of 667 Hz, is shown in Fig. 6.

Loudspeaker mode

In the loudspeaker mode (DM = LOW), pin TONE outputs a delta-modulated signal that approximates a sinewave sampled at a rate of 32 kHz. The output pulse duration is determined by pins IS1 and IS2. The resultant acoustic spectrum is aurally more acceptable and has greater penetration than a square wave spectrum because more power is concentrated at the fundamental frequency.

PXE mode

In the PXE mode (DM = HIGH), pin TONE outputs a square wave. In this mode the ringer impedance and sound pressure level are determined by the characteristics (e.g. the size) of the PXE transducer; inputs IS1 and IS2 are inactive.

Setting of impedance, sound pressure level and automatic swell (IS1 and IS2)

With DM = LOW (loudspeaker mode), inputs IS1 and IS2 determine the pulse duration of the output signal and thereby the d.c. resistance R_{xy} (seen at points x and y in Fig. 8), the input impedance Z_I and and also the Sound Pressure Level (SPL). The selection of 3 impedance settings and automatic swell is shown in Table 4.

Table 4 Setting of pulse duration and automatic swell (DM = LOW)

input state		function	ringing burst number (N)	pulse duration (μs)		R_{xy} (kΩ)	Z_I (kΩ)	SPL (dBr)
IS1	IS2			fund.	harm.			
L	L	automatic swell	1	1,9	–	40	tbf	tbf
			2	2,9	–	20	17,5	–4
			>2	4,1	1,8	5	7	0
L	H	constant level	–	2,9	–	20	17,5	–4
H	L		–	3,8	–	10	10,5	tbf
H	H		–	5,4	–	5	7	0

Where:

1. Typical pulse duration values of the fundamental and harmonic frequencies are for f_{osc} = 64 kHz and f_{CK} = 32 kHz.
2. SPL is the relative Sound Pressure Level, and 0 dBr is defined as the SPL for IS1 = IS2 = HIGH.
3. Values of the d.c. resistance R_{xy}, bell impedance (Z_I) and SPL are valid for a value of input voltage V_I = 40 V_{rms} at 25 Hz in Fig. 8.

Setting of impedance, sound pressure level and automatic swell

When pins IS1 and IS2 are both LOW, the circuit operates in the automatic swell mode. The SPL then increases in three steps so that the maximum level is reached for the third ringing burst.
Each time V_{DD} drops below V_{AS} the automatic swell register is reset and the next ringing burst is considered as N = 1 (see Table 4).
A buffer capacitor C3 (see Fig. 8) must hold $V_{DD} > V_{AS}$ during the time between two consecutive ringing bursts of a series.

For each of the other three combinations of pins IS1 and IS2 the pulse duration has a constant value. Thus the ringer can be designed so that the impedance represented at the telephone line will comply with postal requirements that vary in relation to parallel or series connections of more than one ringer.

To satisfy some applications, a harmonic signal is added to the fundamental frequency in the last step of the automatic swell mode. The pulses representing this harmonic signal are interleaved with the pulses of the fundamental signal (see Fig. 7). The difference in pulse duration shown in Table 4, is chosen so that the harmonic level is 10 dB below the fundamental level.
The harmonic frequency range is from 2 kHz to 3,2 kHz. The individual harmonic frequencies for the seven tone codes and the relative fundamental frequencies are shown in Table 5.

Table 5 Harmonic frequency in relation to tone code and fundamental frequency

tone code	frequency (Hz)	
	fundamental	harmonic
1	533	3200
2	600	2400
3	667	2667
4	800	3200
5	1000	2000
6	1067	2133
7	1333	2667

DEVELOPMENT DATA

Using a single mask it is possible to program the following:—

- Addition of harmonics in all the other input states of IS1 and IS2
- All pulse duration values
- Other even harmonic frequencies.

Optical output ($\overline{OPT}$)

The $\overline{OPT}$ output is designed to drive an optical signal transducer or lamp. It is LOW when the ringer circuit is enabled and HIGH when the ringer circuit is disabled. This output can also be used to switch the transmitter ON and OFF in the base of a cordless telephone set.

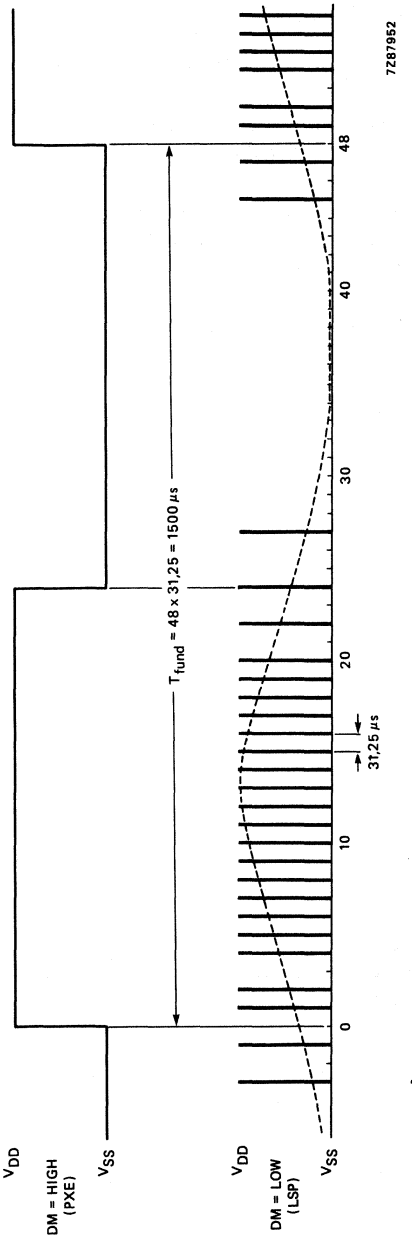


Fig. 6 Fundamental signal (667 Hz) at pin TONE (for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

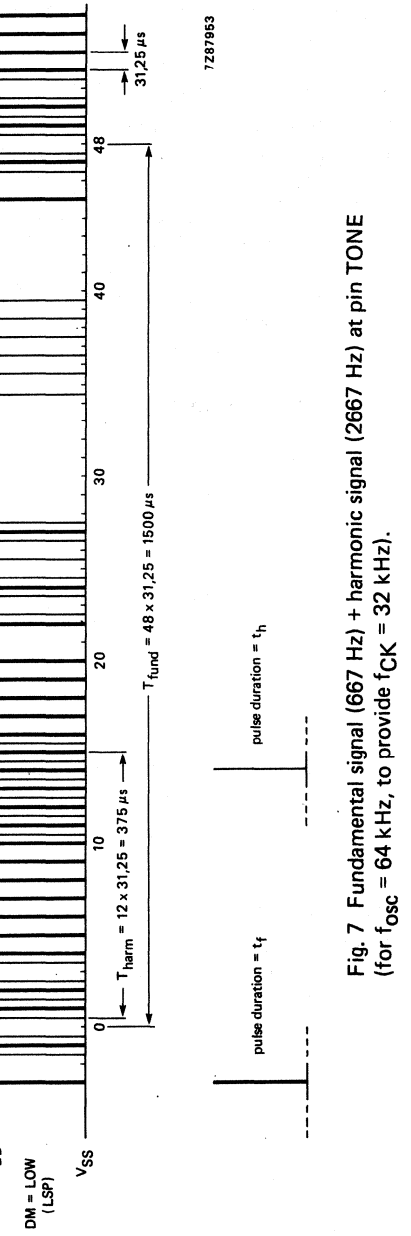


Fig. 7 Fundamental signal (667 Hz) + harmonic signal (2667 Hz) at pin TONE (for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to + 9	V
Supply current	I_{DD}	max.	50	mA
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Total dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	V_{SB}+0,1	–	8,0	V
Standby supply voltage (note 1)	V_{SB}	3,9	4,8	5,7	V
Supply voltage for automatic swell reset (note 2)	V_{AS}	–	0,5V_{SB}	–	V
Operating supply current (note 3)	I_{DD}	–	110	140	μA
Standby supply current at $V_{DD} < V_{SB}$ (note 4)	I_{SB}	–	3	8	μA
Inputs					
Input voltage LOW (any pin)	V_{IL}	0	–	0,3V_{DD}	V
Input voltage HIGH (any pin)	V_{IH}	0,7V_{DD}	–	V_{DD}	V
Pull-down circuits of inputs					
FDE, RR1, RR2, DM, IS1, IS2, TS1, TS2, FL, FH					
pull-down resistance with input at V_{SS}	R_{IL}	–	20	–	kΩ
pull-down current with input at V_{DD}	I_{IH}	–	0,1	–	μA
Pull-down circuit of FDI					
pull-down current with V_{FDI} = 0,3V_{DD}; T_{amb} = 25 °C	I_{SL}	14	23	32	μA
temperature coefficient of I_{SL}	$-\Delta I_{SL}$	–	0,5	–	%/°C
pull-down current with V_{FDI} = 0,8V_{DD}	I_{SH}	–	0,1	–	μA
pull-down current with $V_{DD} < V_{SB}$	I_{SX}	–	0,1	–	μA
Current into input FDI (note 5)	± I_{IS}	–	–	0,2	mA
Outputs					
TONE, $\overline{OPT}$					
Output sink current at V_{OL} = 0,5 V	I_{OL}	1	2	–	mA
Output source current at V_{OH} = V_{DD}−0,5 V	$-I_{OH}$	1	2	–	mA

A.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Switch-on delay (with $\overline{FDE}$ = LOW and ringing frequency within limits set by FL and FH)	$t_{d(on)}$	1	–	1,5	note 6
Switch-off delay (with $\overline{FDE}$ = LOW)					
at FL = LOW	$t_{d(off)}$	–	–	50	ms
at FL = HIGH	$t_{d(off)}$	–	–	75	ms
Oscillator frequency					
at R_{osc} = 365 kΩ; C_{osc} = 56 pF; T_{amb} = 25 °C (note 7)	f_{osc}	60	64	68	kHz
Frequency variation					
as a function of V_{DD}	$-\Delta f_{osc}$	–	1	–	%/V
as a function of T_{amb}	$-\Delta f_{osc}$	–	0,05	–	%/K

DEVELOPMENT DATA

Notes to the characteristics

1. For $V_{DD} < V_{SB}$ the circuit is in standby.
2. At $V_{DD} = V_{AS}$ the automatic swell register is reset.
3. R_{osc} = 365 kΩ; C_{osc} = 56 pF; FDI = $\overline{FDE}$ = V_{DD}; all other inputs and outputs open circuit.
4. The standby supply current is measured with all inputs and outputs open-circuit with the exception of OSC.
5. The current I_{IS} is clamped to V_{DD} and to V_{SS} by two internal diodes. Correct operation is ensured with $V_{FDI} > V_{DD}$ or $V_{FDI} < V_{SS}$, provided the maximum value of I_{IS} is not exceeded. (The input FDI has an extended HIGH and LOW input voltage range.)
6. The switch-on delay is measured in cycles of incoming ringing frequency.
7. Lead lengths of R_{osc} and C_{osc} to be kept to a minimum.

APPLICATION INFORMATION

Application of the PCD3360 in a telephone ringer circuit together with a loudspeaker is shown in Fig. 8.

The threshold levels V_H and V_L of the frequency discriminator circuit are determined by:

- The logic threshold of input FDI ($0{,}5V_{DD}$ typ. 3,4 V for V_{DD} = 6,8 V)
- The pull-down current of input FDI (20 μA typ. for FDI < 3,4 V)
- The value of R2 (680 kΩ in Fig. 8)

For a positive slope, the voltage at R2 must exceed the value V_H before FDI will become HIGH; V_H is the sum of the input threshold and the voltage drop across R2 thus:

$V_H = 3{,}4 + (680 \times 10^3) \times (20 \times 10^{-6}) = 17$ V.

For a negative slope, the voltage at R2 must decrease below the value V_L before FDI will become LOW. Because the current into FDI is negligible with FDI = HIGH the voltage drop across R2 can be discounted, thus V_L = 3,4 V.

The minimum operating voltage across C3 is 17,8 V which is determined by:

- The minimum operating voltage of the PCD3360 (5,8 V)
- The supply current of the PCD3360 (120 μA max.)
- The value of R3 (100 kΩ in Fig. 8)

The total switch-on delay equals approximately the time required to charge the supply capacitor C3 to the minimum operating value, plus the specified switch-on delay of the PCD3360.

The high operating voltage combined with the class D output stage ensures optimal energy conversion and thereby a high sound level. The design can easily be optimized for parallel or series connection of more than one ringer. The diode bridge, zener diode (D1) and resistor R1 protect the ringer against transients up to 5 kV. During these surges the voltage on the 68 V zener diode (BZW03) can rise to 100 V; the DMOS transistor BST72A (TR1) has a maximum drain-source voltage of 100 V. Up to 220 V, 50 Hz can be applied to the a/b terminals without damaging the ringer.
The choke (L1) in series with the 50 Ω loudspeaker increases the sound pressure level by approximately 3 dB by suppression of the 32 kHz carrier frequency and its sidebands.
The flyback diode BAX18A (D2) is a fast type with low forward voltage to obtain high efficiency.

Application of the PCD3360 together with a PXE transducer is shown in Fig. 9. The only significant difference between Fig. 8 and Fig. 9 is the output stage. Two BST72A transistors provide an output voltage swing almost equal to the voltage at C3. Pins IS1 and IS2 are inoperative because DM = HIGH. Volume control is possible using resistor R_V.

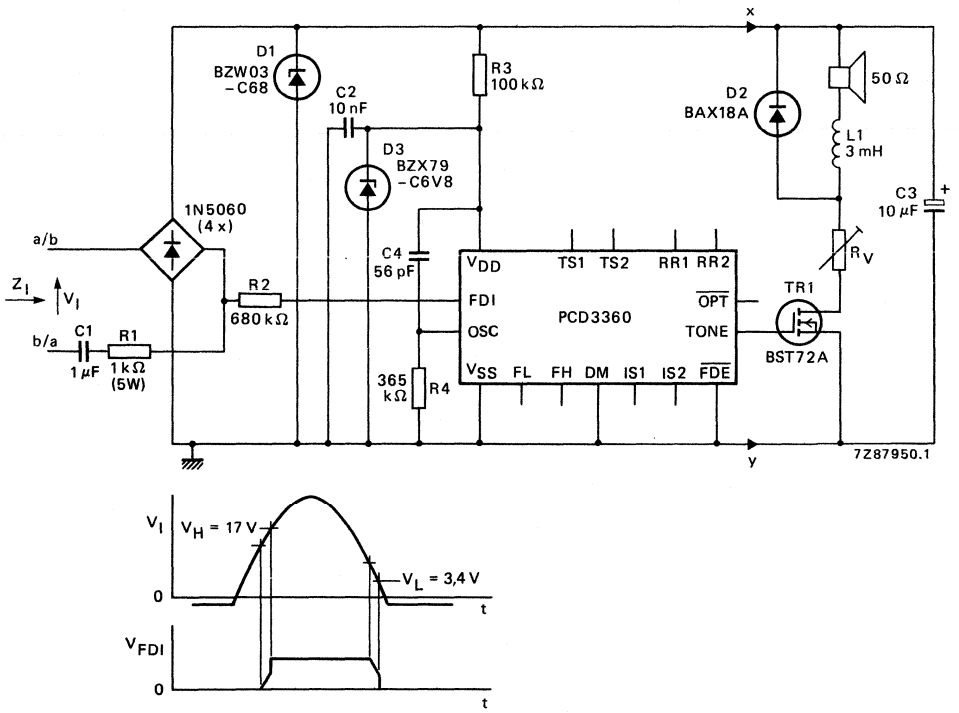


Fig. 8 Transformerless electronic ringer with PCD3360 and a loudspeaker.

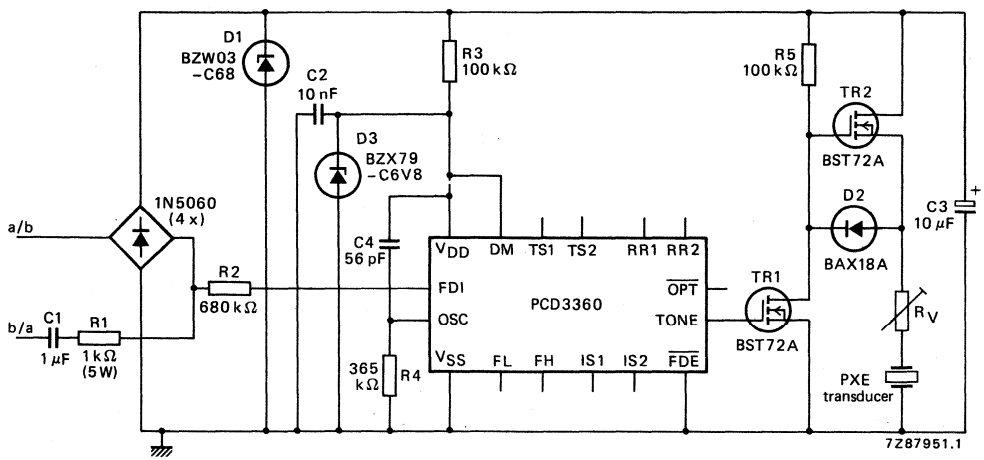


Fig. 9 PCD3360 ringer with PXE transducer.

PULSE AND DTMF DIALLER WITH REDIAL

GENERAL DESCRIPTION

The PCD4410 is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3,58 MHz crystal. It is a dual-standard dialling circuit for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either PD or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

Features

- Pulse and DTMF dialling
- 23-digit capacity for redial operation
- Three dialling modes; pulse, DTMF and data transmission (DTMF)
- Redial buffer for PABX and public calls
- Three function keys; *, # and FL (flash)
- DTMF timing:
  - manual dialling — minimum duration for bursts and pauses
  - redialling — calibrated timing
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3,58 MHz (tv colour burst) crystal
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	1,8 to 6,0	V
Low standby current (on hook) at V_{DDO} = 1,8 V	I_{DDO}	max. 5	μA
Operating currents			
conversation mode	I_{DDC}	max. 150	μA
pulse dialling mode	I_{DDP}	max. 200	μA
DTMF dialling mode	I_{DDF}	max. 0,9	mA
DTMF output voltage level (r.m.s. values)			
HIGH group	$V_{HG(rms)}$	typ. 192	mV
LOW group	$V_{LG(rms)}$	typ. 150	mV
Pre-emphasis of group	ΔV_G	typ. 2,1	dB
Total harmonic distortion	THD	−25	dB
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINES

18-lead DIL; plastic (SOT102).

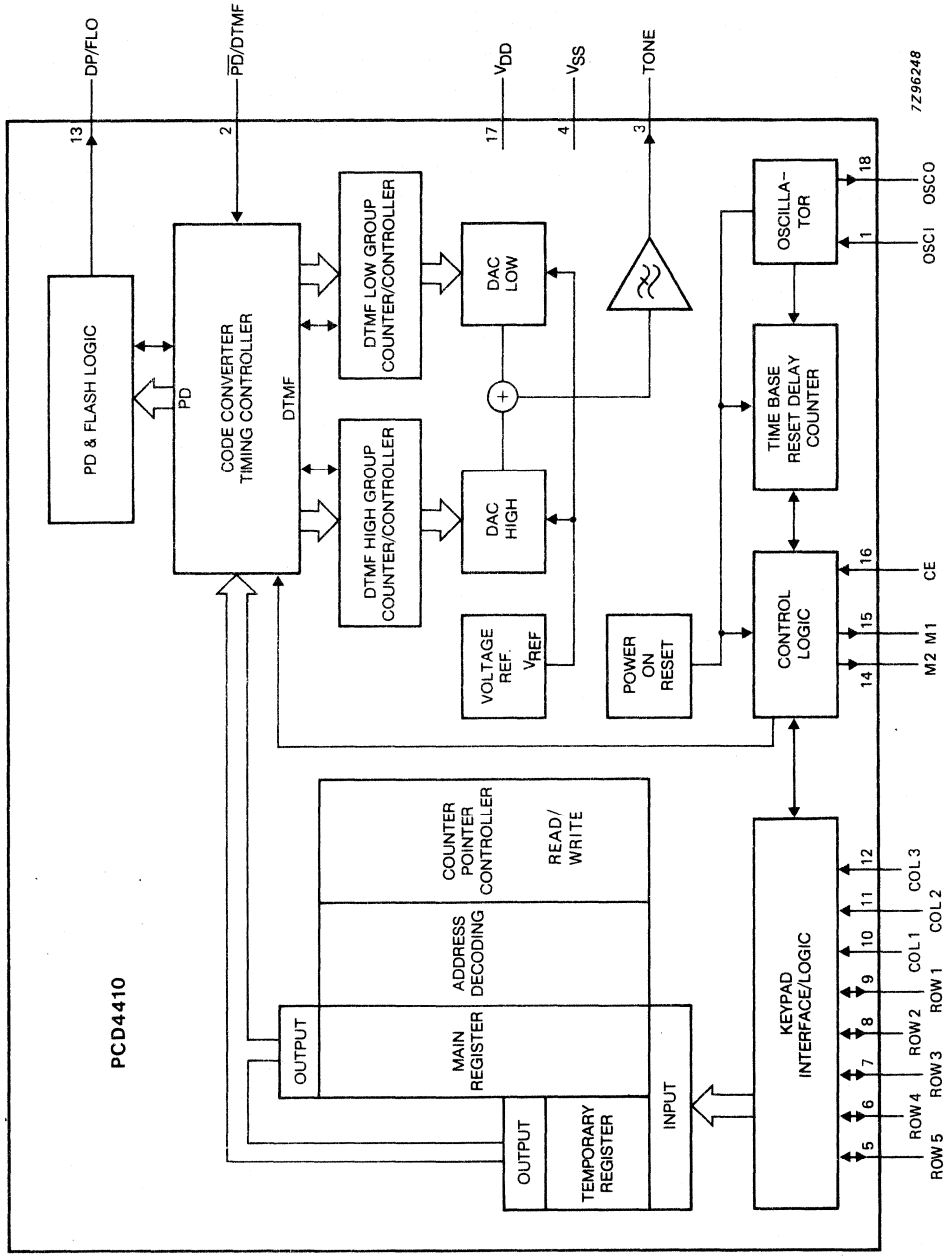


Fig. 1 Block diagram.

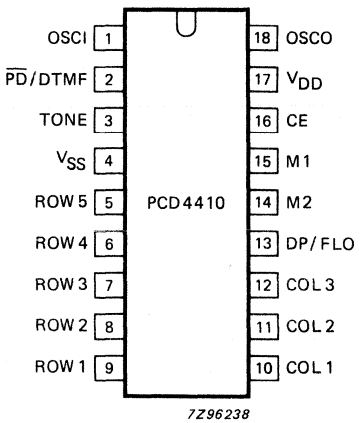


Fig. 2 Pinning diagram.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	ROW 5	scanning row keyboard input/outputs
6	ROW 4	
7	ROW 3	
8	ROW 2	
9	ROW 1	
10	COL 1	sense column keyboard inputs with internal pull-ups
11	COL 2	
12	COL 3	
13	DP/FLO	dialling pulse and flash output
14	M2	strobe; active HIGH during transmission
15	M1	muting output
16	CE	chip enable input
17	V_{DD}	positive supply
18	OSCO	oscillator output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.
To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.
If V_{DD} drops below the minimum standby supply voltage of 1,8 V the power-on reset circuit inhibits redialling after hook-off.
The power-on-reset signal has the highest priority. It blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the PCD4410 for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) which points to the last entered digit (see Fig. 4). The keyboard input is inhibited, but data previously entered is saved in the redial register as long as V_{DD} is higher than $V_{DDO(min)}$.
The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on.

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for more than time t_{rd} (see Fig. 8a, Fig. 8b and timing data) the system changes to the static standby state and the oscillator stops running. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

PD mode

If $\overline{PD}$/DTMF = V_{SS} the pulse dialling mode is selected.

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each numeric push-button activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfil the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

Data transmission mode

Data transmission mode is entered from the dialling mode (PD or DTMF) on first depression of key*. The "*" tones are not transmitted.
In the data transmission mode no digits are stored for later redial, "*" and "#" are purely DTMF keys, so are no longer special functions. The digits are temporarily stored in a special register, which has a maximum capacity of eight digits.

There are two ways to leave the data transmission mode:

- Reactivate chip enable (CE); HIGH to LOW then HIGH again
- Pressing the flash (FL) key

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 3 and the scanning row outputs ROW 1 to ROW 5 of the PCD4410 are directly connected to the keyboard as shown in Fig. 3.
All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e as shown in Fig. 8. Each entry is tested for validity.

When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the pushbutton.

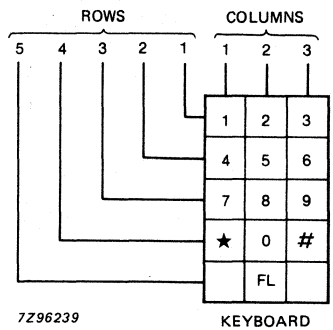


Fig. 3 Keyboard organization.

Row 5 of the keyboard contains the special function key FL — flash or register recall.

Flash

Flash (or register recall) is activated by the FL key and can be used in DTMF, pulse and data transmission modes. Pressing the FL pushbutton will produce a timed line-break of 100 ms at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. This flash pulse duration (t_{FL}) is calibrated at 100 ms.

The flash pulse resets the read address counter (RAC). Later redial is possible (see redial procedure with the "Flash" inserted telephone number).

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

FUNCTIONAL DESCRIPTION (continued)

Table 1 Frequency tolerance of the output tones for DTMF signalling

row/ column	standard frequency Hz	tone output frequency Hz (1)	frequency deviation	
			%	Hz
row 1	697	697,90	+0,13	+0,90
row 2	770	770,46	+0,06	+0,46
row 3	852	850,45	−0,18	−1,55
row 4	941	943,23	+0,24	+2,23
col 1	1209	1206,45	−0,21	−2,55
col 2	1336	1341,66	+0,42	+5,66
col 3	1477	1482,21	+0,35	+5,21

(1) Tone output frequency when using a 3,579 545 MHz crystal.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output stays LOW. During Flash the mute output is active HIGH and remains at this level for the period of flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD4410 it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break and make time in pulse dialling, or during tone transmission in DTMF dialling.

Data transmission mode

Timing in the data transmission mode is the same as the manual dialling mode.

DIALLING PROCEDURES (see also Figs 5, 6 and 7)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig. 4). By entering first a numeric digit, the Write Address Counter (WAC) will be set to the first address, the decoded digit will be stored in the register and the WAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. If more than 23 digits are entered redial will be inhibited. All entries are debounced on both the leading and trailing edges for at least time t_e as shown in Fig. 8. Each entry is tested for validity before being deposited in the redial register.

In manual dialling mode (pulses and DTMF) only the 0 to 9 keys result in dialling operations.

"#" and "*" are special function keys:

 # key

- If the first key after CE or Flash means: Redial (see redial procedure)
- If not the first key, then # is used to program access pause(s) in the RAM for later redial. If it is the last key it will be omitted before going "on-hook".

** key*

- Used to switch from dialling mode (pulse or DTMF) to data transmission mode. The * tones will not be transmitted even if the previous mode was DTMF dialling.

In data transmission mode keys 0 to 9, * and # result in associated DTMF tones (see Table 1).

DEVELOPMENT DATA

Redialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The PCD4410 is in conversation mode.
If "#" is the first keyboard entry the circuit starts redialling the contents of the register,
Timing in the DTMF mode is calibrated for both tone bursts and pauses.
Only the first part entered (the pulse or DTMF dialled part of the stored number) can be redialled.
During redial keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of redailling. The # key is active only during access pauses.

No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory overflow (more than 23 valid data entries)

If an access pause is detected during redial, the circuit is switched back to the conversation mode and stays there until the # key is depressed. Therefore when the # key is depressed the access pause is ended. After termination of the access pause the circuit continues dialling the rest of the telephone number.

If after "on-hook" or "flash" the last stored digit is an access pause then it will be deleted out of the memory.

As soon as the conversation mode is entered depressing the * key will again switch the circuit to the data transmission mode.

Redial takes place in the main register (max. 23 digits). After redial when a numeric key is pressed (first digit of an extension number) the redial number will be cleared. Thus the total capacity of the main register is available for extension number dialling. This extension number is stored in the main register (max. 23 digits) and is available later after "on-hook", "off-hook".

The main register will also store digits that have been keyed-in at a rate faster than dialled out.

Access pause

- The number of access pauses is unlimited.
- Consecutive pauses will be stored as a single pause.

DIALLING PROCEDURES (continued)

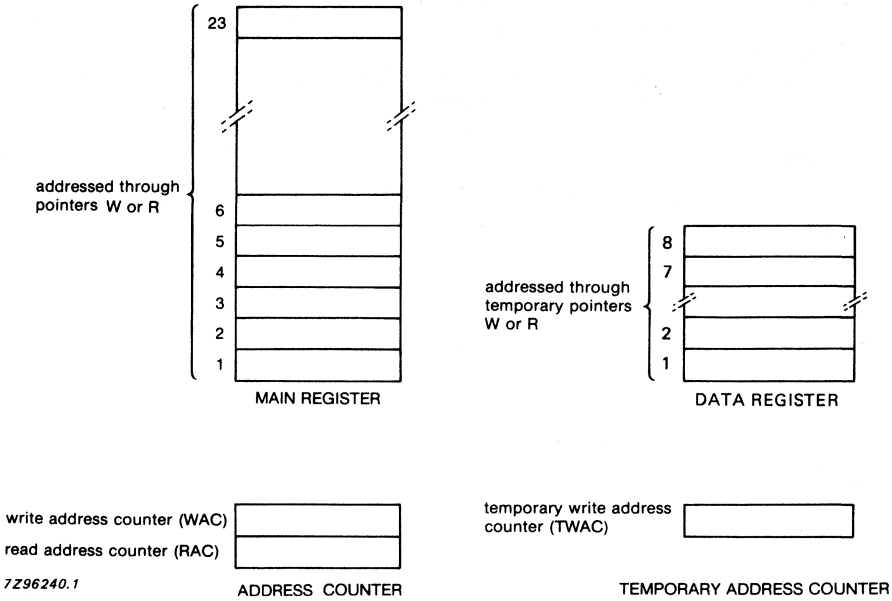


Fig. 4 Memory organization.

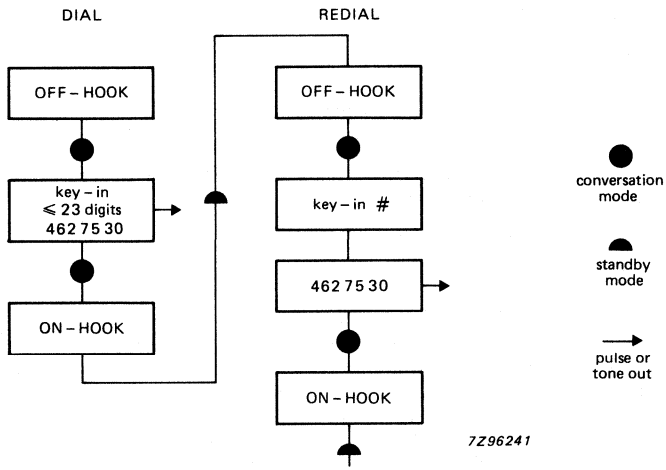


Fig. 5 Pulse/DTMF dialling mode.

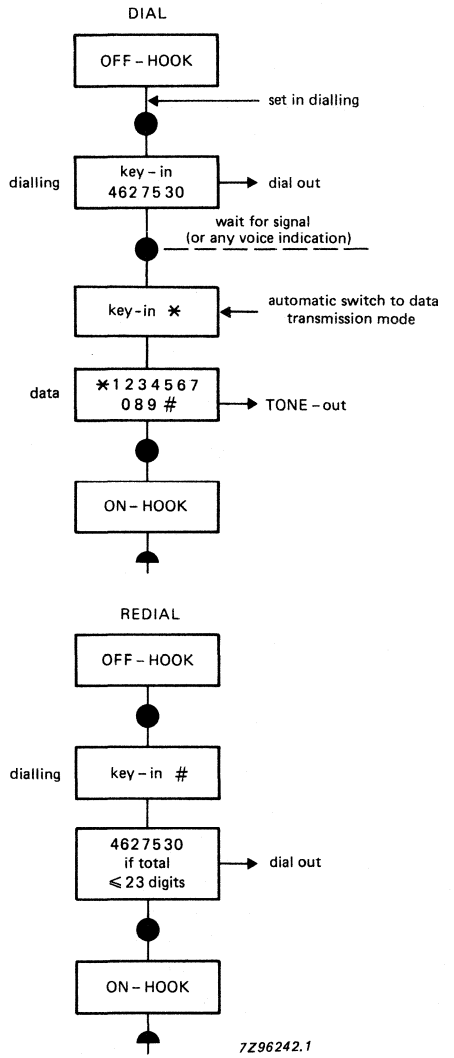


Fig. 6 Pulse/DTMF dialling and data transmission mode.

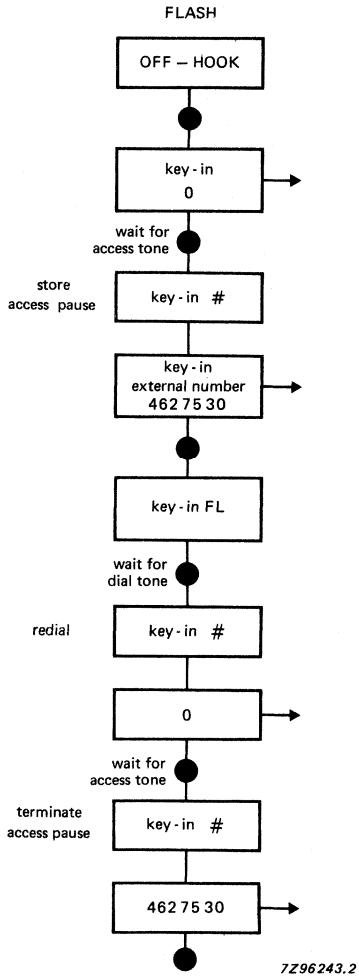


Fig. 7 Flash; independent of dialling mode.

DEVELOPMENT DATA

TIMING

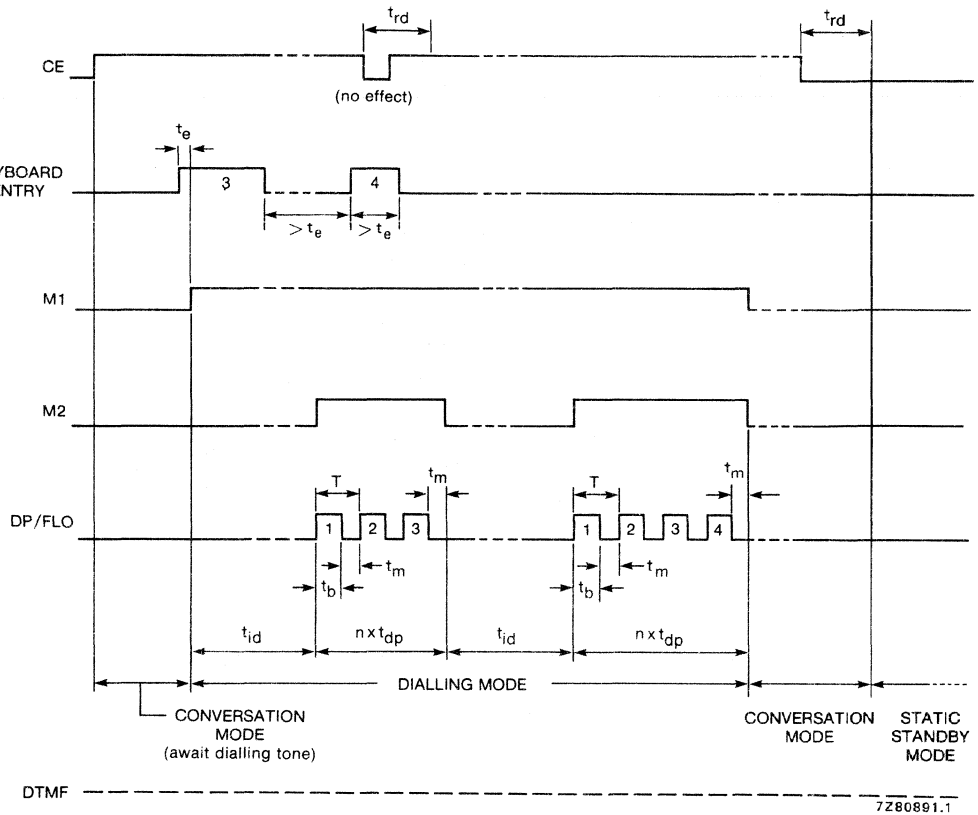


Fig. 8a Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling ($\overline{PD}$/DTMF = V_{SS}).

TIMING (continued)

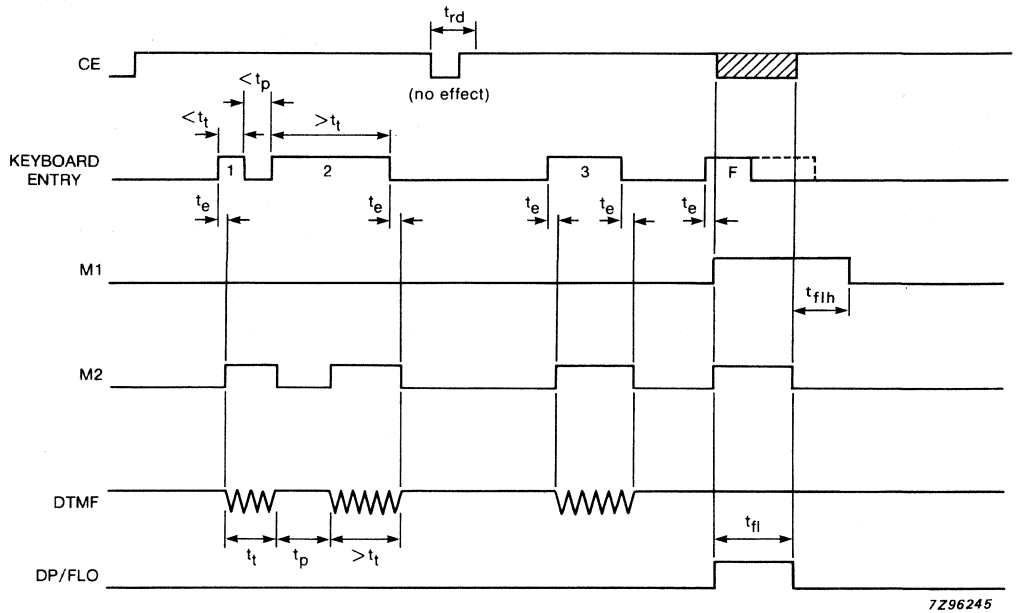


Fig. 8b Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).

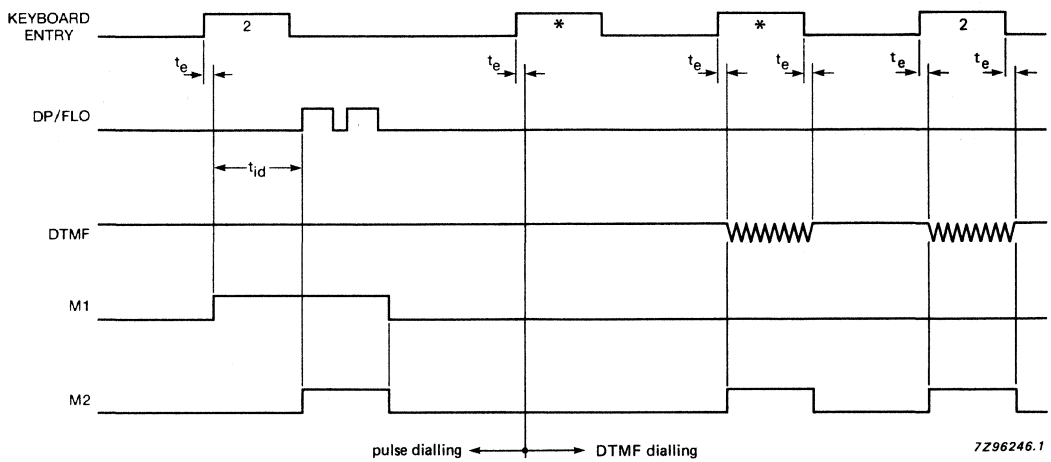


Fig. 8c Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling and data transmission mode.

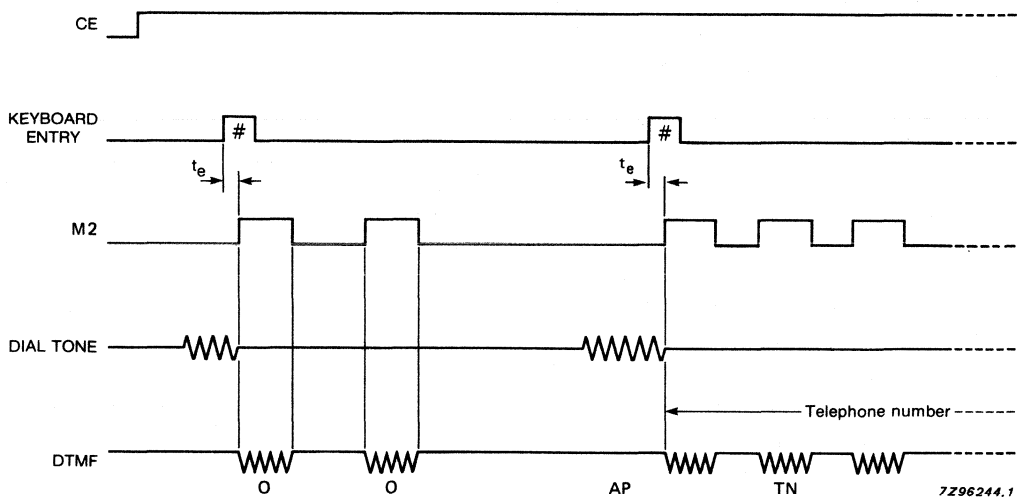


Fig. 9 Timing diagram showing REDIAL where PABX access digits are the first keyboard entries; DTMF dialling with $\overline{PD}$/DTMF = V_{DD}.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to 8 V
Supply current	I_{DD}	max.	50 mA
DC current into any input or output	$\pm I_I, \pm I_O$	max.	10 mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8 V
Total power dissipation	P_{tot}	max.	300 mW
Power dissipation per output	P_O	max.	50 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 70 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579545 MHz; R_S = 100 Ω max.; T_{amb} = −25 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Standby supply voltage	V_{DDO}	1,8	–	6,0	V
Operating supply current					
conversation mode (oscillator ON)	I_{DDC}	–	–	150	μA
pulse dialling or flash	I_{DDP}	–	–	200	μA
DTMF dialling (tone ON)	I_{DDF}	–	–	0,9	mA
DTMF dialling (tone OFF)	I_{DDF}	–	–	200	μA
Standby supply current (oscillator OFF; note 1) at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	–	–	5	μA
INPUTS					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current; CE	$\lvert I_{IL}\rvert$	–	–	1	μA
Keyboard inputs					
Keyboard ON resistance	R_{KON}	–	–	2	kΩ
Keyboard OFF resistance	R_{KOFF}	1	–	–	MΩ
OUTPUTS					
Output sink current at $V_{OL} = V_{SS} + 0{,}5$ V					
M1, M2, DP/FLO	I_{OL}	0,7	–	–	mA
Output source current at $V_{OH} = V_{DD} - 0{,}5$ V					
M1, M2, DP/FLO	$-I_{OH}$	0,6	–	–	mA
TIMING AND FREQUENCY					
Clock start-up time	t_{on}	–	4	–	ms
Debounce time	t_e	–	12	–	ms
Reset delay time	t_{rd}	72	80	88	ms

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 10) at V_{DD} = 2,5 to 6 V					
DTMF output voltage levels (r.m.s. value)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Frequency deviation	$\Delta f/f$	−0,6	—	+ 0,6	%
DC voltage level	V_{DC}	—	½V_{DD}	—	V
Output impedance	$\|Z_O\|$	—	0,1	0,5	kΩ
Load resistance	R_L	10	—	—	kΩ
Pre-emphasis of group	ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion at T_{amb} = 25 °C (note 2)	THD	—	−25	—	dB
Transmission and pause time					
Manual and data transmission dialling mode	t_t	65	—	—	ms
	t_p	135	—	—	ms
Redialling	t_t	65	70	75	ms
	t_p	135	140	145	ms
Flash pulse duration	t_{FL}	95	100	105	ms
Flash hold-over time	t_{flh}	32	34	36	ms
Pulse dialling (PD)					
Dialling pulse frequency	f_{dp}	9,6	10	10,4	Hz
Inter-digit pause	t_{id}	450	500	600	ms
Break time (note 3)	t_b	64	66	68	ms
Make time (note 3)	t_m	32	34	36	ms

DEVELOPMENT DATA

Notes to the characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Mark-to-space ratio 2 : 1.

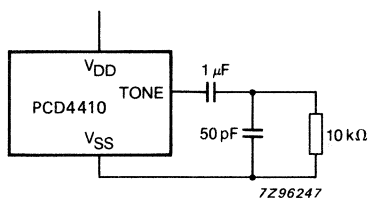
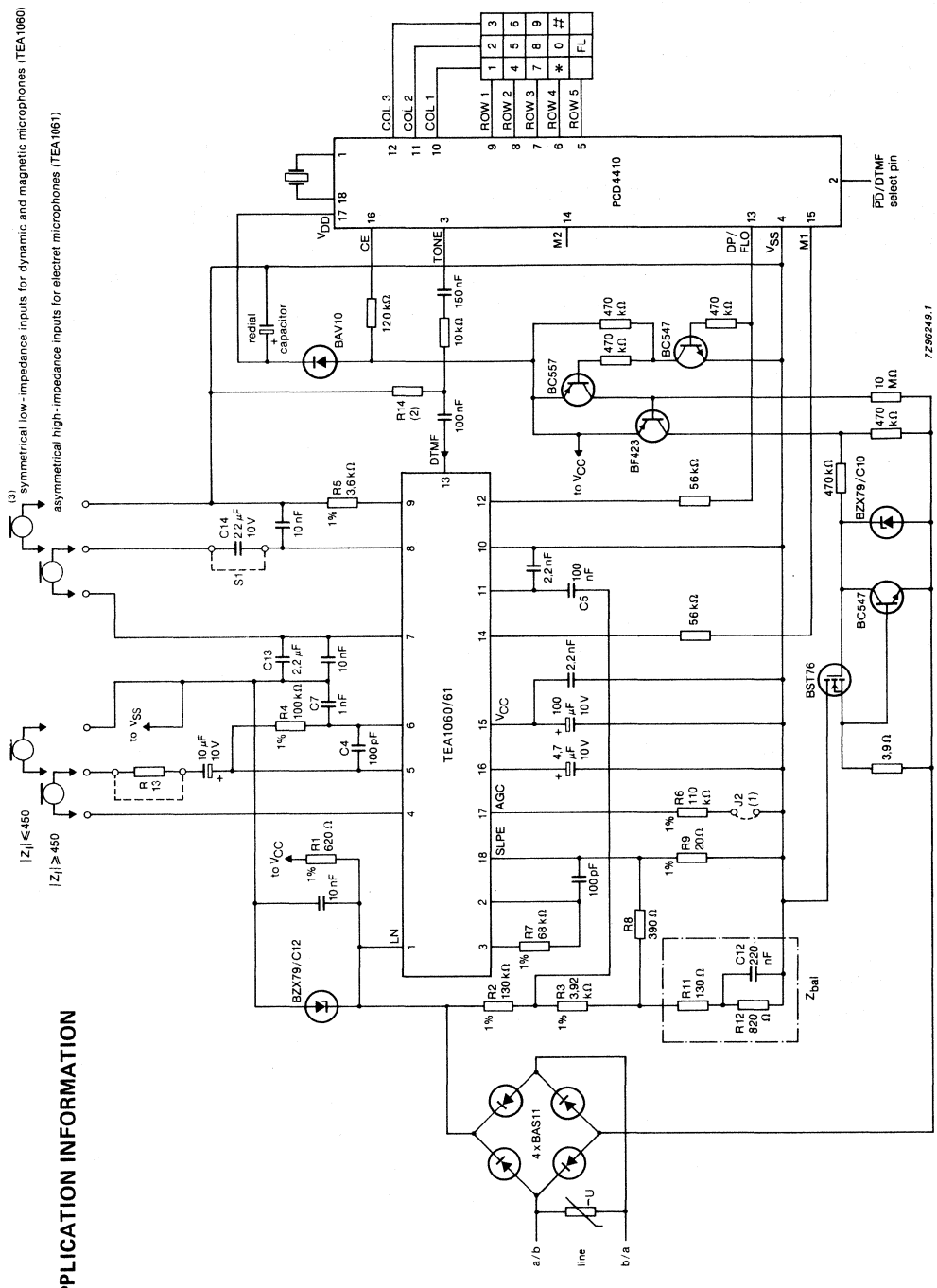


Fig. 10 Tone output test circuit.

APPLICATION INFORMATION



(1) Automatic line compensation obtained by connecting R6 to V_{SS}.
(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060.
(3) Omit C13 and C14; insert S1.

Fig. 11 Application diagram of the full electronic basic telephone set.

PULSE AND DTMF DIALLER

GENERAL DESCRIPTION

The PCD4413 is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3,58 MHz crystal. It is a dual-standard dialling circuit for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either PD or DTMF mode.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

Features

- Pulse and DTMF dialling
- 23-digit memory capacity
- Three dialling modes; pulse, DTMF and data transmission (DTMF)
- Two function keys; * and FL (flash)
- DTMF timing:
  manual dialling — minimum duration for bursts and pauses
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3,58 MHz (tv colour burst) crystal
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}		2,5 to 6,0 V
Standby supply voltage	V_{DDO}		1,8 to 6,0 V
Low standby current (on hook) at V_{DDO} = 1,8 V	I_{DDO}	max.	5 μA
Operating currents			
conversation mode	I_{DDC}	max.	150 μA
pulse dialling mode	I_{DDP}	max.	200 μA
DTMF dialling mode	I_{DDF}	max.	0,9 mA
DTMF output voltage level (r.m.s. values)			
HIGH group	$V_{HG(rms)}$	typ.	192 mV
LOW group	$V_{LG(rms)}$	typ.	150 mV
Pre-emphasis of group	ΔV_G	typ.	2,1 dB
Total harmonic distortion	THD		−25 dB
Operating ambient temperature range	T_{amb}		−25 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

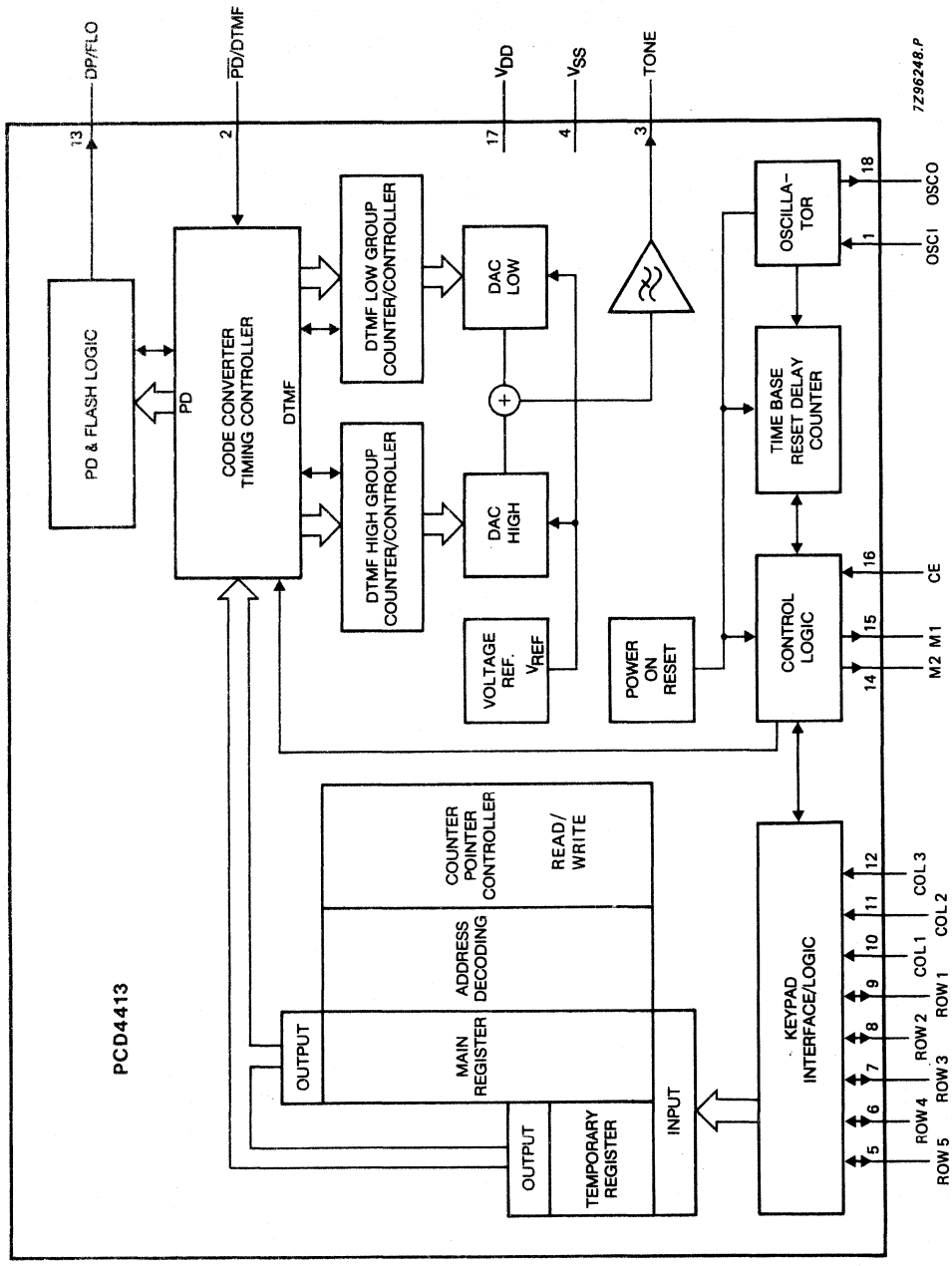


Fig. 1 Block diagram.

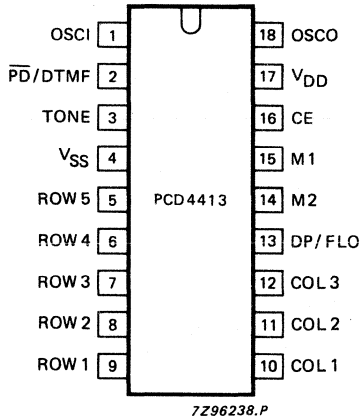


Fig. 2 Pinning diagram.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	ROW 5	scanning row keyboard input/outputs
6	ROW 4	
7	ROW 3	
8	ROW 2	
9	ROW 1	
10	COL 1	sense column keyboard inputs with internal pull-ups
11	COL 2	
12	COL 3	
13	DP/FLO	dialling pulse and flash output
14	M2	strobe; active HIGH during transmission
15	M1	muting output
16	CE	chip enable input
17	V_{DD}	positive supply
18	OSCO	oscillator output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.
To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.

The power-on-reset signal has the highest priority. It blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the PCD4413 for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, the keyboard input is inhibited and all registers and logic are reset with the exception of the Write Address Counter (WAC) which points to the last entered digit (see Fig. 4).
The current drawn is I_{DDO} (standby current) during hook-on.

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for more than time t_{rd} (see Fig. 7, Fig. 8 and timing data) the system changes to the static standby state and the oscillator stops running. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each pushbutton activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfil the CEPT CS 203 recommendations.

The duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

PD/Data transmission mode

If PD/DTMF = V_{SS} the pulse-data mode is selected. Starting with numeric keys digits will be dialled out in pulse dialling mode, until key * is depressed which selects the data transmission mode (the * tone is not transmitted). All keys (including * and #) will now be transmitted in DTMF tones.

There are two ways to leave the data transmission mode:

- Reactivate chip enable (CE); HIGH to LOW then HIGH again
- Pressing the flash (FL) key

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 3 and the scanning row outputs ROW 1 to ROW 5 of the PCD4413 are directly connected to the keyboard as shown in Fig. 3.
All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e as shown in Fig. 7, 8 and 9. Each entry is tested for validity.

When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the pushbutton.

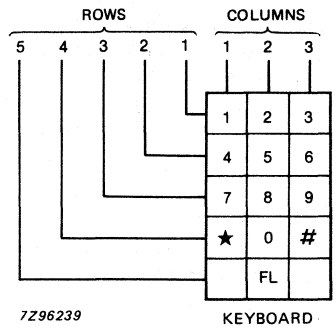


Fig. 3 Keyboard organization.

Row 5 of the keyboard contains the special function key FL — flash or register recall.

Flash

Flash (or register recall) is activated by the FL key and can be used in DTMF, pulse and data transmission modes. Pressing the FL pushbutton will produce a timed line-break of 100 ms at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. This flash pulse duration (t_{FL}) is calibrated at 100 ms.

The flash pulse resets the read address counter (RAC).

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

FUNCTIONAL DESCRIPTION (continued)

Table 1 Frequency tolerance of the output tones for DTMF signalling

row/ column	standard frequency Hz	tone output frequency Hz (1)	frequency deviation	
			%	Hz
row 1	697	697,90	+0,13	+0,90
row 2	770	770,46	+0,06	+0,46
row 3	852	850,45	−0,18	−1,55
row 4	941	943,23	+0,24	+2,23
col 1	1209	1206,45	−0,21	−2,55
col 2	1336	1341,66	+0,42	+5,66
col 3	1477	1482,21	+0,35	+5,21

(1) Tone output frequency when using a 3,579 545 MHz crystal.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output stays HIGH for the period of the transmit and pause time. During Flash the mute output is active HIGH and remains at this level for the period of flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD4413 it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break and make time in pulse dialling, or during tone transmission in DTMF dialling.

Data transmission mode

Timing in the data transmission mode is the same as the manual dialling mode.

DIALLING PROCEDURES (see also Figs 5 and 6)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig. 4). By entering first a numeric digit, the Write Address Counter (WAC) will be set to the first address, the decoded digit will be stored in the register and the WAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the main register after validation. All entries are debounced on both the leading and trailing edges for at least time t_e as shown in Figs 7, 8 and 9. Each entry is tested for validity before being deposited in the main register.

In pulse dialling mode only the 0 to 9 keys result in dialling operations.

* is a special function key:

* *key*

- Used to switch from dialling mode to data transmission mode. The * tones will not be transmitted.

In DTMF and data transmission mode keys 0 to 9, * and # result in associated DTMF tones (see Table 1).

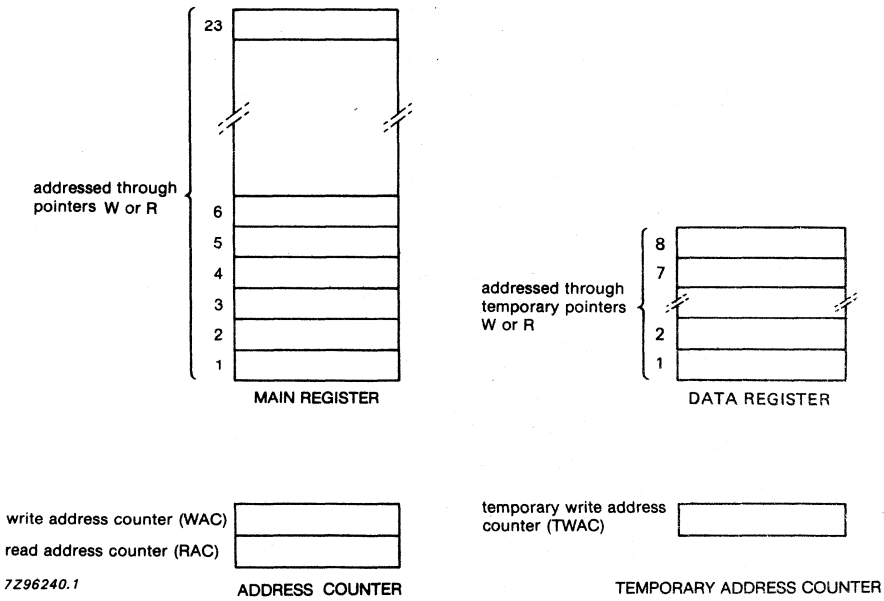


Fig. 4 Memory organization.

DIALLING PROCEDURES (continued)

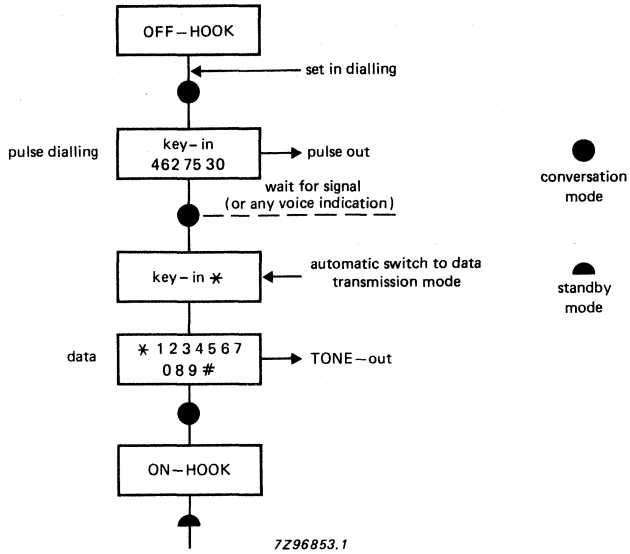


Fig. 5 Pulse and data transmission mode.

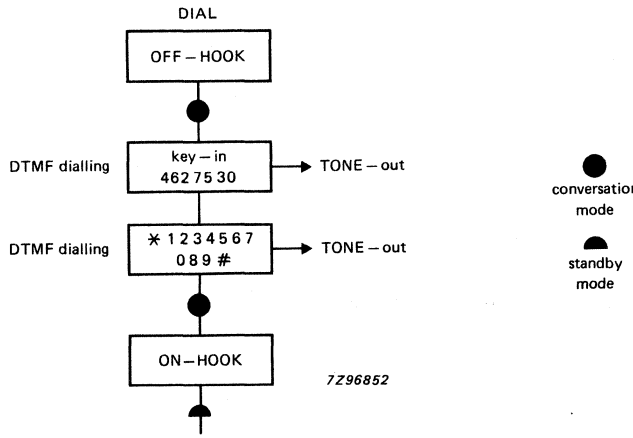


Fig. 6 DTMF mode.

DEVELOPMENT DATA

TIMING

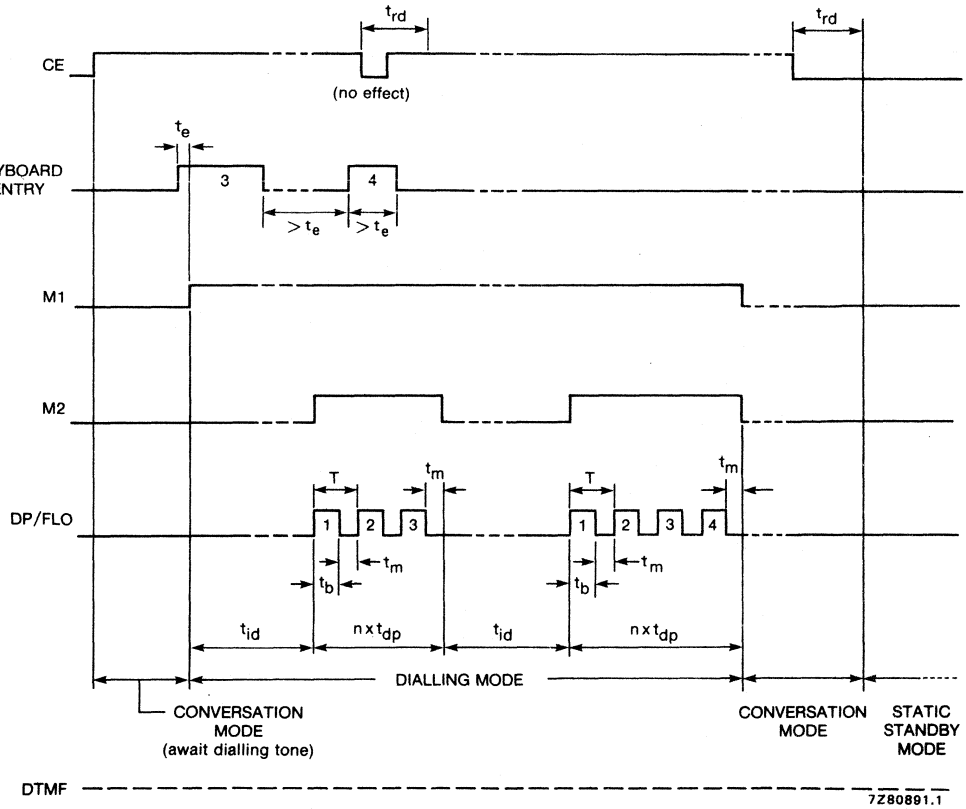


Fig. 7 Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling ($\overline{PD}$/DTMF = V_{SS}).

TIMING (continued)

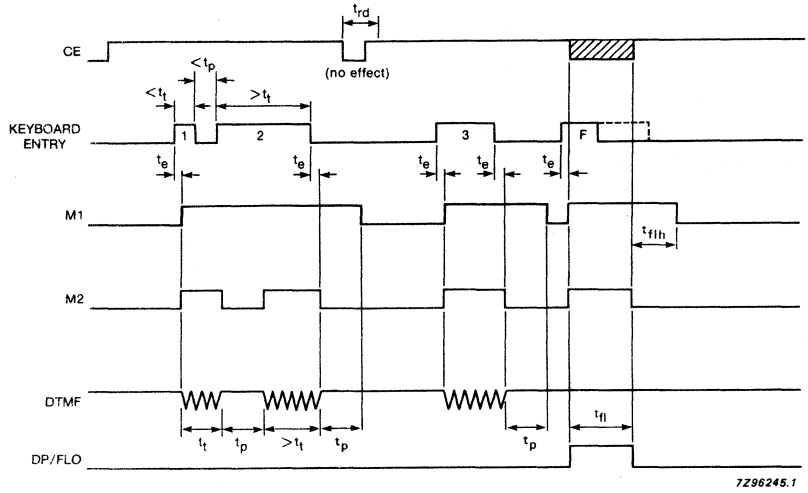


Fig. 8 Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).

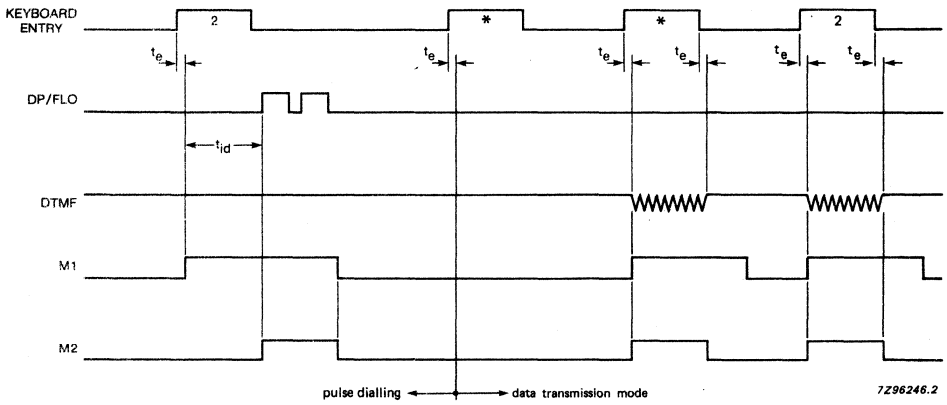


Fig. 9 Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling and data transmission mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to 8	V
Supply current	I_{DD}	max.	50	mA
DC current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579545 MHz; R_S = 100 Ω max.; T_{amb} = −25 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Standby supply voltage	V_{DDO}	1,8	–	6,0	V
Operating supply current					
conversation mode (oscillator ON)	I_{DDC}	–	–	150	μA
pulse dialling or flash	I_{DDP}	–	–	200	μA
DTMF dialling (tone ON)	I_{DDF}	–	–	0,9	mA
DTMF dialling (tone OFF)	I_{DDF}	–	–	200	μA
Standby supply current (oscillator OFF; note 1) at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	–	–	5	μA
INPUTS					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current; CE	$\lvert I_{IL}\rvert$	–	–	1	μA
Keyboard inputs					
Keyboard ON resistance	R_{KON}	–	–	2	kΩ
Keyboard OFF resistance	R_{KOFF}	1	–	–	MΩ
OUTPUTS					
Output sink current at $V_{OL} = V_{SS} + 0{,}5$ V					
M1, M2, DP/FLO	I_{OL}	0,7	–	–	mA
Output source current at $V_{OH} = V_{DD} - 0{,}5$ V					
M1, M2, DP/FLO	$-I_{OH}$	0,6	–	–	mA
TIMING AND FREQUENCY					
Clock start-up time	t_{on}	–	4	–	ms
Debounce time	t_e	–	12	–	ms
Reset delay time	t_{rd}	152	160	168	ms

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 10) at V_{DD} = 2,5 to 6 V					
DTMF output voltage levels (r.m.s. value)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Frequency deviation	$\Delta f/f$	−0,6	−	+ 0,6	%
DC voltage level	V_{DC}	−	$\frac{1}{2}V_{DD}$	−	V
Output impedance	$\lvert Z_O \rvert$	−	0,1	0,5	kΩ
Load resistance	R_L	10	−	−	kΩ
Pre-emphasis of group	ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion at T_{amb} = 25 °C (note 2)	THD	−	−25	−	dB
Transmission and pause time					
Manual and data transmission dialling mode	t_t	65	−	−	ms
	t_p	65	−	−	ms
Flash pulse duration	t_{FL}	95	100	105	ms
Flash hold-over time	t_{flh}	30	32	34	ms
Pulse dialling (PD)					
Dialling pulse frequency	f_{dp}	9,8	10	10,4	Hz
Inter-digit pause	t_{id}	800	840	880	ms
Break time (note 3)	t_b	58	60	62	ms
Make time (note 3)	t_m	38	40	42	ms

Notes to the characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Mark-to-space ratio 3 : 2.

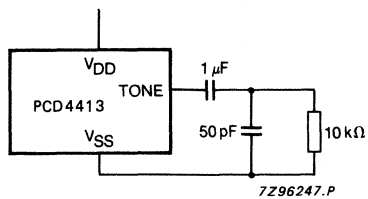
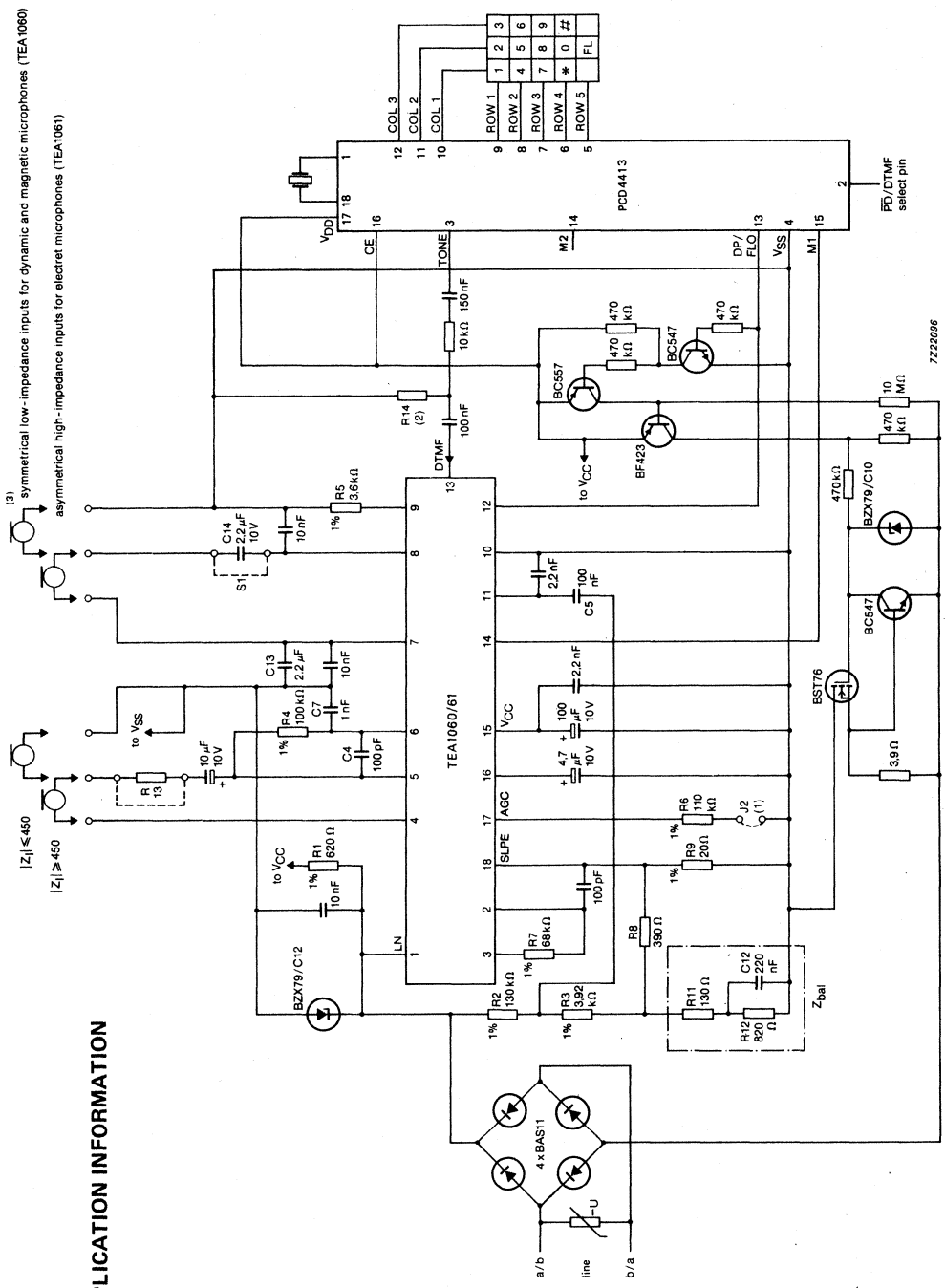


Fig. 10 Tone output test circuit.

APPLICATION INFORMATION



(1) Automatic line compensation obtained by connecting R6 to V_{SS}.
(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060/61.
(3) Omit C13 and C14; insert S1.

Fig. 11 Application diagram of the full electronic basic telephone set.

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